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Generic Hardware Platform for future high-bandwidth detector readout

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In the High Energy Physics (HEP) and Nuclear Physics (NP) experiments, there is always a wish to readout all the detector data to improve efficiency and avoid losing potential useful information. This requirement motivates the development of technologies such as the on-detector processing, high speed data links and powerful back-end electronics. The Front-End Link eXchange (FELIX) system is an interface between the detector and trigger readout electronics and commodity switched networks for the ATLAS experiment at CERN. The FELIX approach takes advantage of modern FPGAs and commodity computing to reduce the system complexity and effort needed to support data acquisition systems in comparison to previous designs. FELIX Phase-I hardware (FLX-712) is based on the generic PCIe form factor with Kintex Ultrascale FPGA with support of PCIe Gen3. It has been widely adopted by other HEP and NP experiments - sPHENIX at RHIC, ProtoDUNE-SP at CERN, CBM/RE21 at FAIR, test beam experiments at Fermilab and CERN. The Phase-II design FLX-182 and FLX-155 are based on the AMD Versal FPGA with support of PCIe Gen4/5 and 25Gb/s optical links. It has been and is going to be tested by several HEP and NP experiments - ePIC at EIC, sPHENIX at RHIC, LHCb at CERN, ALICE at CERN, CBM/RE21 at FAIR. In addition, CERN DRD7 (Electronics) collaboration has it as a hardware platform for adaptation from Front-End to Back-End with 100+ GbE in one of Work Packages. This rapid improvement in the back-end electronics is a paradigm shift and enables triggerless readout of the future particle experiments that maximize their discovery potential. The design and test results of Versal FPGA based FELIX development will be presented in this contribution.

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