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Design and characterization of 28nm readout ASICs for 3D-integrated LGAD sensors

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Highly granular precision timing detectors are required to achieve scientific breakthroughs across HEP, NP, BES, and FES applications, and their critical need was highlighted by DOE BRN, European Strategy for Particle Physics, and Snowmass. To enable the development of these detectors, 3D-intgration between advanced sensor wafers and scaled CMOS technology nodes is required but is currently cost-prohibitive for use in scientific applications and experiments. Closing this technology gap is the main objective of the joint SLAC, FNAL and LLNL effort "3D Integrated Sensing Solutions", supported by DOE's Accelerated Innovation in Emerging Technologies grant. In collaboration with leading semiconductor industry partner, this effort is pursuing development of LGAD structures compatible with fabrication in commercial 12-inch wafer processes that can be cost-effectively 3D-integrated with readout ASICs. In parallel with the LGAD development, a co-design effort in the development of high-performance readout ASICs is underway and will be the subject of this talk. The first readout ASIC prototype has been fabricated and tested. It features a linear array of 40 pixels with 50 µm and 100 µm pitch, matched to LGAD cell variants. Each pixel integrates a low-jitter front-end, fast comparator, and a high-resolution in-pixel Time-to-Digital Converter (TDC). The system targets timing resolution below 20 ps with power consumption under 1 W/cm². Initial testing confirms ~10 ps jitter for the in-pixel TDCs. The TDC employs a 2D Vernier ring oscillator architecture with an embedded sliding-scale technique, enabling simultaneous measurement of Time-of-Arrival (TOA) and Time-over-Threshold (TOT) with resolutions of 6.25 ps (11-bit) and 50 ps (8-bit), respectively. Power consumption scales with occupancy, averaging 51.1 µW at 10% and 6.2 µW at 1% occupancy per TDC.
The prototype has been characterized using on-chip charge injection and will be wire-bonded to LGAD sensors. Finally, we will present the design of the second-generation 10k-pixel ASIC scheduled for fabrication in September, to be bump bonded to designed LGAD sensors for testing and system validation.

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