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Network intelligence for fault tolerance and data load balancing

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This project will use on-chip machine learning algorithms to produce intelligent networks. Both conventional digital logic and spike-based neuromorphic implementations will be explored. Two network scales will be prototyped: a multi-chip network, where each element is a complex functionality sensor and many sensors are integrated on a circuit board to form the network (suitable for DUNE or other detectors of similar scale), and a network-on-chip, where the individual pixels of a sensor are the network elements (suitable for collider pixel detectors). Both these cases are 2-dimensional, regular geometry networks, where each element has exactly 4 neighbors. A third case, corresponding to an ad-hoc wireless network in 3-dimensional space, relevant for proposed smart dust detector systems, will be investigated with theory and simulation.

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