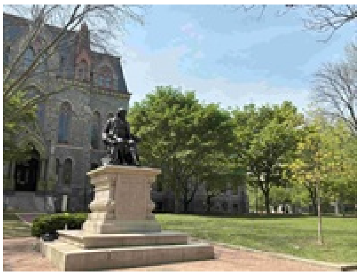

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# Megapixel Monolithic Active Pixel Sensor Prototype with Event-Driven Readout and Pathway to Electro-Photonic Integration

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Future collider experiments and upgrades in high-energy physics (HEP) and nuclear physics (NP) demand vertex and tracking detectors that combine extreme granularity, minimal material budget, and precise timing. The Brookhaven National Laboratory (BNL) carried out development of a 1-megapixel monolithic active pixel sensor (MAPS) prototype addresses these needs by uniting binary event-driven readout with an ultra-low-power analog front-end (AFE) and a half-duplex EDWARD (Event-Driven with Access and Reset Decoder) architecture. Designed in the same Tower Partners Semiconductor (TPSCo) 65 nm process used for ALICE-ITS3, the prototype targets ˜20 µm pixels, ˜100 ns or better time resolution, and sub-nA per-pixel bias currents via a temperature-compensated current reference. This configuration eliminates the power and bandwidth inefficiencies of traditional frame-based or continuously scanned readouts, delivering zero activity in the absence of events and collision-free arbitration without pixel-level geo-priority.

The design implements a modular column-based parallel readout structure, scalable to stitched large-area devices. In addition to the 0.5 V AFE and EDWARD logic, the reticle will include test structures for future functionality expansions. Mechanical considerations are integrated from the outset: the MAPS will be fabricated on thinned (˜50 µm) wafers, enabling self-supporting stave structures without the need for additional support materials, thus minimizing the detector radiation length.

The half-duplex EDWARD readout supports both greedy and non-greedy arbitration, selective per-pixel configuration, and in-pixel multi-channel analysis, all while maintaining minimal logic footprint. This approach draws on lessons from neuromorphic engineering, enabling frameless, asynchronous event capture with synchronous output serialization—compatible with both AI-driven near-sensor processing and conventional DAQ systems. Its scalability makes it equally applicable to spectroscopic imaging, safeguards monitoring, and compact field-deployable detectors.

Looking forward, this architecture is intended as a bridge to electro-photonic readout. Building on synergies with the DOE-funded El-Pho project, the post-pixel data flow will migrate from traditional copper interconnects to photonic technology hosting silicon photonic transceivers. This will support multi-channel wavelength-division multiplexed (WDM) optical links at ≥6 × 10 Gbps per link while delivering Watt-level optical power for "power-over-fiber"schemes. Such integration will improve signal integrity, reduce cabling mass, and enable long-distance, high-bandwidth data transport with immunity to electromagnetic interference—essential for next-generation colliders such as the FCC-ee, where per-pixel hit rates are projected to be >25× higher and timing resolution demands >50× greater than current LHC detectors, for nearly identical power density.

Completion of this development will position BNL as a U.S. center for MAPS technology in HEP, NP, and beyond. In the nearer term, the 1 Mpixel prototype will serve as a demonstrator for EIC Silicon Vertex Tracker upgrades, with potential to replace priority-encoder-based matrices (e.g., ALICE-ITS3 MOSAIX) with EDWARD-driven architectures, or to underpin fully BNL-designed stitched MAPS for collider experiments. In the longer term, coupling this low-latency, low-power, large-area MAPS platform with integrated electro-photonic data transport offers a clear roadmap to meet—and surpass—the performance requirements of the next generation of high-granularity detectors.

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