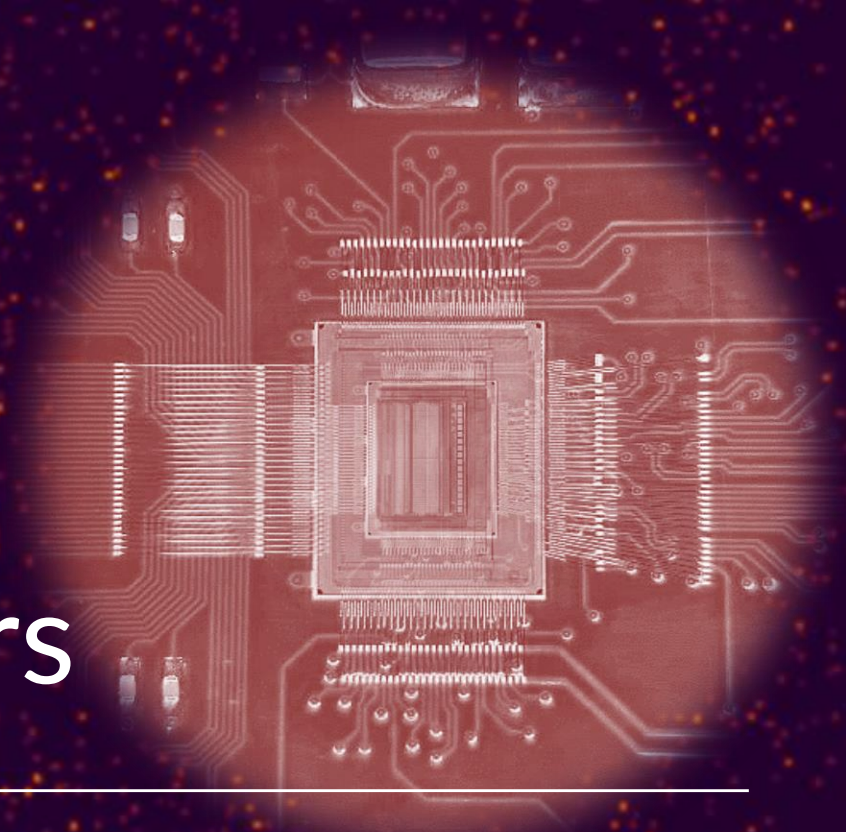


MAPS with improved timing performance for low-duty cycle accelerators



Lorenzo Rota, Aiden Duncanson, Bojan Markovic, Megan Zeng, Victor Turbiner, Christos Bakalis, Caterina Vernieri, Martin Breidenbach, Angelo Dragone

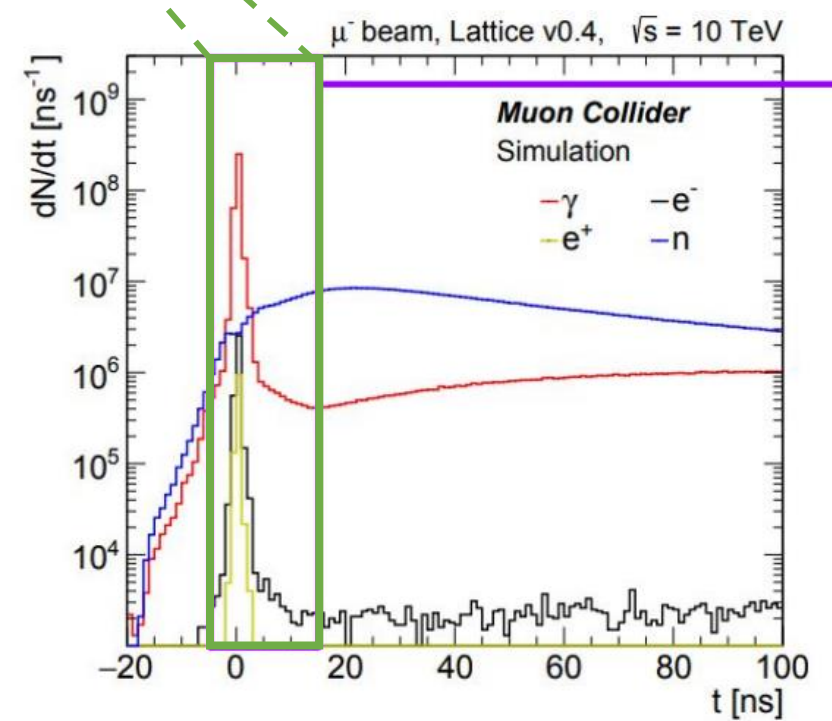
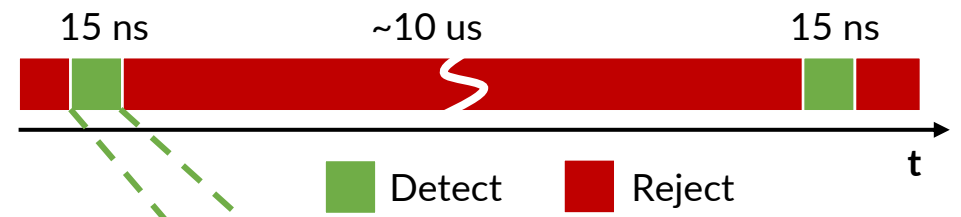
lorenzor@slac.stanford.edu

Tracking detectors for muon collider

from S. P. Griso & T. Heim
talks @ CPAD 2024

- A muon collider looks like “low-duty cycle” machine*:
 - Bunch crossing 10-30 μs
 - Need to “reject” hits outside of 15 ns timing window
 - “Duty cycle”: 0.15%

	muC Tracker		
	Vertex Detector	Inner Tracker	Outer Tracker
Resolution [$\mu\text{m} \times \mu\text{m}$]	25x25	50x1,000	50x10,000
Channels	1200M	290M	170M
Area [m^2]	0.75	14.5	85
Double Layer Spacing [mm]	2mm		
Total Ionizing Dose [Mrad]*	200	10	
Fluence [1MeV neq/ cm^2]*	3×10^{15}	1×10^{16}	$< 1 \times 10^{15}$
Time resolution	30ps	60ps	
Hit density [mm^{-2}]	3.7**	0.5**	0.03**

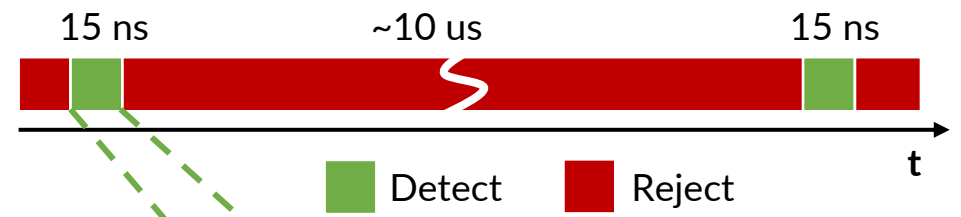


* from a front-end electronics designer point of view

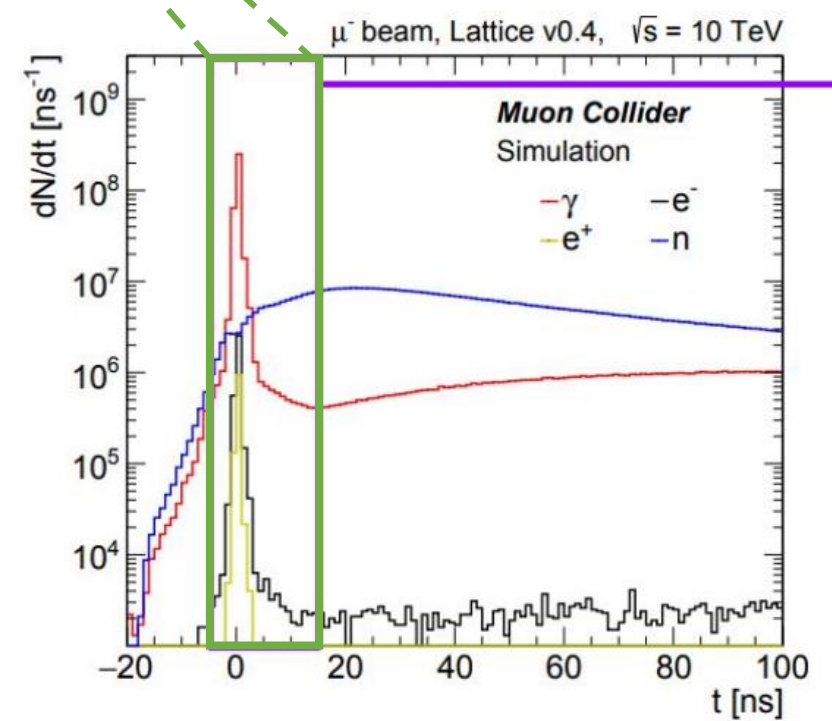
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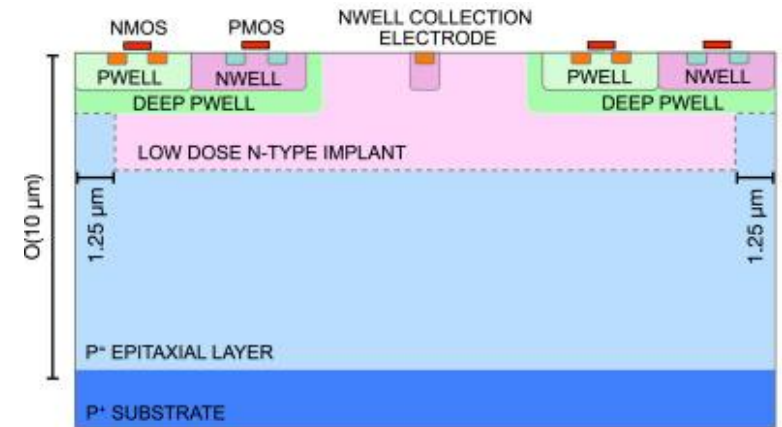
Probably need scaled CMOS node?
See B. Markovic's talk: LGAD+28nm
Wednesday 5:50 PM

What can be achieved with current MAPS technology?

* from a front-end electronics designer point of view

MAPS technology choice

- **Technology:**
 - TPSCo 65nm, optimized by CERN → see talks by G. Deptuch
- **Radiation hardness:**
 - proof-of-principle that can operate up to 10^{15} neq [1, 2]
- **Timing resolution:**
 - Is the “sensor” fast enough?
 - Achieved “time resolution of 63 ps* with over 99% detection efficiency” with 10 μm pitch [3]
 - Can the sensor be further optimized?
 - R&D from CERN to further reduce detector capacitance, see last DRD7.6a meeting



[4] G.A. Rinella et al., Digital pixel test structures implemented in a 65 nm CMOS process

This talk:

Can we design analog FE and time-to-digital conversion circuitry to achieve sub-100 ps in this technology?

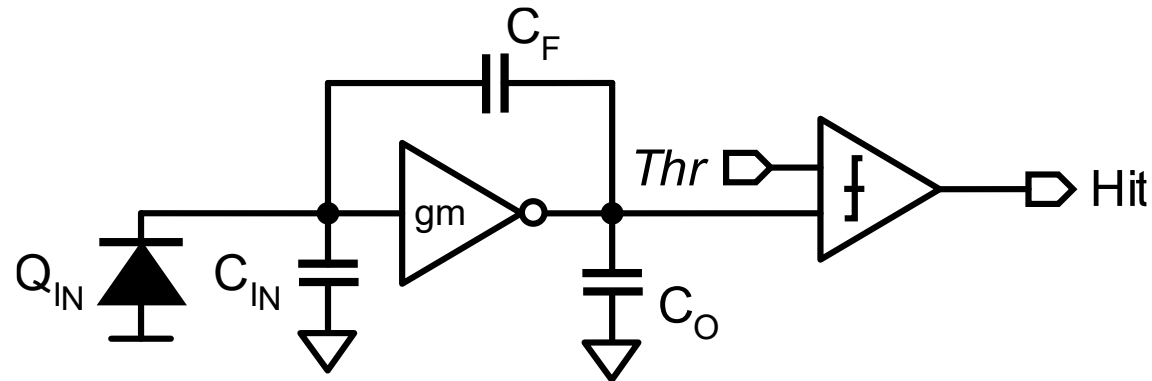
[1] F. Reidt, MAPS sensor developments in ALICE, [link](#)

[2] Letter of intent for ALICE 3: A next-generation heavy-ion experiment at the LHC, [arxiv](#)

[3] Time performance of APTS with in-chip operational amplifier implemented in 65 nm CMOS imaging process, [arxiv](#)

* Obtained on small test-structure, with off-chip processing based on CFD + additional time-walk correction based on cluster-size)

Pixel front-end: timing basics



- Jitter in a front-end architecture with CSA [1]:
$$Jitter = \frac{1}{Q_{in}} q Enc \frac{C_O}{g_m} (1 + C_{IN}/C_{FB})$$

- Reducing jitter:

- Increase power consumption
- Reduce noise
- Decrease ratio C_{IN}/C_{FB}
- Reduce capacitance at CSA output
- Time-walk is also reduced

→ limited power budget

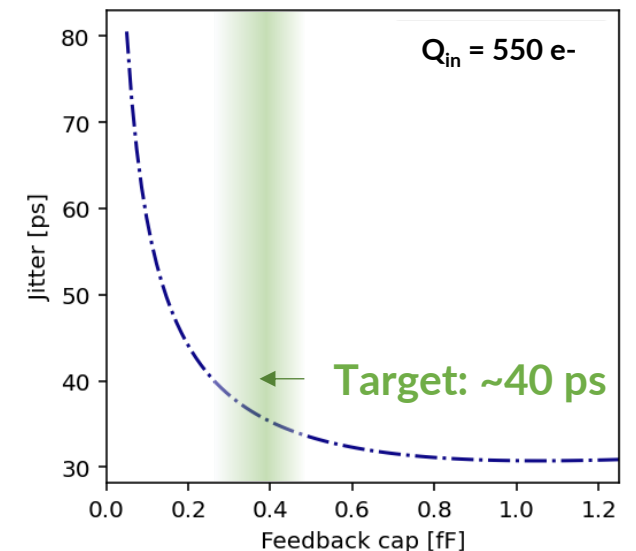
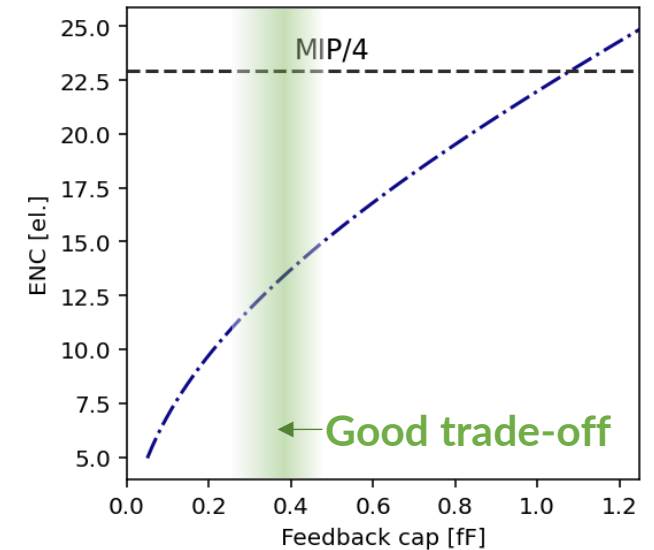
} Trade-off: noise, timing performance, threshold dispersion

→ optimize circuit & adopt scaled CMOS nodes

→ important if we want to gate the front-end

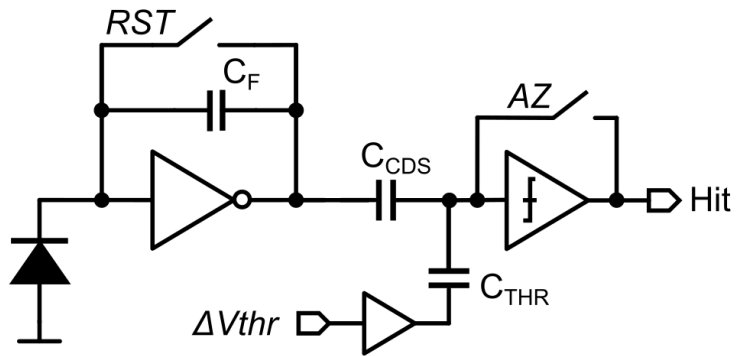
Pixel front-end: timing optimization

- Developed a more complete numerical simulation, including:
 - gm / power
 - ENC from noise, bandwidth and noise shaping
 - Discriminator noise
 - Threshold set to $6 \times \text{ENC}$
- Assuming $3 \mu\text{W}/\text{pixel}$, simulations shown on right :
 - ENC versus C_{FB} → upper limit to feedback capacitance
 - Jitter versus C_{FB} → expected $1/C_{\text{FB}}$ trend, with minimum
- Not shown, but equally important:
 - Lower $C_{\text{FB}} \rightarrow \downarrow$ amplitude at CSA out $\rightarrow \uparrow$ threshold dispersion
 - $\rightarrow \uparrow$ discriminator gain

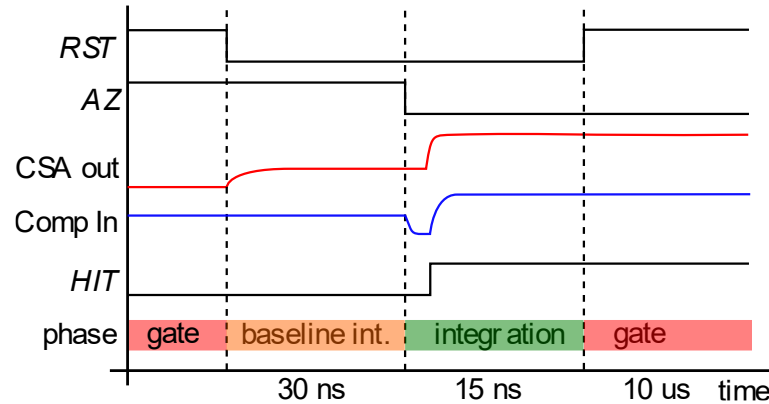


Pixel front-end: architecture

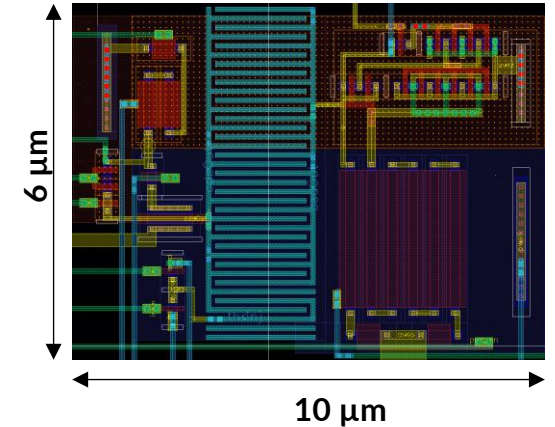
Simplified schematics of pixel front-end architecture



Timing diagram



Layout of front-end schematics in NAPA v2 (not optimized for area)



Main design approach:

- Gating implemented in front-end amplifier
- Time-variant front-end with Correlated Double Sampling (CDS) noise shaping
- Auto-zeroed, inverter-based comparator
- Capacitance at output of CSA is minimized during "detection" phase: <2fF
- **Digital signal from multiple front-ends sent to one TDC \rightarrow "macro-pixel" (see next slides)**

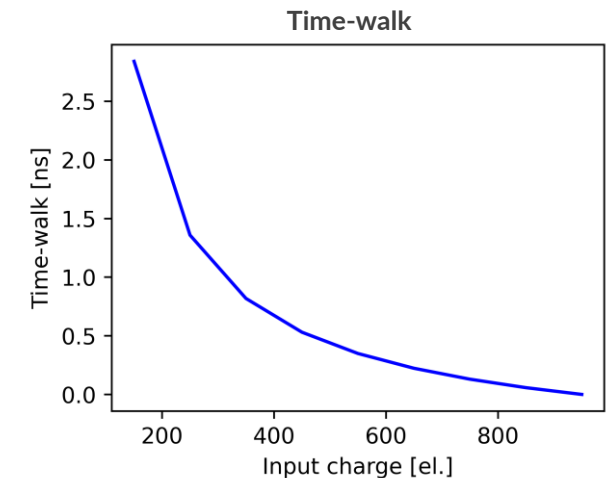
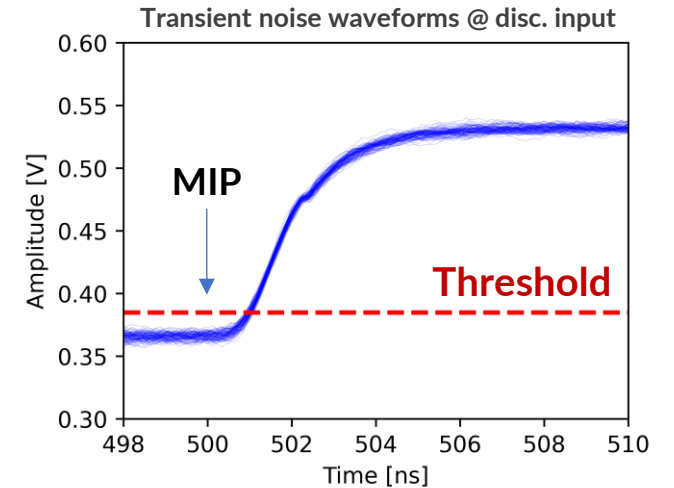
Pixel front-end: timing performance

- Preliminary simulation results of pixel front-end*:

- ENC: 16 e⁻
- Jitter: 36.8 ps
- Current: 2.6 μA
- Timewalk: 3 ns → “gating” accuracy of 15±3 ns

- Limitations of current circuit/model:

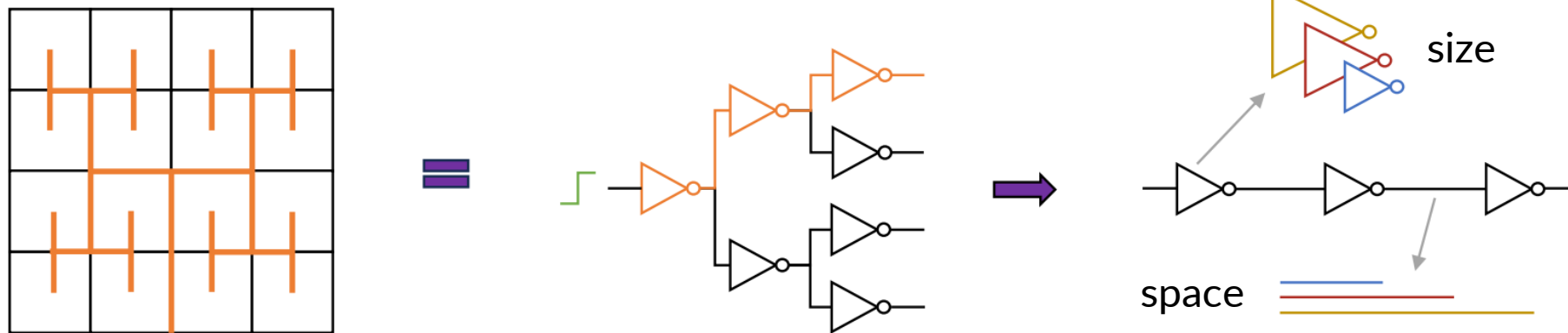
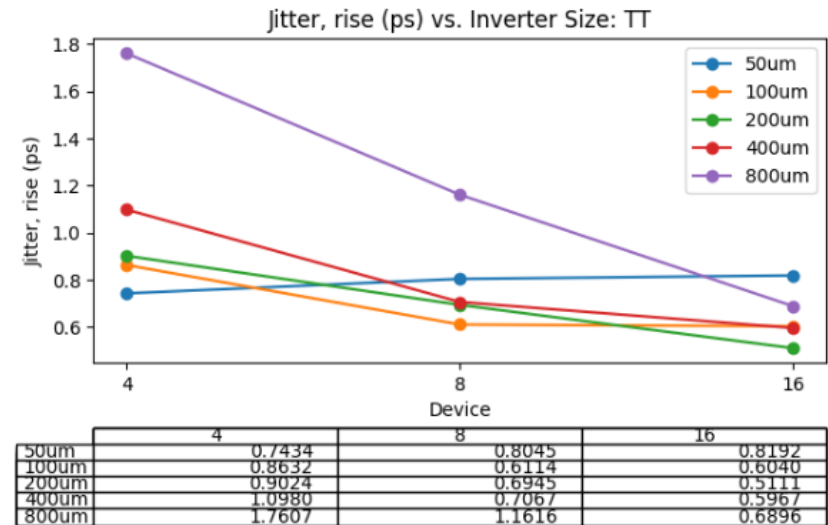
- Circuitry for TOT not included, needed for time-walk correction
- Assuming a 1 ns rise time for typical signal
- Contribution to threshold dispersion due to custom MOMcaps cannot be simulated accurately



Clock & timing signal distribution

M. Zeng (Stanford - HEPIC), B. Markovic

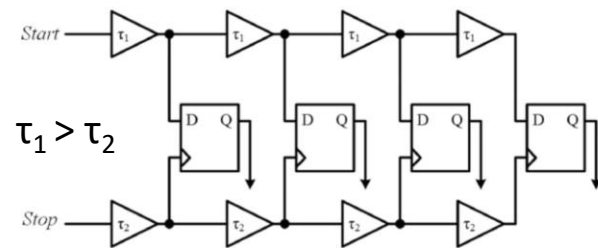
- Clock & signal distribution network strategy based on H-tree
- Evaluate performance for different buffer size & spacing
- Assuming a 256x256 matrix of 50 μm pixels:
 - Jitter*: $\lt; 2\text{ ps}$
 - Power consumption @100 kHz clock freq: **0.1 mW/cm²**
 - Power scales linearly with rep-rate & number of signals



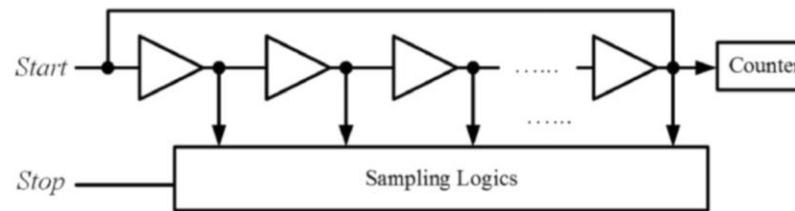
TDC Architecture

A. Duncanson, M. Zeng (Stanford - HEPIC), B. Markovic

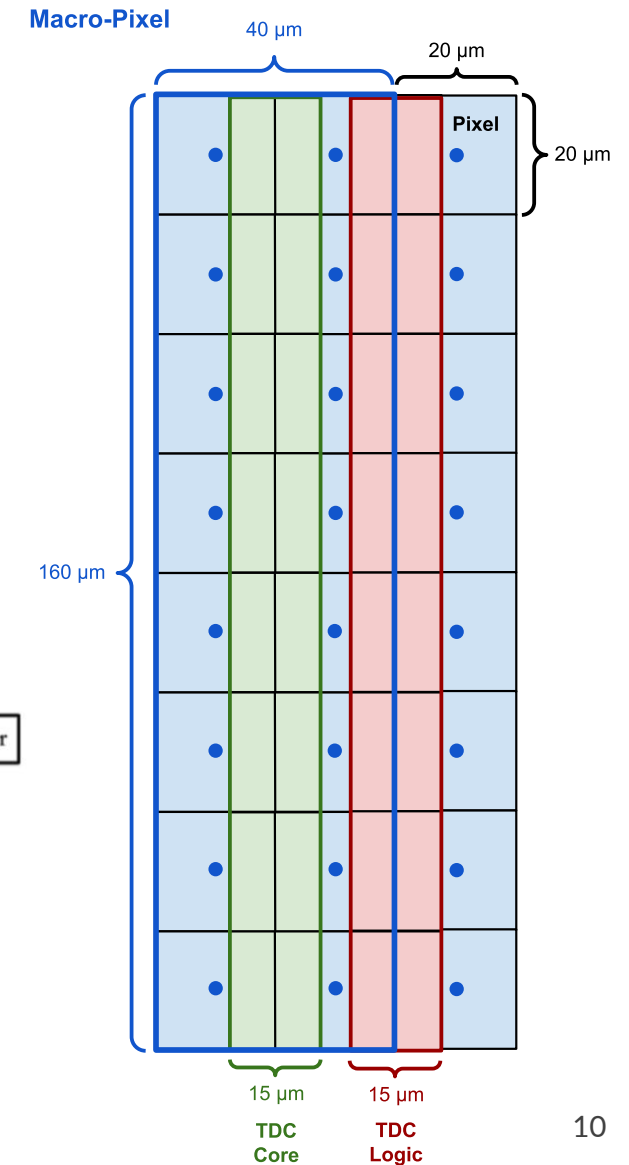
- Multiple pixel analog front-ends connected to one TDC
- HIT information from pixel combined in digital domain \rightarrow START signal
- Clock \rightarrow STOP signal
- Time-to-Digital Converter (TDC) architecture [1]:
 - Vernier Delay line: high resolution ($\tau_1 - \tau_2$)
 - Ring Oscillator: large dynamic range due to counter



Vernier Delay Line



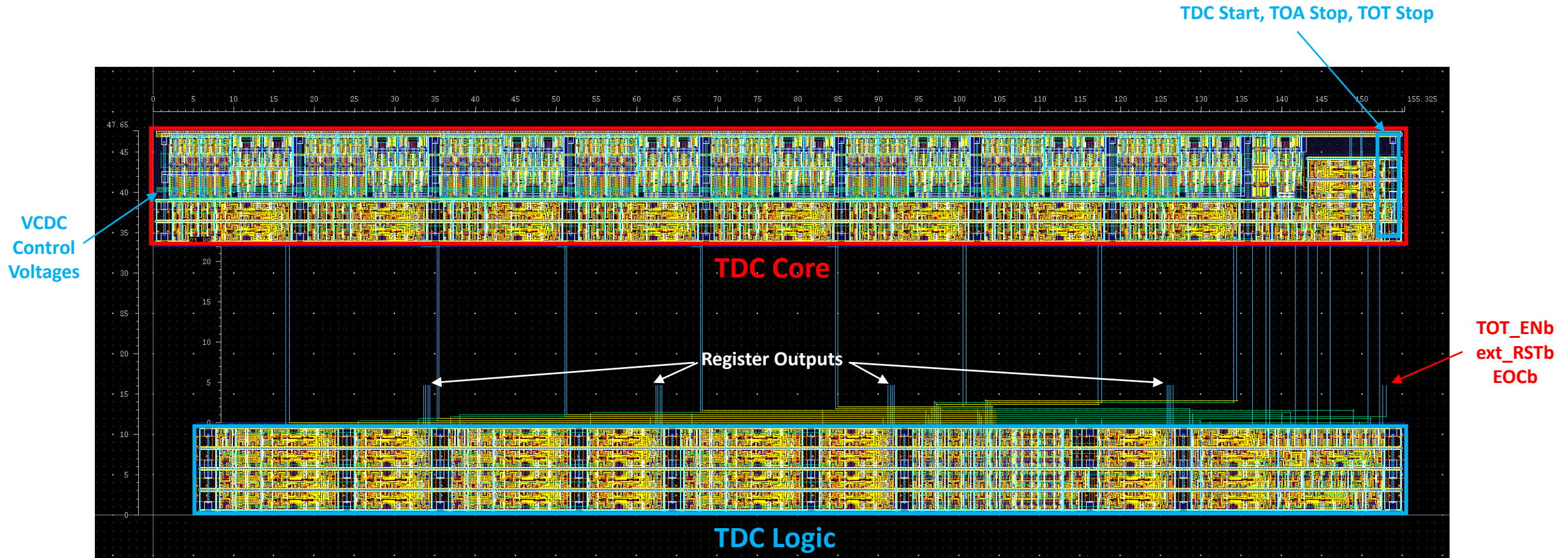
Ring Oscillator (RO)



TDC: Layout

A. Duncanson, M. Zeng (Stanford - HEPIC), B. Markovic

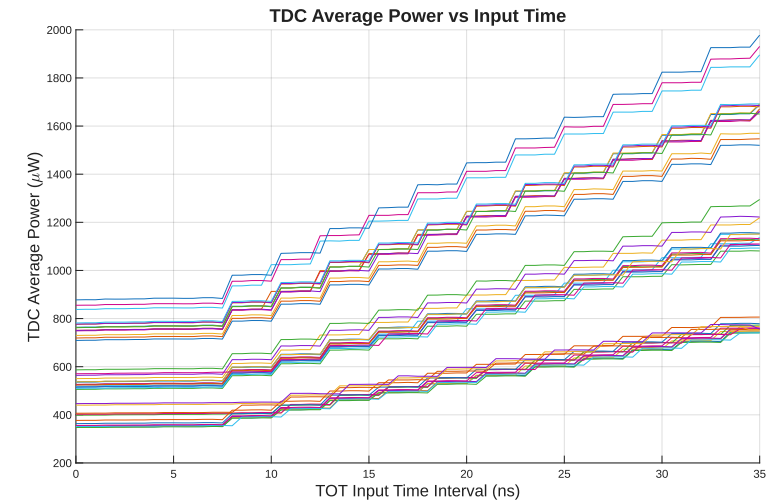
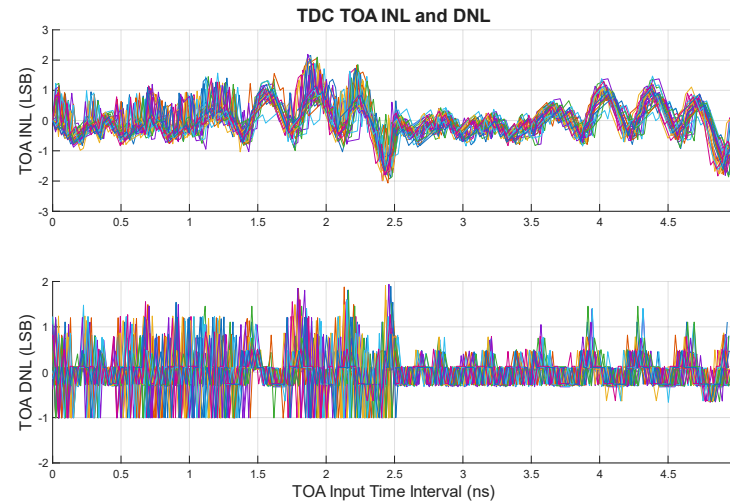
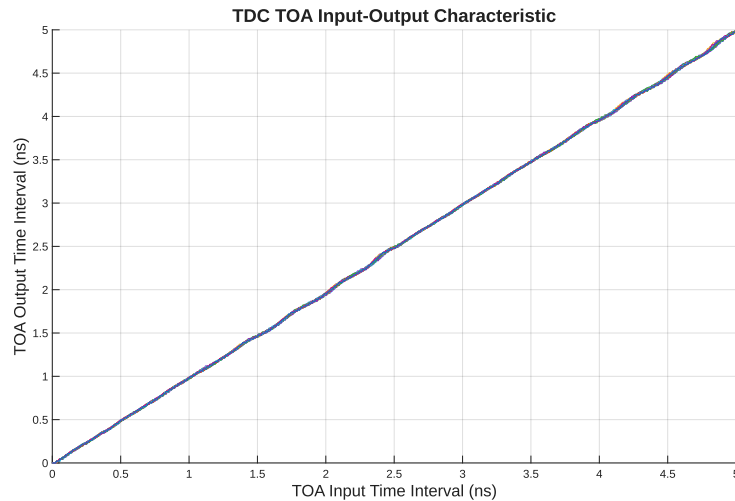
Full TDC area: TDC Core + TDC Logic = 4,250 μm^2



TDC: Post-layout simulations

A. Duncanson (Stanford - HEPIC), B. Markovic

TOA Simulations Across Corners¹



- **TOA resolution:** 20 ps
- **TOT resolution:** 2.5 ns
- **Power consumption:**
 - If no HIT: only static power consumption due to leakage
 - If HIT: 6 μ W assuming continuous conversion every 10 μ s \rightarrow scaled by macro-pixel occupancy

Putting it all together: power breakdown

- **Power in pixel analog front-end dominates power consumption**

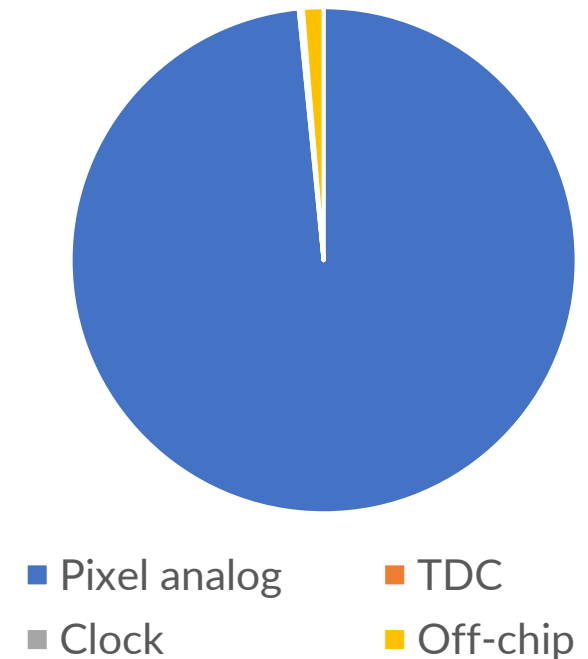
- Estimated power consumption:

- Analog front-end: 750 mW (2.6 μ A/pixel)
- TDC: 1 mW
- Clock distribution: 1 mW
- Off-chip data link: 10 mW

- Assumptions:

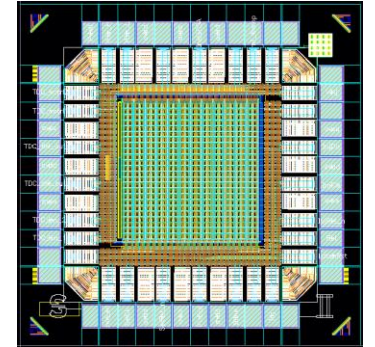
- Bunch-crossing: 10 μ s
- Occupancy: 100 hits / cm^2 / BX (assuming in-pixel timing cuts)
- Macro-pixel pitch: 200 \times 60 μ m
- Pixel pitch*: 20 μ m (!!!)

Power consumption breakdown



Summary & next steps

- **A chiplet prototype was submitted in CERN ER2 run (NAPA v2):**
 - Designed for \sim ns timing performance, but should achieve $O(100)$ ps jitter
 - Includes pixels matrix & test structure for TDC (delay cells) for characterization
- **Takeaways:**
 - Required timing performance can be achieved, analog FE power is bottle-neck
 - Gating is feasible with time-variant front-end with $O(\text{ns})$ accuracy
- **Next steps & community engagement:**
 - Future R&D:
 - can sensor pitch be relaxed without degrading timing / noise performance?
 - is power-pulsing an option at 10-30 μs rep-rate?
 - TDC being developed as IP block, part of DRD7.6a
 - Discussing collaborations with other groups exploring timing performance of TPSCo 65nm



Thank you for your attention

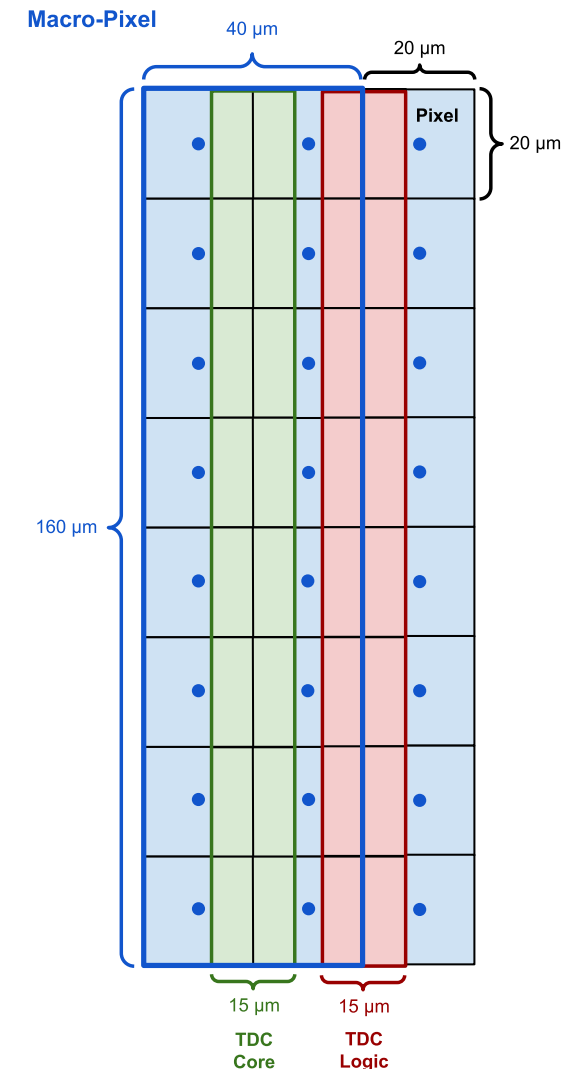
Acknowledgments:

- CERN-ME & ALICE group for providing access & support to TPSCo 65nm technology
- Walter Snoeys for the useful discussions which guided the TDC specifications

TDC Specifications Achieved

A. Duncanson (Stanford - HEPIC), B. Markovic

Parameter	Min	Typical	Max
Process Node		TowerJazz 65 nm CIS	
Supply Voltage	1.0 V	1.2 V	1.4 V
Substrate Bias		-1.2 V	
TOA Resolution		20 ps	
TOA Dynamic Range		15 ns	
TOT Resolution		2.5 ns	
TOT Dynamic Range		35 ns	
Conversion Time ¹			40 ns
TDC Core Area ²		14.4 μm x 155.5 μm	
TDC Logic Area ²		13.4 μm x 149.9 μm	
Average Power ³		150 μW (10% occupancy) 15 μW (1% occupancy)	
Temperature	-40 $^{\circ}\text{C}$	20 $^{\circ}\text{C}$	80 $^{\circ}\text{C}$



¹ Dead time required for **both** TOT and TOA valid data and reset, measured from start of conversion.

² TDC broken down into "core" and "logic" connected across separate bays within pixel grid.

³ Estimate. TDC average power depends on distribution of TOA and TOT, PVT, pixel occupancy, etc.