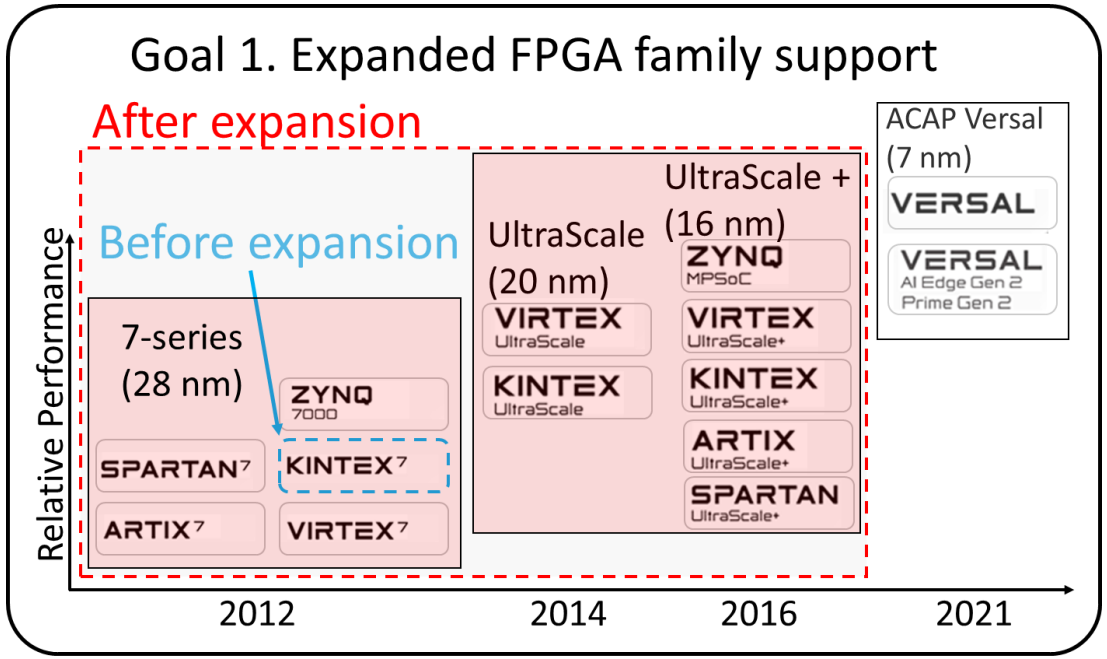
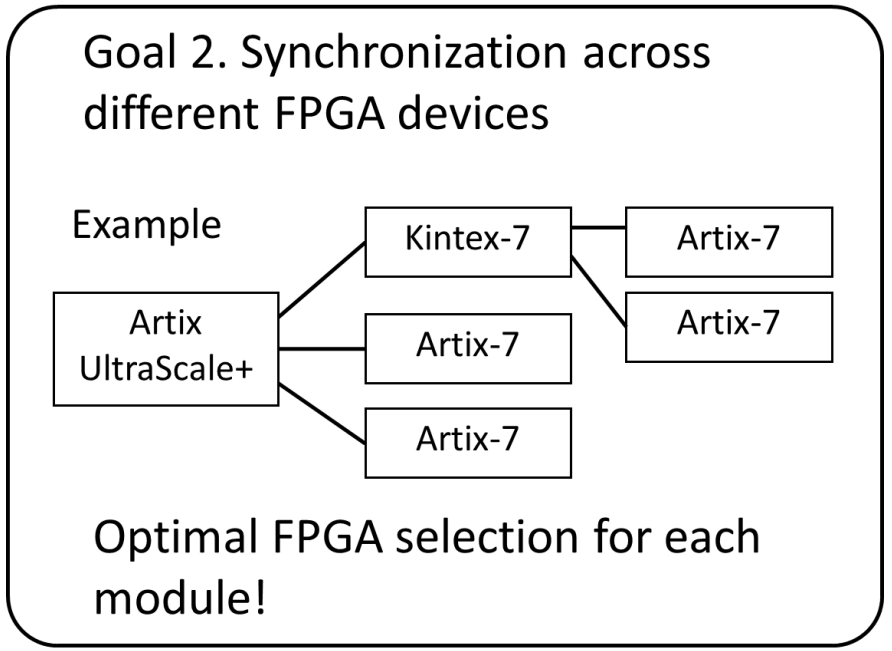
Extension of a wired time-synchronization protocol for sub-nanosecond accuracy to multiple FPGA families

#57

Features： Clock synchronization network over FPGA general I/Os
Sub-nanosecond time synchronization (~300 ps)
Limitation： AMD Kintex-7 only

Two extensions were implemented while maintaining 300 ps accuracy.





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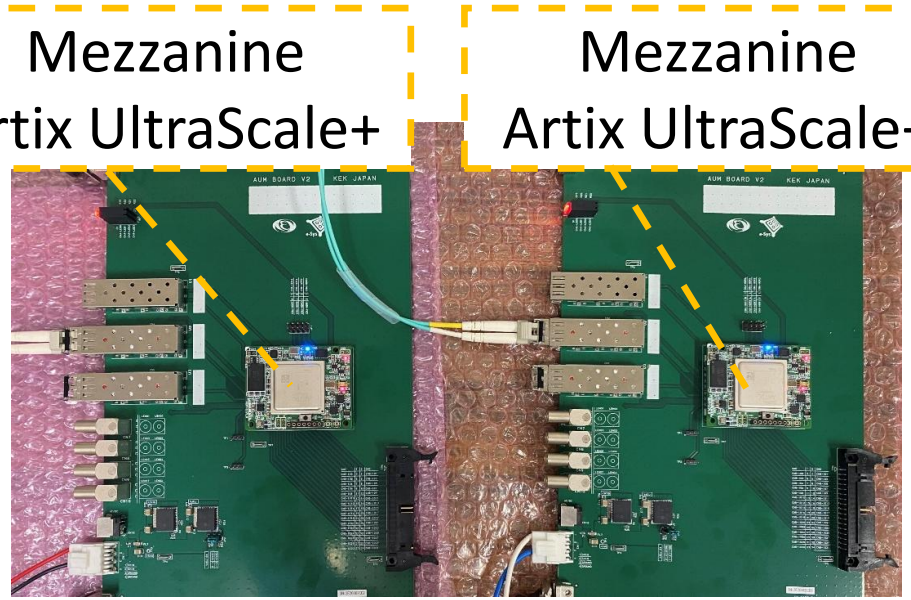
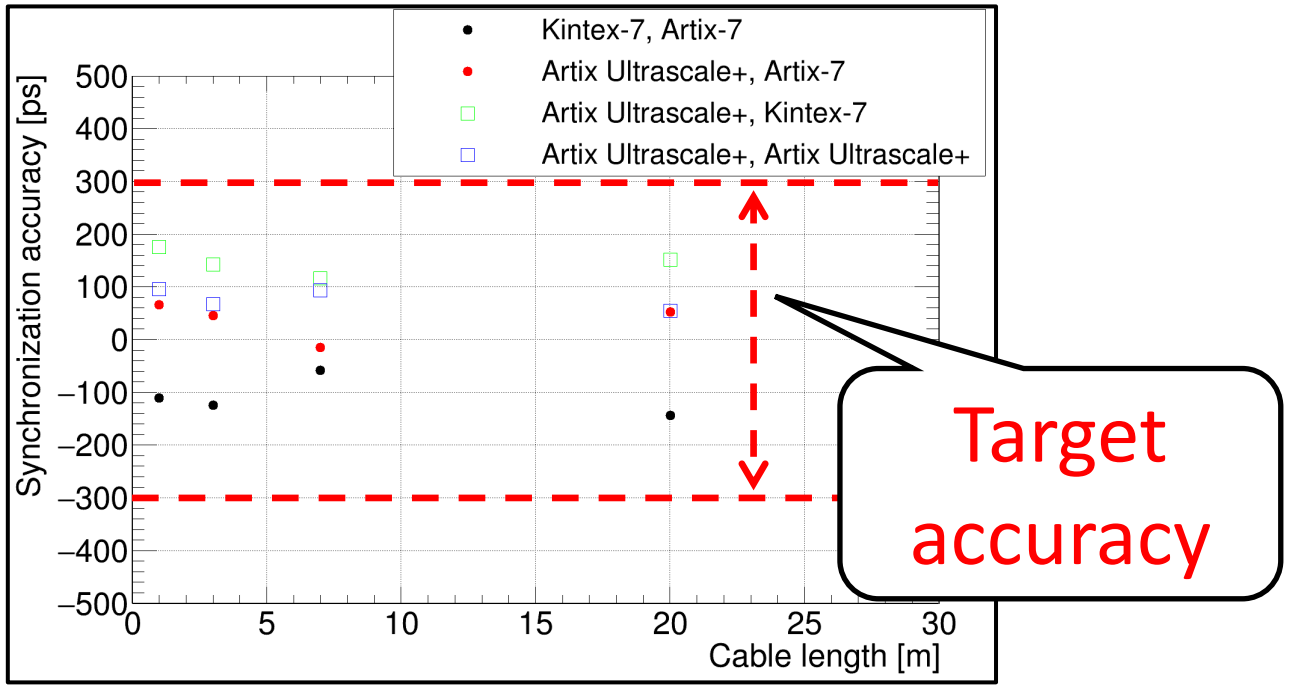
The system supports any FPGA combination
while maintaining the original 300 ps synchronization accuracy.



Example Test Setup



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