A 10-ps Resolution Direct-Digitizing Time Measurement ASIC for Fast Detectors

Zhuang Li, Junbo Zhao, Bingchen Mao, Jiajun Qin, Jiashu Yu, Xiaoyu Liao, Lei Zhao

***Abstract*—High-precision time measurement is one of the key techniques in the readout electronics for nuclear and particle physics experiments. To increase the integration level of time-of-flight (TOF) systems based on fast detectors such as multi-gap resistive plate chambers (MRPCs), and to suppress the signal reflections caused by impedance mismatch under large input signals, this paper presents an 8-channel front-end readout ASIC, with the pre-amplifier, the discriminator, and the time-to-digital converter (TDC) integrated into a single die. The pre-amplifier adopts a regulated common-gate (RGC) topology, which achieves wide bandwidth and low noise while maintaining a stable and low input impedance over a wide dynamic range. The discriminator employs a four-stage cascaded amplification structure, coping with the trade-off between bandwidth and gain. The TDC adopts a three-level hierarchical architecture that balances a large dynamic range and a fine bin-size, with the finest stage implemented as a Vernier delay line. The prototype was designed and fabricated in a 180-nm CMOS process, and test results show that the input impedance remains stable at 13 Ω to 16 Ω over a dynamic range of 100 fC to 2 pC, and that the full-chip timing precision reaches 10 ps, with the analog front-end and the TDC each contributing approximately 7 ps. The average per-channel power consumption is 45 mW, of which the analog front-end consumes 26 mW and the TDC consumes 19 mW.**

***Index Terms* — Readout electronics, Fast detectors, High-precision time measurement, Amplification and discrimination.**

I. Introduction

Time-of-Flight (TOF) measurement is a fundamental technique in high-energy physics experiments for particle identification. By precisely measuring the flight time of particles over a known path length and combining this information with momentum data from tracking detectors, the particle mass can be determined [1], [2]. In modern large-scale experiments such as the Compressed Baryonic Matter (CBM) experiment at FAIR [3] and the Cooler Storage Ring External-target Experiment (CEE) at HIAF [4], TOF detector systems are required to cover large areas with tens of thousands of readout channels while achieving a system-level time resolution on the order of tens of picoseconds [5].

To meet the stringent requirements on channel density and time resolution, various fast timing detectors have been developed and deployed in TOF systems, including Multi-gap Resistive Plate Chambers (MRPCs) [6], Micro-Channel Plate Photomultiplier Tubes (MCP-PMTs) [7], and diamonds [8]. Among these, MRPCs have been widely adopted as the detector of choice for large-area TOF systems due to their excellent intrinsic time resolution, relatively low cost, and ease of large-scale production [9], [10].

For high-precision time measurement, two main approaches are commonly adopted: waveform digitization and leading-edge discrimination followed by Time-to-Digital Conversion (TDC) [11]. Waveform digitization preserves the complete signal information and allows advanced offline timing extraction, but it relies on high-speed, high-resolution ADCs that consume significant power and area, limiting the channel density achievable in large-scale systems [12]. In contrast, the discriminator-plus-TDC approach digitizes only the signal arrival time, offering substantially lower power and higher integration density per channel, which makes it particularly attractive for TOF systems with a large number of channels [13].

Over the past two decades, several prominent readout ASICs have been developed for MRPC-based TOF systems. The NINO chip [14], designed at CERN, pioneered ultra-fast front-end processing for RPCs, achieving a time resolution below 25 ps. The PADI chip [15], developed for the CBM-TOF wall, further improved power efficiency and timing performance. However, both NINO and PADI are purely analog front-ends; they output timing pulses that must be digitized by a separate Time-to-Digital Converter (TDC), typically implemented in an FPGA or a dedicated Application-Specific Integrated Circuit (ASIC) like HPTDC or GET4 [16], [17], [18], [19]. This separation of the analog front-end and the digital quantization mandates complex inter-chip interconnections via PCB traces or cables, which not only introduces power consumption of interface circuits but also restricts the achievable channel density in space-constrained detectors.

Furthermore, a critical yet often underappreciated issue in conventional front-end designs is the stability of input impedance across a wide dynamic range. Most existing front-ends employ a Common-Gate (CG) input topology for its well-known low-impedance characteristics [20]. While the CG structure provides a nominally low input impedance, this impedance is inherently dependent on the transconductance of the input transistor, which varies significantly under large-signal conditions. When a large input charge drives the amplifying transistor out of its saturation region, the input impedance changes correspondingly, causing a severe mismatch with the

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The authors are with the Department of Modern Physics, University of Science and Technology of China, Hefei 230026, China (e-mail: zlei@ustc.edu.cn.)

detector's or transmission line's characteristic impedance. This mismatch results in signal reflections at the detector-electronics interface, leading to waveform distortion, degraded timing precision, and potential false triggering. For systems with a large dynamic range spanning more than one order of magnitude in charge, this impedance instability becomes a systematic error source that cannot be mitigated by simple threshold tuning.

To overcome these bottlenecks, this paper presents an 8-channel monolithic, direct-digitizing time measurement ASIC implemented in a 180-nm CMOS process. To address the impedance instability of conventional common-gate (CG) input stages under large signals, a Regulated Cascode (RGC) pre-amplifier is employed and optimized to maintain a stable and low input impedance across a wide dynamic range, thereby suppressing the signal reflections caused by impedance mismatch. To increase integration density, the complete signal processing chain, including the Analog Front-End (AFE) consisted of a Pre-Amplifier (PA) and a discriminator, and a high-precision three-stage TDC, is integrated onto a single silicon die, eliminating the dependence on external TDC chips. Within this monolithic framework, careful layout planning and dedicated power-ground isolation are further employed to suppress digital-to-analog crosstalk, ensuring the high timing precision of the full chip.

The paper is organized as follows. Section II provides the design of the ASIC, including the overview of the chip, the RGC pre-amplifier, the discriminator, and the hierarchical TDC. Section III presents the measurement results. Finally, Section IV concludes the paper.

II. ASIC DESIGN

A. The Architecture of the Chip

The proposed ASIC is designed as a monolithic, direct-digitizing time measurement solution dedicated to the readout of fast detectors such as MRPCs. The overall block diagram of the chip is illustrated in Fig. 1. The ASIC integrates eight independent time-measurement channels along with the necessary peripheral circuits, including a bandgap reference, a digital-to-analog converter (DAC) for threshold generation, a phase-locked loop (PLL) for system clock generation, a delay-locked loop (DLL) for multi-phase clock generation, and a global Gray-code counter for coarse time tagging.

Each channel comprises a complete signal-processing chain that converts the weak analog current pulse from the detector into a digitized time stamp. As shown in Fig. 1, the chain consists of three principal stages: a regulated cascode (RGC) pre-amplifier, a leading-edge discriminator, and two parallel hierarchical time-to-digital converters (TDCs), one for measuring the time of arrival (TOA) of the leading edge and the other for the time over threshold (TOT) by measuring the time of the trailing edge. In addition, some channels retain the TDC test signal input interface and discriminator output interface for measuring the time precision of the analog front end and TDC respectively.

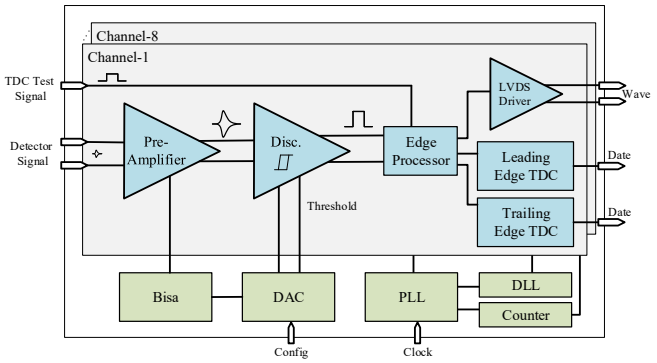


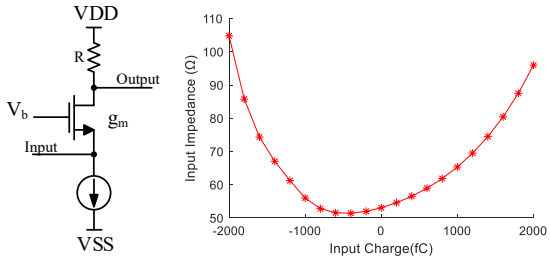
Fig. 1. Block diagram of the chip.

B. Pre-Amplifier

The pre-amplifier is the most critical circuit of the analog front-end, since it operates on the smallest signal in the entire chain. Any noise, interference, or impedance mismatch introduced at this stage is directly translated into timing jitter. For fast-detector readout, two design considerations dominate the pre-amplifier architecture: maintaining a stable and well-defined input impedance, and achieving a low timing jitter under the constraints of weak and fast signals.

The common-gate (CG) amplifier, shown in Fig. 2(a), has been widely adopted in MRPC readout ASICs such as NINO and PADI because of its inherently low input impedance, which is approximately $1/g_{m1}$, where g_{m1} is the transconductance of the input transistor MN1. By tuning the bias current of MN1, the input impedance can be set to match the characteristic impedance of the transmission line (typically 50 Ω).

However, the input impedance of the CG amplifier is fundamentally tied to the small-signal operating point of MN1, and it degrades substantially when a large input charge is injected. When a negative-polarity signal arrives, both the source and drain voltages of MN1 drop, pushing the transistor out of saturation and into the triode region; conversely, a positive-polarity signal raises both voltages, driving MN1 into the sub-threshold or even cut-off region. In either case, gm1 is reduced and the input impedance increases accordingly. Simulation shows that, with a static input impedance set to 50 Ω, the CG structure exhibits an input impedance close to 100 Ω under a 2-pC input charge.



(a)Circuit structure. (b)Simulation of input impedance.

Fig. 2. Structure and input impedance of CG circuit.

The impedance variation degrades the signal integrity of the MRPC readout chain. Since the detector strip, the interconnect cable, and the pre-amplifier input together form a transmission-

line system nominally matched to 50 Ω [21], [22], any deviation of the pre-amplifier input impedance under large-signal conditions produces reflections at the detector–electronics interface. The reflected waves superimpose on the incident waveform, distorting both its amplitude and its pulse width, the latter being particularly harmful as it is used for time-over-threshold (TOT) based time-walk correction. Although a portion of the reflection-induced events can be filtered out in offline processing, the residual distortion still degrades the overall timing performance. A pre-amplifier whose input impedance remains stable across the full dynamic range is therefore strongly desired.

To address the above issue, a regulated common-gate (RGC) [23] structure is proposed, as shown in Fig. 3. Conventionally, the RGC topology is employed in op-amp design to boost the output impedance of a cascode current source; in this work, however, its low-source-impedance property is exploited to realize a low and stable input impedance for the pre-amplifier.

The proposed circuit consists of four functional blocks. The CG amplifier (MN1 and RD1) provides the main signal amplification: the source of MN1 serves as the input node, the drain serves as the output node, and RD1 acts as the load. A common-source (CS) feedback loop (MN2 and RD2) senses the input voltage at MN1's source through MN2's gate, amplifies and inverts it, and feeds the result back to MN1's gate, thereby stabilizing the input-node voltage and lowering the input impedance. A PMOS current source (MP1) provides a tunable compensating current that allows the bias current of MN1 to be set flexibly without disturbing the static operating point. Finally, a clamping transistor MN4 limits the negative swing of the output node, preventing MN1 from entering deep triode region during large-signal injection.

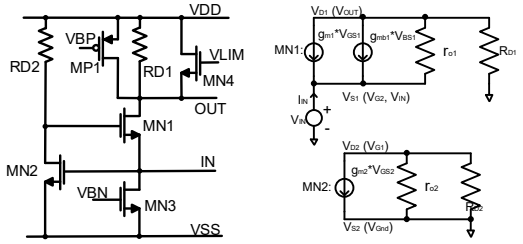


Fig. 3. (a)RGC PA circuit. (b)small-signal model.

A small-signal analysis is performed to quantify the input impedance. MN3 (the static tail current source) and MP1 (the static compensation current source) present high impedance and are neglected; MN4 is off under nominal operation and is also neglected. Writing KCL at the output node and the gate of MN1, and noting that the source of MN1 is shorted to the gate of MN2 and that the drain of MN2 is shorted to the gate of MN1, the small-signal input impedance can be derived as

$$R_{in} = \frac{1}{g_{m1}(1 + g_{m2}R_{D2})} \tag{1}$$

Compared with the conventional CG structure whose input impedance is $1/g_{m1}$, the proposed RGC structure reduces R_{in} by a factor of $(1+g_{m2}R_{D2})$, bringing benefits under large-signal conditions. First, the negative feedback actively regulates the input-node voltage, so MN1 remains in saturation across a larger dynamic range. Second, even if MN1 is momentarily driven into the triode region by an extreme signal, the resulting reduction in g_{m1} is divided by $(1+g_{m2}R_{D2})$, which strongly attenuates its impact on R_{in}. Simulation indicates that the proposed RGC pre-amplifier maintains an input impedance variation of less than 5 Ω under a 2-pC charge injection, much better than the performance of CG circuits.

We now turn to the second design consideration—low timing jitter. For a leading-edge discriminator, the timing jitter σ_t is determined by the slew rate (SR) of the signal at the threshold crossing and by the noise voltage [24]:

$$\sigma_t = \frac{V_{n,out}}{SR} = \frac{V_{n,out} \times t_r}{V_{out}} \tag{2}$$

where $V_{n,out}$ is the rms output-referred noise voltage at the discriminator input, t_r is the rise time of the pre-amplifier output, and V_{out} is the output amplitude. As shown in Equation (3) and (4), the t_r is related to the pre-amplifier bandwidth BW and the detector signal duration t_{det}, and the $V_{n,out}$ is related to the noise spectral density e_n and bandwidth.

$$t_r \approx \sqrt{t_{det}^2 + \left(\frac{0.35}{BW}\right)^2} \tag{3}$$

$$V_{n,out} \approx e_n\sqrt{BW} \tag{4}$$

Equation (5) can be derived from equation (2-4), which reveals that minimizing jitter requires both appropriate bandwidth and extremely small noise—the two figures of merit that must be jointly optimized.

$$\sigma_t \propto e_n \times \sqrt{\left(\frac{t_{det}}{0.35}\right)^2 \times BW + \frac{1}{BW}} \tag{5}$$

The signal of common fast detectors such as MRPC has an intrinsic rise time of roughly 0.5 ns ~ 1 ns, corresponding to a frequency content of approximately 350 MHz ~ 700 MHz. If the pre-amplifier bandwidth is significantly lower than this value, the output edge is slowed down and the slew rate suffers; on the other hand, a bandwidth substantially higher does not improve t_r further, which is now limited by t_{det}, but unnecessarily integrates additional wideband noise, degrading the noise performance of the chain.

To guide device sizing, the noise contribution of each transistor and resistor in the proposed RGC structure is analyzed. The dominant noise sources are the thermal noise of MN1, MN2, MN3, RD1, and RD2. The flicker (1/f) noise is negligible at the frequencies of interest (>100 MHz). The current-noise spectral densities of the MOSFETs and resistors are

$$\overline{i_{n,MNk}^2} = 4kT\gamma g_{m,k} \tag{6}$$

$$\overline{i_{n,R_{Dk}}^2} = \frac{4kT}{R_{Dk}} \tag{7}$$

where k is Boltzmann's constant, T is the absolute temperature, and $\gamma \approx 2/3$ for long-channel devices.

Referring each noise source to the output node and then back to the input, the input-referred noise voltage spectral density of the proposed RGC pre-amplifier can be derived as

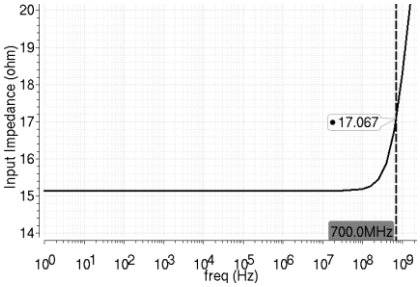
$$\overline{i_{n,in}^2} = 4\mathrm{kT}\gamma g_{m1} + 4\mathrm{kT}\gamma g_{m3} + \frac{4kT}{R_{D1}} + \frac{4\mathrm{kT}\gamma}{g_{m2}} g_{m1}^2 (1 + g_{m2}R_{D2})^2 + \frac{4kT\gamma g_{m1}^2}{g_{m2}^2 R_{D2}} (1 + g_{m2}R_{D2})^2 \quad (8)$$

Equation (8) reveals the optimization directions of the circuit:

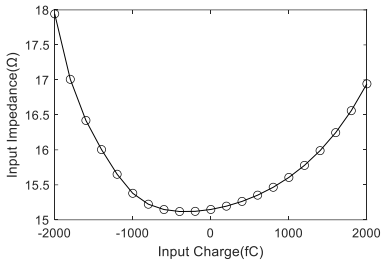
1. The noise contribution of the feedback branch (MN2 and RD2) is higher than that of the amplification branch by a factor of the loop gain ($1+g_{m2}\cdot R_{D2}$), which is exactly the factor by which the input impedance is reduced. This indicates that the reduction of the input impedance does not come for free, but is obtained at the cost of degraded noise performance. Accordingly, under the constraint of satisfying the large-signal impedance-matching requirement, the loop gain of the feedback branch should be kept as low as possible.

2. Reducing the transconductances (g_{m1}, g_{m2}, and g_{m3}) and increasing the load resistances (R_{D1} and R_{D2}) are favorable for noise suppression, but these two parameters cannot be optimized without limit, as their bottlenecks lie in the bandwidth and the voltage margin. For the load resistance, a larger value lowers the pole frequency at the corresponding node and increases the voltage drop under the same bias current, thereby reducing the bandwidth and the voltage margin. For the transconductance of the amplification transistor, its value is tied to the load resistance through the circuit gain $g_m \cdot R_D$, so reducing the transconductance and increasing the load resistance are essentially the same action. For the transconductance of the tail current source, it has to be reduced by increasing the overdrive voltage under a fixed bias current. Based on the above considerations, the adopted optimization strategy is to employ a 3.3-V supply for a larger voltage margin, instead of the 1.8-V core supply commonly used in 180-nm CMOS, and to reduce the transconductances and increase the load resistances as much as possible under the bandwidth constraint discussed above.

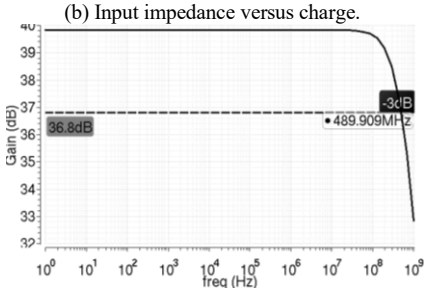
Following the above guidelines, the device parameters of the pre-amplifier have been optimized and the post-simulation results are as follows.



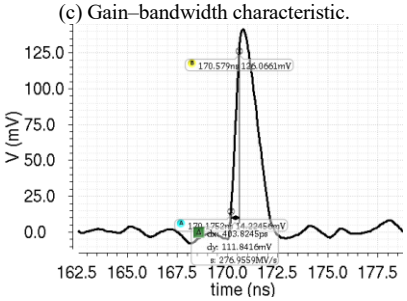
(a) Input impedance versus frequency.



(b) Input impedance versus charge.



(c) Gain–bandwidth characteristic.



(d) Transient waveform at 100 fC input charge.

Fig. 4. Simulation results of PA.

The gain of the feedback loop is designed to be 9.5 dB, reducing the input impedance of the preamplifier by approximately a factor of 3. The input impedance remains stable around 15 Ω within a 700-MHz bandwidth and a 2-pC signal range.

The bandwidth is 490 MHz, which meets the discussion indicators mentioned above. It is worth mentioning that although the RGC structure introduces noise, its low input impedance makes it easier to achieve a larger bandwidth, so the overall time jitter does not increase significantly even with the additional noise from RD2 and MN2.

Transient noise simulations show that, with an input signal charge of 100 fC, the RMS noise at the pre-amplifier output baseline is 1.91 mV, and the slew rate at the rising edge of the output signal is 277 MV/ns. The corresponding timing jitter introduced by the pre-amplifier can therefore be calculated as 6.9 ps, showing that the proposed RGC pre-amplifier achieves an improved input-impedance stability without notable degradation in timing performance compared with the conventional CG topology.

C. Discriminator

The discriminator converts the amplified analog waveform from the pre-amplifier into a digital pulse whose leading and trailing edges carry the TOA and TOT information. Two design issues must be carefully addressed: the discriminator should provide sufficient gain to amplify the smallest signal of interest

to a full-swing CMOS level, so that the downstream TDC can correctly capture the edges; meanwhile, the propagation delay and the additional jitter introduced by the discriminator itself should be minimized.

A single-stage discriminator can hardly satisfy both requirements simultaneously due to the fundamental gain-bandwidth trade-off. To address this, a four-stage cascaded fully-differential amplifier topology is adopted in this work, as shown in Fig. 5(a). Each stage provides a moderate gain (~10 dB) together with a wide bandwidth (>1 GHz), and the cascade of four stages delivers an overall gain in excess of 40 dB, sufficient to drive even the smallest input signal of interest (corresponding to ~50 fC input charge) into saturation. The use of fully differential signaling throughout the discriminator chain effectively rejects common-mode disturbances coupled from the supply rails and the substrate.

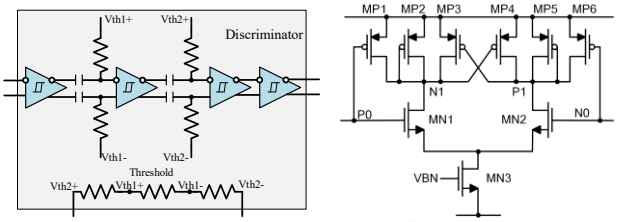


Fig. 5. (a)Discriminator structure. (b)Amplifier in Discriminator.

The single-stage amplifier structure is shown in Fig. 5(b). It employs a differential complementary common source structure as the main amplifying core, combined with a cross-coupled positive-feedback pair at the output nodes to introduce a controlled amount of hysteresis. The hysteresis serves two purposes: (i) it suppresses spurious transitions caused by noise when the input signal crosses the threshold slowly, thereby avoiding double-triggering; and (ii) it sharpens the output edge transition once the threshold is crossed, reducing the effective rise/fall time at the stage output and consequently lowering the time-walk and jitter contributions of the subsequent stages.

A practical issue arising from the cascaded structure is the accumulation of DC offset. The input-referred offset of each stage, although small individually (a few mV due to device mismatch), is amplified by all subsequent stages, and the accumulated offset at the output can easily saturate the later stages or cause significantly different equivalent thresholds under the same nominal threshold setting. To eliminate this effect, AC coupling networks are inserted between adjacent stages, as illustrated in Fig. 5(a). The coupling capacitors block the DC component while passing the signal band of interest, so that each stage operates at its own well-defined DC operating point, independent of the offsets accumulated from preceding stages.

The values of the coupling capacitors and the biasing resistors are jointly determined by the desired high-pass corner frequency $f_{HP} = 1 / (2\pi RC)$. On the lower end, f_{HP} must be sufficiently below the lowest significant frequency component of the MRPC signal spectrum (which extends from a few MHz to several hundred MHz given the sub-nanosecond rise time) to avoid distorting the leading and trailing edges that carry the timing information. On the upper end, the resistance cannot be made arbitrarily large because it also sets the input common-mode voltage of the following stage through the biasing path, and excessively large resistance would slow down the recovery from large signal excursions, thereby limiting the maximum count rate. In this design, the capacitance is chosen as 1 pF and the resistance as 20 kΩ, yielding a high-pass corner of approximately 8 MHz, which is well below the MRPC signal band while keeping the recovery time within acceptable limits.

The threshold of the discriminator is set by a programmable DC voltage generated by an on-chip DAC, which is injected into the DC bias nodes of the second-stage and third-stage amplifiers via the AC-coupling biasing resistors. By adjusting this threshold voltage, the trigger level can be flexibly adapted to accommodate different detector signal amplitudes and noise environments.

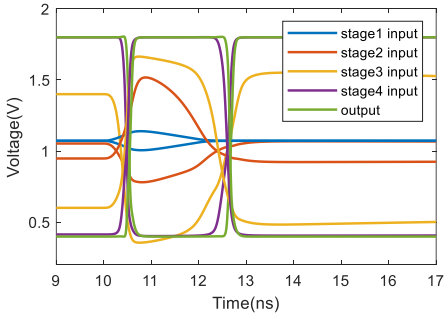


Fig. 6. Waveforms at each stage in the discriminator.

Fig. 6 shows the transient waveforms at the input and output of each discriminator stage under a 100-fC input charge. The differential signal is amplified progressively through the cascade. At the input of the second and third stages, the DC threshold voltage injected by the on-chip DAC offsets the baseline of the positive and negative branches, creating the effective discrimination threshold. By the end of the third stage, the signal has been driven into full-swing saturation. The fourth stage provides additional gain margin and sharpens the rising and falling edges, ensuring well-defined logic-level transitions for subsequent TDC digitization.

D. Three-Stage TDC

The TDC is responsible for converting the leading and trailing edges of the discriminator output into digital time codes. In this work, a three-stage hierarchical architecture is adopted to achieve a fine timing bin together with a wide measurement range and a manageable power consumption. This TDC has already been implemented and verified in a standalone chip, and the detailed circuit design can be found in [25].

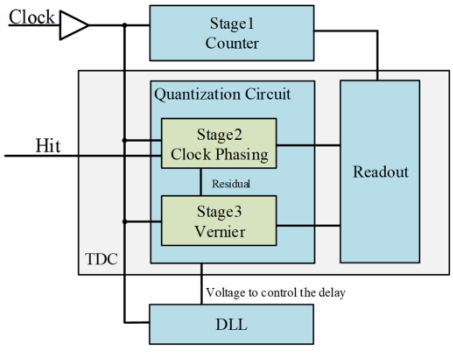


Fig. 7. Structure of TDC.

The overall block diagram of the TDC is shown in Fig. 7. The first stage is a coarse counter shared by all channels and clocked by the system reference clock. It provides a large dynamic range and outputs an overflow carry signal that can be used for further dynamic-range extension, so as to cover the full inter-event interval of the detector. The counter is implemented in Gray code with an additional parity bit to avoid metastability when the asynchronous edge from the discriminator latches the counter value.

The second stage is a DLL-based multi-phase clock interpolator. A DLL shared by all TDC channels locks the total delay of a delay-cell chain to one system clock period, and thereby generates the control voltage that sets the delay of each individual delay cell. Based on this control voltage, each TDC channel produces a set of equally spaced clock phases, identifies the two adjacent phases that bracket the discriminator edge to obtain the corresponding time code, and passes the residue to the third stage.

The third stage is a Vernier TDC. Two separate DLLs in the peripheral circuitry produces the control voltages corresponding to two slightly different delay values. Using these control voltages, each TDC channel generates signals propagating along two delay chains with different per-cell delays, forming a Vernier TDC. Its bin size is determined by the difference between the two per-cell delays and is about 6 ps. The combination of the three hierarchical stages allows the TDC to cover a wide measurement range with a fine timing bin without resorting to an excessively long delay line, keeping the overall power and area cost at a moderate level.

Two such TDC channels are implemented in parallel within each readout channel, one dedicated to the leading edge for TOA measurement and the other to the trailing edge for TOT measurement.

E. Full-chip Layout

The proposed readout ASIC is fabricated in a 180-nm CMOS process. The chip layout is shown in Fig. 8, with the major functional blocks highlighted. The die occupies a total area of 2550 × 3350 μm² and integrates eight readout channels together with the shared peripheral circuitry, which consists of the PLL, the DLLs, the bias circuits, and the coarse counter.

Within each channel, the analog front end is placed along the left side of the chip so as to minimize the routing length from the input pads to the pre-amplifier inputs, thereby reducing the parasitic inductance and capacitance at the input node. The TDC and the digital readout logic are placed on the right side of the channel, physically separated from the analog front end to suppress the coupling of digital switching noise into the analog circuitry.

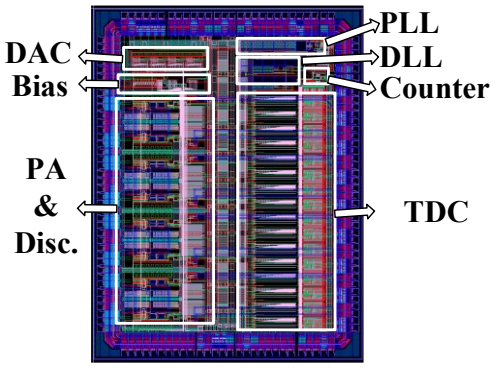


Fig. 8. Layout of the chip.

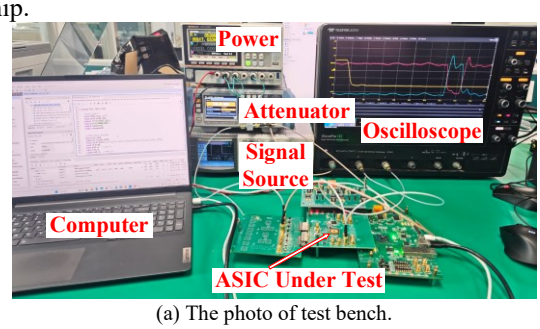
In a mixed-signal chip design, an appropriate partitioning of the power supply network is essential to suppress crosstalk between analog and digital. In this work, the on-chip supply network is divided into four independent power domains: the analog 3.3-V domain, the analog 1.8-V domain, the TDC domain, and the digital domain. Each power domain is provided with its own bonding pads, on-chip decoupling capacitors, and a dedicated ground return, so as to minimize the cross-domain interference between the different supplies.

III. TEST RESULTS

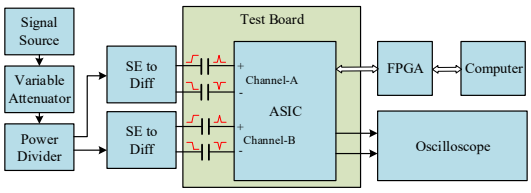
To evaluate the performance of the proposed readout ASIC, a series of systematic test were carried out on the prototype chip. Since the chip is intended for the direct readout of fast timing detectors such as MRPCs, three key performance metrics are of primary concern: timing precision, input impedance, and power consumption.

A. Time Precision Test

The time performance test platform is set up following the scheme illustrated in Fig. 9. A signal generator produces a step pulse with a rise time of 1 ns, which is then processed sequentially by an attenuator, a power divider, delay lines, and single-ended to differential converters, yielding two pairs of differential step signals. The differential step is subsequently converted into a differential charge signal through a series differentiating capacitor, with the injected charge being equal to the differential voltage of the step signal multiplied by the value of the differentiating capacitor, that is, $Q = V_{diff} \times C$. After being amplified and discriminated by the chip, the injected signal can either be observed directly with an oscilloscope from the discriminator output to evaluate the timing precision of the analog front end, or be read out through an FPGA after being digitized by the TDC to evaluate the overall timing precision of the chip.



(a) The photo of test bench.



(b) Test system structure diagram.

Fig. 9. Time precision test setup.

To characterize the AFE performance, the discriminator outputs of channel 2 and channel 4 were connected to a oscilloscope. Assuming that all channels exhibit comparable timing precision, the standard deviation of the measured time difference between the two channels was divided by $\sqrt{2}$ to obtain the single-channel timing jitter. The measured result is presented in Fig. 10, showing that the single-channel jitter is better than 7.5 ps.

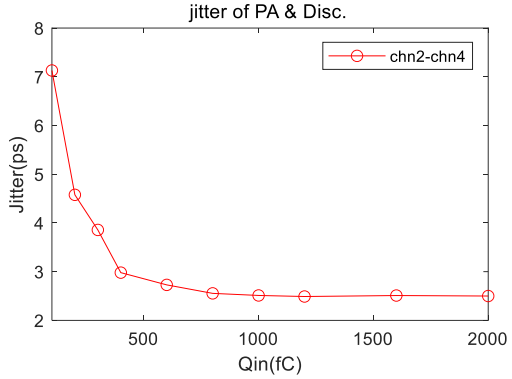


Fig. 10. AFE jitter test.

To independently evaluate the timing precision of the on-chip TDC, a delay-line scan method is adopted. In the test, two strictly synchronous pulse signals are generated by a high-precision signal source and injected into two channels of the TDC. The relative delay between the two signals is finely tuned to scan over the effective measurement range of the TDC. At each delay setting, the time measurements from the two TDC channels are recorded, and the difference between them is calculated. The single-channel timing precision of the TDC can be obtained by taking the standard deviation of the difference and dividing it by $\sqrt{2}$. The measurement results show that the single-channel timing precision of the TDC is better than 7 ps

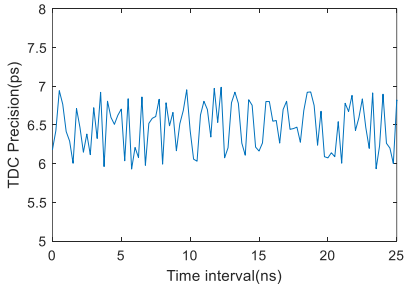


Fig. 11. TDC precision test.

The overall timing precision of the chip, including the contributions from both the analog front end and the TDC, is shown in Fig. 12. Over the input charge range from 100 fC to 2 pC, the overall timing precision remains better than 10 ps.

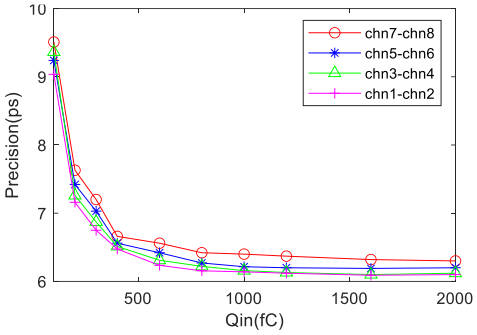


Fig. 12. Full-chip precision test result.

B. *Input Impedance Test*

The input impedance of the pre-amplifier strongly depends on the spectral content and the amplitude of the input signal. In order to characterize the actual input impedance seen by the fast detector signals of interest, the measurement setup shown in Fig. 13 is adopted.

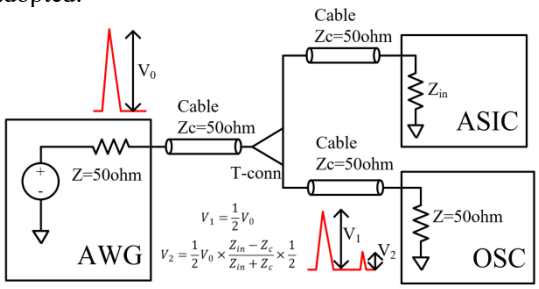


Fig. 13. Input impedance test setup.

The signal generator produces a test waveform whose shape is representative of the detector's output; in this work, a triangular pulse with both rising and falling edges of 0.5 ns is used. After passing through a T-junction, the signal is split into two paths: one is fed into the on-chip pre-amplifier, and the other is sent directly to the oscilloscope as a reference of the incident waveform. When the pre-amplifier input impedance is not matched to the characteristic impedance of the transmission line, the signal is partially reflected at the pre-amplifier input, and the reflected waveform travels back through the tee junction to the oscilloscope. As a result, both the incident and the reflected waveforms can be observed on the oscilloscope, and their amplitudes satisfy:

$$V_2 = V_1 \times \frac{Z_{in} - Z_c}{Z_{in} + Z_c} \times \frac{1}{2} \tag{9}$$

Where V_1, and V_2 represent the amplitude of the two signals received by the oscilloscope, respectively. Z_{in} is the characteristic impedance of pre-amplifier input, and Z_c is the characteristic impedance of the transmission line (50 Ω in this measurement). By measuring the peak ratio between the incident and the reflected waveforms, the pre-amplifier input impedance can be extracted.

The measured results are shown in Fig. 14. Over a dynamic range of 2 pC and for both positive and negative input polarities, the input impedance remains stable at around 14 Ω, with a fluctuation not exceed 1.5 Ω.

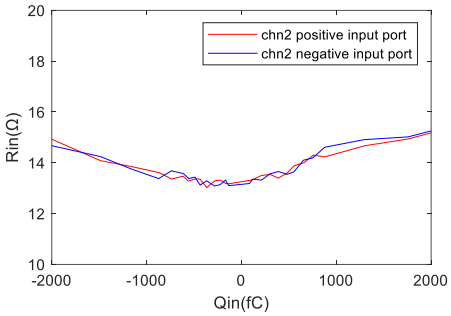


Fig. 14. Input impedance test result.

C. Power Consumption

The power consumption of the chip is measured by inserting a 0.1-Ω resistor in series with the supply line and measuring the voltage drop across it. The static power consumption of the entire chip, with no hit events, is 360 mW, in which the analog front-end accounts for 210 mW and the TDC together with the digital logic accounts for 150 mW. When the per-channel hit rate is 1 MHz, the total power consumption increases by 15 mW, corresponding to an average dynamic power of 15 mW/MHz/channel.

D. Summary of test results

The test results this work are summarized in Table. 1.

Parameters	Value
Process	180 nm
Area	2550 × 3350 μm²
AFE Jitter	<7.5 ps
TDC Precision	<7 ps
Full-chip Precision	<10 ps
Input Impedance	13 Ω – 16 Ω
AFE Power	26 mW/channel
TDC Power	19 mW/channel
Dynamic Power	15 mW/MHz/channel

Table. 1. Summary of parameters.

IV. Conclusion

This paper has presented a fully integrated 8-channel front-end readout ASIC for fast timing detectors. The chip, implemented in a 180-nm CMOS process, integrates a low-input-impedance analog front end and an on-chip TDC on a single die. The pre-amplifier employs a regulated common-gate (RGC) input topology, which provides a low and stable input impedance over a wide input charge range. Together with the high-precision discriminator and the TDC, the chip achieves high-precision direct digitization readout for fast detectors within a single die.

Test results show that the chip achieves a timing precision better than 10 ps over the input charge range from 100 fC to 2 pC, an input impedance stable at approximately 14 Ω over a 2-pC dynamic range for both positive and negative signal polarities, a static power consumption of 360 mW and a dynamic power of 15 mW/MHz/channel.

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