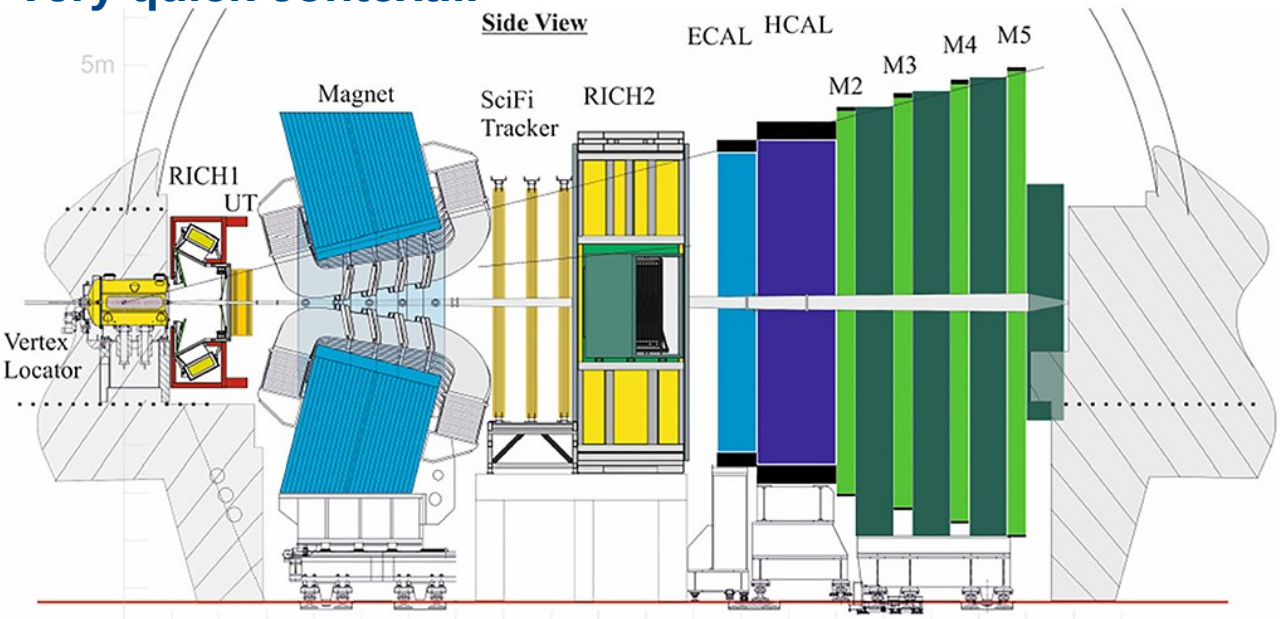
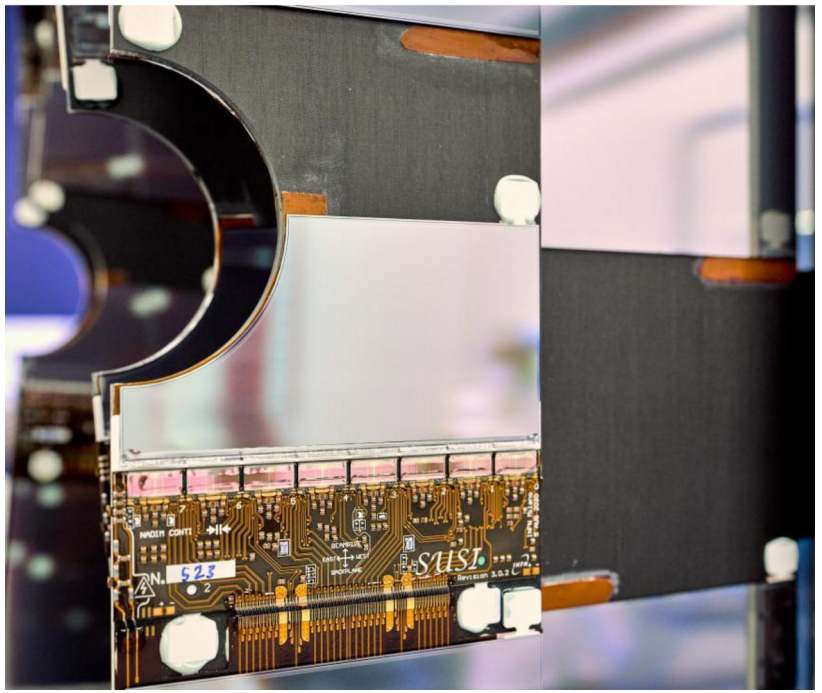
Data Processing Firmware of the Upstream Tracker for LHCb Run 3

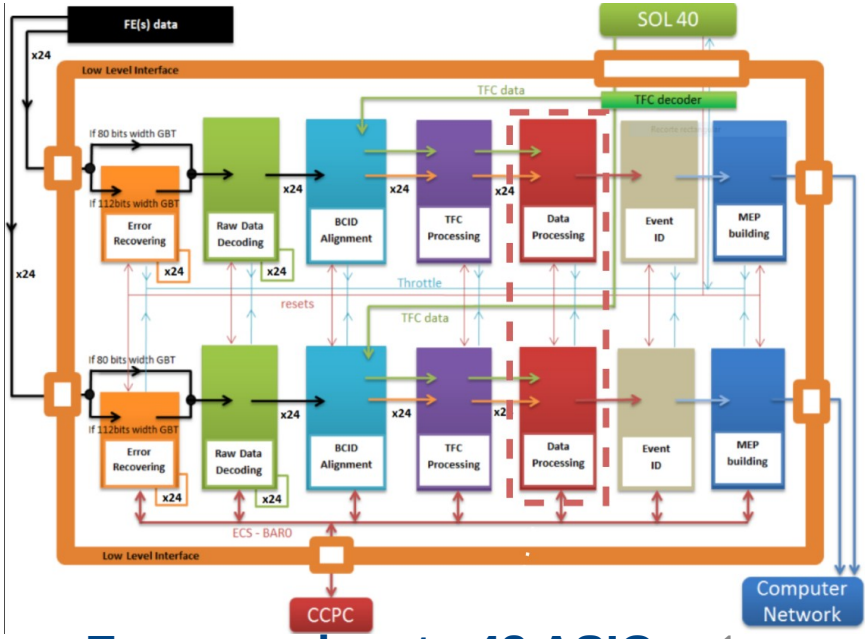
Very quick context...





Packet name	Header (12-bit) BXID 4 bits	Parity 1 bit	Flag 1 bit	Length 6 bit	Data n·12 bits	Comment
Idle	0000	1	1	'b11_0000	—	no enough data
BxVeto	*bxid_cnt[3:0]*	*	1	'b01_0001	—	BxVeto in TFCcmd
HeaderOnly	*bxid_cnt[3:0]*	*	1	'b01_0010	—	HeaderOnly in TFCcmd
BusyEvent	*bxid_cnt[3:0]*	*	1	'b01_0011	—	*nHits*> 63
BufferFull	*bxid_cnt[3:0]*	*	1	'b01_0100	—	no space in memory
BufferFullN	*bxid_cnt[3:0]*	*	1	'b01_0101	—	no space in memory
NZS	*bxid_cnt[3:0]*	*	1	'b00_0110	Values	NZS in TFCcmd
Normal	*bxid_cnt[3:0]*	*	0	*nHits*	Hits	Normal event
Sync	*bxid_cnt[11:0]*				*sync_pattern*	Synch in TFCcmd

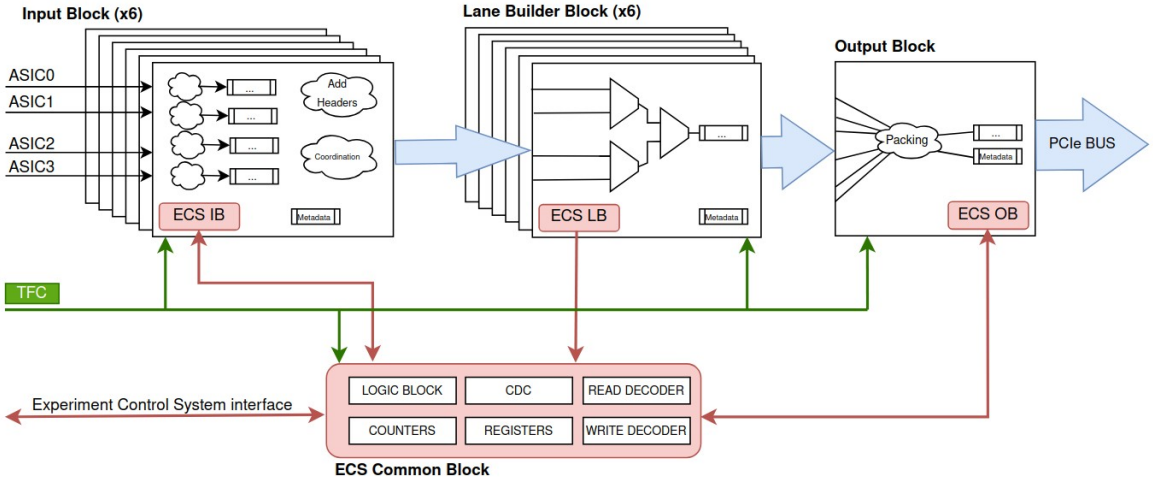
GBT frame byte	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4 x 3-eports			24-bit			24-bit			24-bit			24-bit		
2 x 3-eports			24-bit					24-bit						
2 x 4-eports			32-bit					32-bit						
2 x 5-eports			40-bit					40-bit						

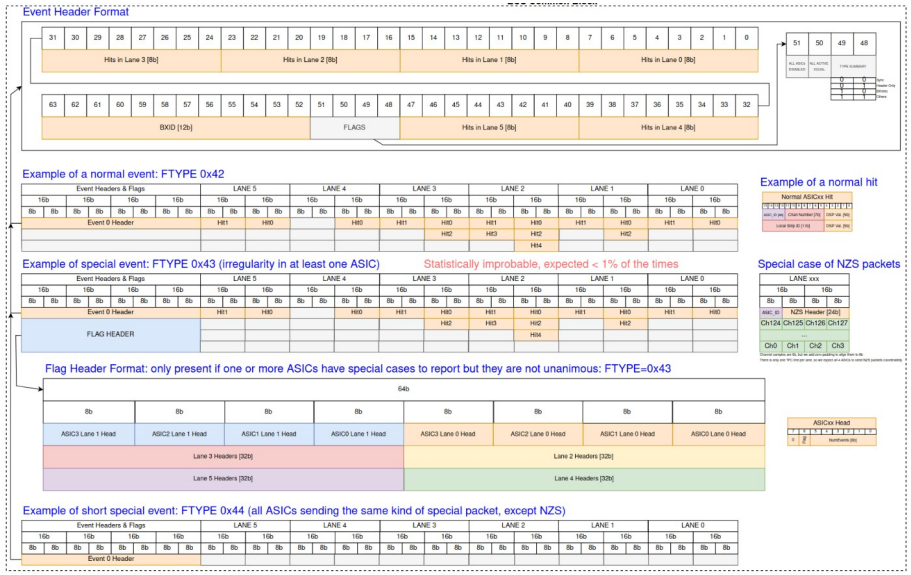


Every card up to 48 ASICs

Data Processing Firmware of the Upstream Tracker for LHCb Run 3

Architecture overview

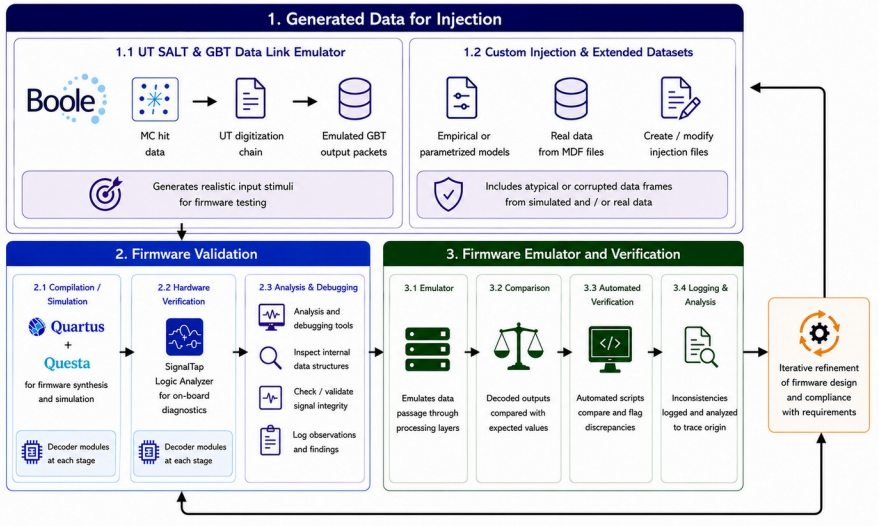




Simple, adapts to all cases, scalable, easy to implement, small ALM footprint, performant...

Output data format: simple, 8b aligned, easy to implement, include all cases, have reasonable BW efficiency

A lot of effort to simulate, verify, debug, CI, ...



Lessons learned: control software, debugging features, important things to consider for FPGA implementation, And many others!