FPGA based RDMA for BEE Readout

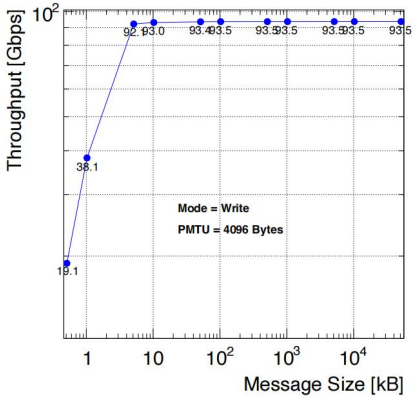
Chang Xu, Institute of High Energy Physics

Research Objectives

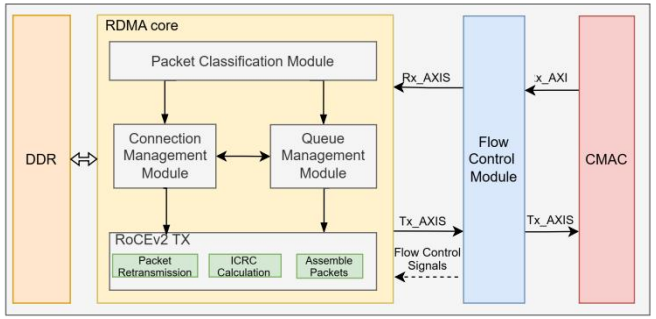
- Use RDMA instead of traditional protocols for BEE-to-DAQ data transmission, improving efficiency and reducing computing resource usage
- Support connection establishment and full RoCEv2 functions (Write, Send, Receive, Read)

Project Progress

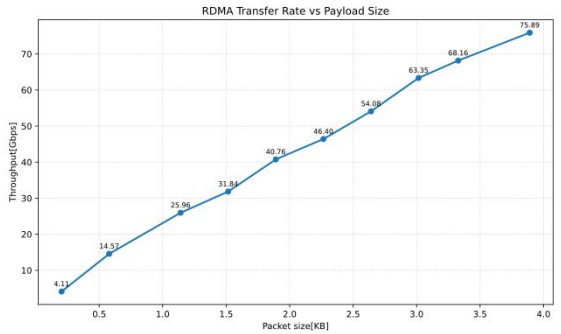
- **Software Implementation**
  - FPGA-PC data transmission test completed
- **Customized Firmware Implementation**
  - Peak throughput reaches about **75.9 Gbps**
- **100G ROCEv2 Transmission**
  - Developed Based on Open-source Project
  - Throughput reaches **~92 Gbps** for packets larger than **5 KB**
  - Single-packet latency is ~730 cycles, about **2.27 µs**



Throughput Test for 100G ROCEv2 Transmission



Network Stack Design



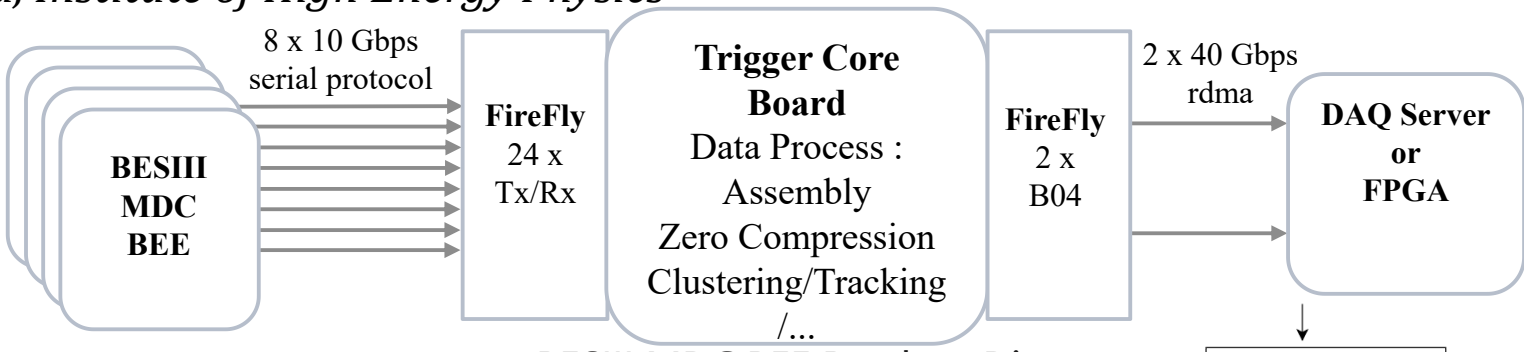
Throughput Test Result for Customized Network Stack

FPGA based RDMA for BEE Readout

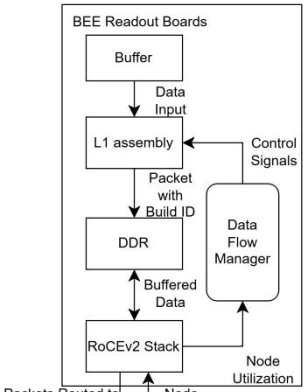
Chang Xu, Institute of High Energy Physics

- **Future Application**
  - **BESIII BEE Readout**
  - **BEE Readout System for CEPC**

No. 134



BESIII MDC BEE Readout Diagram



CEPC BEE Readout Module

- **Other BESIII-related Work**
  - Poster No.192 by Haoxin Wang: *Design of a Full Trigger Data Readout Scheme for the BESIII MDC Sub-trigger System*
  - Poster No.143 by Xin Cao: *The upgrade of the BESIII trigger fast control system*