Benchmarking Streaming Readout Performance of CAEN Digitizer 2.0 Family

Giovanni Cerretani, Matteo Bianchini, Alberto Potenza, and Carlo Tintori

***Abstract*—The CAEN x2740/x2745, x2730, and x2751 digitizers belong to the Digitizer 2.0 family and are designed to meet the high data-rate requirements of modern nuclear and particle-physics experiments, medical-imaging systems, and large-scale detector readouts. These platforms support both triggered acquisition and continuous streaming readout, integrating high-speed Flash ADCs, FPGA-based real-time processing, large DDR4 buffers, and native USB 3.1, 1 GbE TCP, and 10 GbE UDP connectivity. This work provides a performance evaluation of streaming readout (SRO) architectures. Hardware benchmarks were performed using triggered and streaming readout firmware in order to investigate saturation behavior and identify throughput limitations. In triggered readout with raw-waveform transmission over 10 GbE UDP, data rates close to 1.1 GB/s were achieved with no packet loss. In list-mode streaming readout with onboard processing, the maximum event rate is limited by the internal FPGA event-sorting algorithm rather than by network bandwidth. Software benchmarks using the CAEN FELib library and the CoMPASS DAQ software highlight additional decoding and processing bottlenecks. The results identify clear directions for future improvements in FPGA-level event handling and host-side parallelization.**

***Index Terms*—Data acquisition, digitizers, FPGA, streaming readout, 10 GbE, UDP, nuclear instrumentation.**

I. Introduction

THE CAEN x2740/x2745, x2730, and x2751 digitizers [1] belong to the latest Digitizer 2.0 family and are designed to meet the performance requirements of modern data-acquisition (DAQ) systems for nuclear and particle physics, medical imaging, and other high-rate detector applications. The x2740/x2745 models primarily target applications where high energy resolution is required, such as systems based on photomultiplier tubes (PMTs), silicon detectors, or high-purity germanium (HPGe) detectors. The x2730 and x2751 are instead designed for fast signal acquisition, providing higher sampling rates and enhanced timing performance, and are therefore well suited to applications requiring precise time measurements and accurate reconstruction of fast signal shapes. An overview of the Digitizer 2.0 product family is shown in Fig. 1.

These platforms share a common modular architecture based on high-speed Flash ADCs, FPGA-based real-time signal processing, large DDR4 memory buffers, and an embedded ARM processor for system management and slow control.

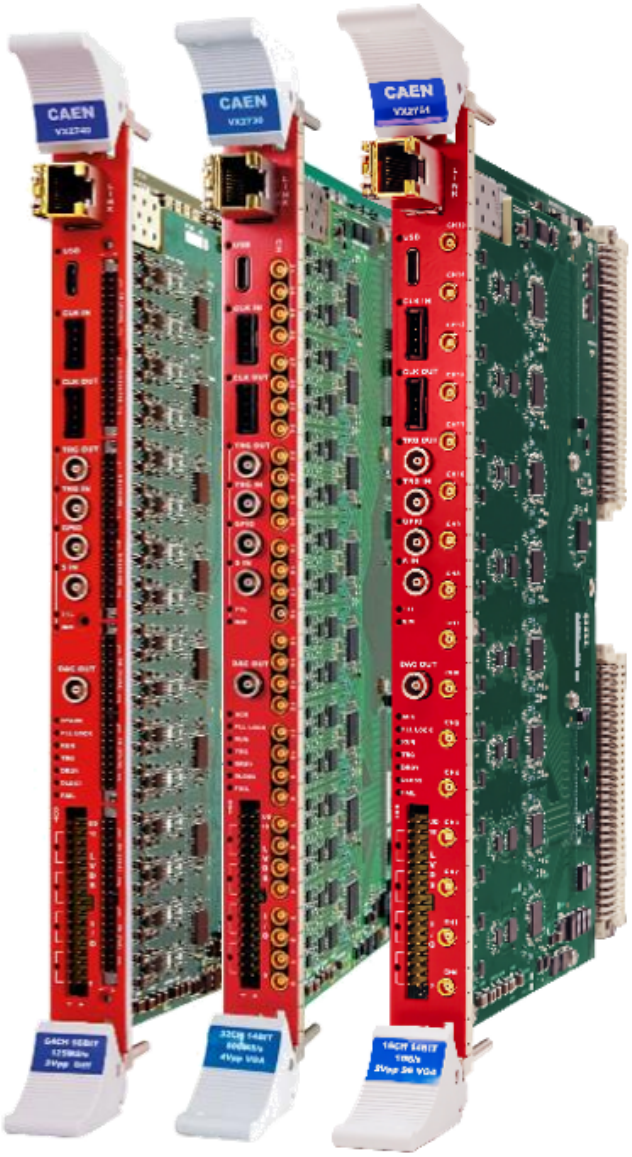

Fig. 1. Overview of the CAEN Digitizer 2.0 family.

All models support both traditional triggered readout and streaming readout paradigms, and provide native high-speed connectivity via USB 3.1, 1 GbE TCP, and 10 GbE UDP interfaces. Fig. 2 illustrates the common internal architecture shared across the different models.

The growing adoption of streaming readout in large detector systems motivates a systematic characterization of where, in

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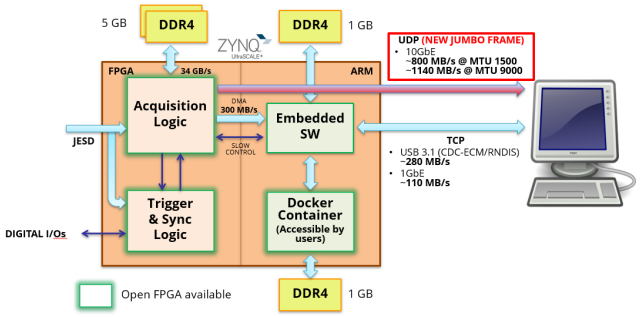

Fig. 2. Sketch of the Digitizer 2.0 internal architecture, from the ADC stage to the high-speed network link. Data digitized by the Flash ADCs are processed in real time by the FPGA and buffered in DDR4 memory; depending on the selected interface they are routed either through the embedded ARM processor (USB 3.1, 1 GbE TCP) or streamed directly from the FPGA to the host (10 GbE UDP).

practice, the achievable throughput is limited. The contribution of this work is twofold: *(i)* a quantitative, end-to-end benchmark of the Digitizer 2.0 data path, from the ADC front end to the host application, in both triggered and streaming modes; and *(ii)* the identification of the dominant bottleneck in each operating regime, separating network-bandwidth limits from FPGA-internal and host-software limits. The remainder of the paper is organized as follows. Section II describes the streaming readout architecture and the network optimizations applied. Section III details the measurement setup and methodology. Section IV presents the hardware and software benchmark results. Section V discusses the implications, and Section VI concludes.

II. Streaming Readout Architecture and Network Optimization

The increasing adoption of streaming readout (SRO) architectures poses new challenges compared with conventional triggered systems, shifting performance bottlenecks away from the front-end electronics towards data transport, network configuration, and host-side processing. In the CAEN Digitizer 2.0 architecture, digitized data are processed in real time by the FPGA and buffered in DDR4 memory. Depending on the selected readout interface and protocol, data are either routed through the embedded ARM processor, as in the case of USB and 1 GbE TCP communication, or streamed directly from the FPGA to the host system when using 10 GbE UDP. A detailed view of this end-to-end streaming architecture, from the ADC stage to the high-speed network link, is shown in Fig. 2.

Particular attention was devoted to network optimization, with a focus on the role of Jumbo Frames. Enabling a maximum transmission unit (MTU) of 9000 bytes allows large UDP datagrams to be transmitted without fragmentation, significantly reducing CPU overhead, minimizing packet loss, and improving overall link efficiency [2], [3]. As summarized in Table I, raising the MTU from the standard 1500 bytes to 9000 bytes substantially increases the sustainable single-link throughput. These optimizations are essential to fully exploit the available 10 GbE UDP bandwidth under sustained streaming conditions.

TABLE I
Effect of MTU on sustained single-link UDP throughput.

Interface	MTU (bytes)	Sustained throughput
10 GbE UDP	1500 (standard)	∼800 MB/s
10 GbE UDP	9000 (jumbo)	∼1140 MB/s
1 GbE TCP	1500 (standard)	∼110 MB/s
USB 3.1	–	∼280 MB/s

TABLE II
Measurement setup.

Item	Value
Digitizer	CAEN VX2730
Triggered firmware	Scope (raw waveform)
Streaming firmware	DPP-PSD (list mode)
Host CPU	Intel Core i7-10700K @ 3.80 GHz
Host RAM	32 GB
Network interface	Intel XL710-BM1 (4× SFP+)
Operating system	Ubuntu 24.04
Control software	minimal demo on CAEN FELib

III. Measurement Setup and Methodology

Benchmarks were carried out on a CAEN VX2730 digitizer connected to a Linux host through a dedicated point-to-point 10 GbE optical link. The host was equipped with an Intel Core i7-10700K CPU (3.80 GHz), 32 GB of RAM, and an Intel XL710-BM1 network interface (four SFP+ links), running Ubuntu 24.04. Data acquisition was driven by a minimal demonstration program built on top of CAEN FELib. The setup is summarized in Table II.

The host network stack was tuned for high-throughput UDP reception: the kernel socket receive buffers were enlarged (`net.core.rmem_max` and `rmem_default`), the device backlog queue was increased (`net.core.netdev_max_backlog`), the NIC receive ring buffer was set to its maximum (`ethtool -G rx 4096`), and Jumbo Frames were enabled by setting the interface MTU to 9000 bytes. These settings reduce per-packet overhead and packet loss under sustained streaming.

Two firmware configurations were exercised on the same board. In the *triggered* configuration (Scope firmware), raw waveforms were transmitted over 10 GbE UDP. For an event carrying the full waveform of every enabled channel, the payload size S_{event} (in bytes) is

$$S_{\text{event}} = H + b\, N_{\text{ch}}\, N_{\text{samples}}, \tag{1}$$

where $H = 24$ bytes is the fixed per-event header, N_{ch} is the number of enabled channels, N_{samples} is the record length expressed in samples, and $b = 2$ bytes is the storage size of a single digitized sample (one 16-bit word). The second term therefore grows linearly with both the channel count and the record length, so the aggregate data rate $R_{\text{data}} = f_{\text{event}}\, S_{\text{event}}$ (with f_{event} the event rate) scales in the same way and drives the acquisition towards the network-bandwidth ceiling. Accordingly, the event rate was scanned versus the number

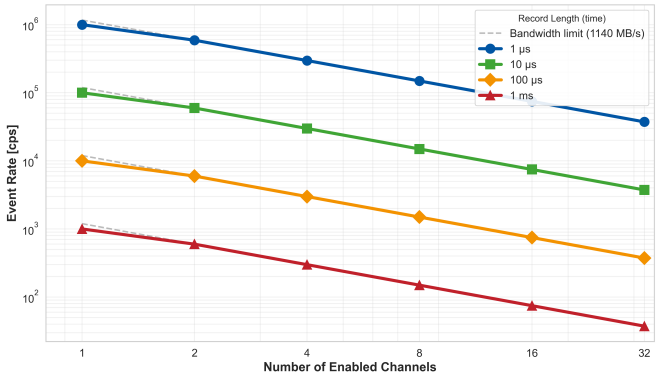

Fig. 3. Triggered readout saturation analysis with raw-waveform transmission over 10 GbE UDP, showing the maximum sustainable data throughput.

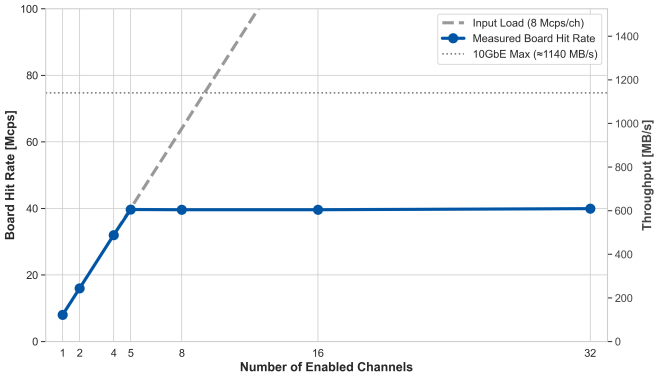

Fig. 4. Streaming readout saturation analysis in list-mode operation, showing the event rate at channel level and the onset of losses due to internal processing limitations.

of enabled channels for several record lengths (1, 10, 100 μs, and 1 ms) to map the saturation throughput. In the *streaming* list-mode configuration (DPP-PSD firmware, 16 bytes per hit), an external trigger at 8 MHz was applied and the per-board and per-channel hit rates were recorded as a function of the number of enabled channels, identifying the onset of losses.

On the software side, two access layers were compared: CAEN FELib, the low-level C library for digitizer control and data readout, and CoMPASS, CAEN's multiparametric DAQ application. For each layer the sustainable decoded event rate was measured under otherwise identical hardware conditions, so that the hardware data path and the software processing path could be characterized independently. Each configuration was characterized with a single acquisition run, and the reported value corresponds to the sustained throughput observed at the onset of packet loss for that configuration.

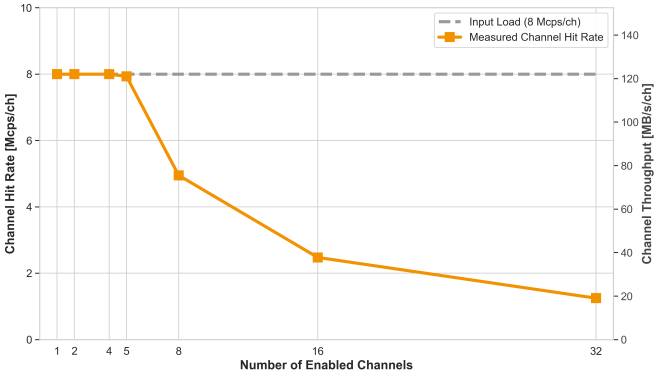

Fig. 5. Measured throughput limitation in decoded streaming readout using CAEN FELib, highlighting the software-side bottleneck due to per-event processing.

IV. Hardware and Software Benchmark Results

A. Triggered Readout over 10 GbE UDP

Hardware benchmarks were performed to characterize the maximum sustainable throughput in both triggered and streaming readout modes. In triggered readout with raw-waveform transmission over 10 GbE UDP, the system reaches a saturation throughput of approximately 1140 MB/s (about 1.1 GB/s) with no observed packet loss, as shown in Fig. 3. The measured ceiling coincides with the practical 10 GbE UDP bandwidth limit, demonstrating that the observed limitation originates from the network link rather than from any internal processing bottleneck.

B. Streaming Readout in List Mode

In streaming readout list-mode operation (DPP-PSD firmware, 16 bytes per hit), the per-channel hit rate reaches up to about 8 Mcps, measured with an external trigger at 8 MHz, while the per-board rate saturates at about 40 Mcps, corresponding to about 600 MB/s (Fig. 4). In this regime the dominant bottleneck is related to event sorting and handling within the FPGA, rather than to the 10 GbE data link: the board-level hit rate saturates well below the nominal network ceiling, with no UDP data losses detected. When waveform data are added to the streaming payload, the event size increases substantially and the achievable hit rate becomes directly constrained by the available network bandwidth, recovering a transport-limited behavior analogous to the triggered case.

C. Software-Side Benchmarks: FELib and CoMPASS

In addition to hardware performance, software-side benchmarks were carried out using CAEN FELib and CoMPASS. Raw data access through FELib shows no intrinsic limitation, and decoded triggered readout (one event per trigger) is also unconstrained, tested up to about 1 Mcps. Decoded streaming data, instead, reveal a software bottleneck associated with per-event processing and context switching, limiting the sustainable rate to about 5.6 Mcps, corresponding to about 85 MB/s with 16-byte hits (Fig. 5). CoMPASS, which provides advanced features such as multi-board synchronization, event building, real-time visualization, and online filtering, exhibits a lower throughput ceiling, of approximately 1 Mcps per setup (about 15 MB/s), consistent with its higher processing complexity. Table III summarizes the limiting factor identified in each operating regime.

TABLE III
SUMMARY OF OPERATING REGIMES AND LIMITING FACTORS.

Regime	Measured ceiling	Limiting factor
Triggered (Scope), decode on	∼1140 MB/s	10 GbE UDP (physical layer)
Streaming (DPP), decode off	40 Mcps (∼600 MB/s)	FPGA event-sorting algorithm
Streaming (DPP), decode on	5.6 Mcps (∼85 MB/s)	Software (context switches)
CoMPASS	∼1 Mcps (∼15 MB/s)	Software (complex processing)

V. DISCUSSION

The benchmark campaign shows that the limiting factor of the Digitizer 2.0 data path depends strongly on the operating regime. In triggered raw-waveform mode the system is transport-limited and saturates the 10 GbE UDP link, confirming that the FPGA and memory subsystem can sustain the full network bandwidth. In list-mode streaming the bottleneck moves inside the FPGA, to the event-sorting and handling logic, while the network link remains underutilized. On the host side, raw FELib access is transparent, but decoding and per-event processing introduce a software ceiling that is further reduced by the additional features offered by CoMPASS.

These observations suggest several concrete directions for improvement. At the firmware level, optimizing the FPGA event-sorting algorithm would address the dominant limitation of list-mode streaming. At the software level, three complementary strategies are identified: implementing batch processing on raw data, so that multiple hits are returned per API call and the context-switching overhead is reduced; adopting a multi-threaded producer-consumer architecture to process events in parallel; and employing a host CPU with higher single-thread performance, which directly benefits the per-event decoding path. Together, these measures target the two software bottlenecks observed in the decoded FELib and CoMPASS paths.

VI. CONCLUSION

We presented an end-to-end benchmark of the CAEN Digitizer 2.0 family in triggered and streaming readout modes. Triggered raw-waveform transmission over 10 GbE UDP sustains approximately 1.1 GB/s with no packet loss, limited by network bandwidth. List-mode streaming reaches about 40 Mcps per board, limited by the FPGA event-sorting algorithm, while adding waveforms to the payload returns the system to a transport-limited regime. Software benchmarks identify a per-event processing bottleneck in the decoded path, with CoMPASS showing a lower ceiling consistent with its richer feature set. Overall, the results demonstrate that the CAEN Digitizer 2.0 platforms can reliably support high-rate streaming readout applications when properly configured, and they highlight clear directions for future improvements in FPGA-level event handling and host-side parallelization.

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