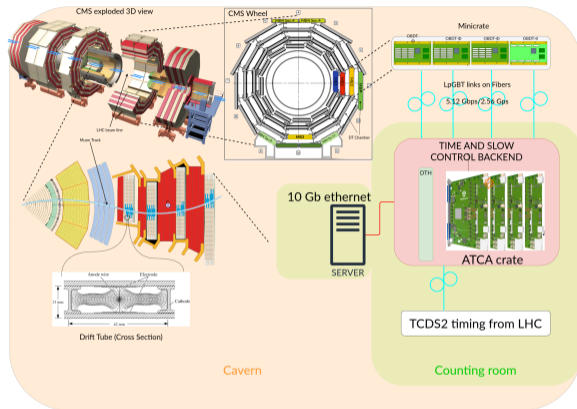


Timing and Slow Control Backend for CMS Drift Tube On-Board Electronics

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on behalf of the CMS Muon Group
May 25–29, 2026

INFN Padova Division



Main backend functions

- System based on 10 Serenity ATCA boards with powerful FPGAs (Virtex Ultrascale+) and optical links (90 per board).
- Distribution of the 40.079 MHz bunch-crossing clock and synchronous events to the on-detector electronics using LpGBT protocol .
- Synchronization signals from TCDS2 through the DAQ and Timing Hub Board (DTH).
- Monitoring detector electronics voltages, currents, temperatures, and thresholds, as well as configuration of the on-detector electronics and remote FPGA reconfiguration.

Firmware concepts

- CPU-less Ethernet architecture connected to a server plus Reliable UDP mapped to AXI-Lite / AXI-Stream (SURF framework).
- LpGBT logic in one 320 MHz clock domain.
- Transceivers operate in buffer-bypass mode → preserve time skew between reboots and reconfiguration.
- Backend implementation of LpGBT and SCA interfaces.

HL-LHC Phase-2 upgrade:

- Higher luminosity requires upgraded DT electronics with improved performance.
- Support for the new LHC machine clock distribution system.



Figure 1: The oscilloscope screenshot shows signals from a synchronous event acquired on three OBDT channels connected to the backend system. The horizontal time scale is set to 100 ps/div.

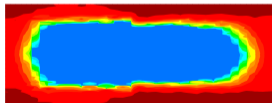


Figure 2: 5.12 Gbps Uplink eye diagram produced by the in-system IBERT core, bit error rate $< 10^{-6}$.

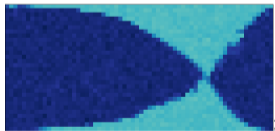


Figure 3: 2.56 Gbps Downlink eye opening diagram produced by the LpGBT chip; eye is not centered due to chip limitations.

Test and measurement performed using the provisional system: same FPGA, same clock distribution scheme

Timing requirements

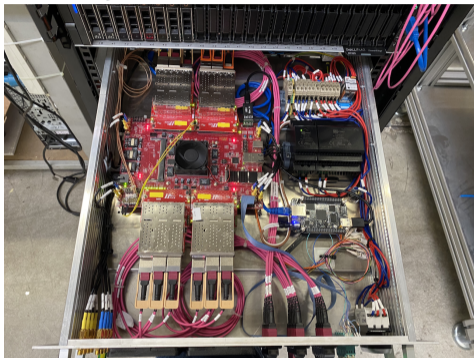
- DT intrinsic time resolution: approximately 2 ns.
- Required timing distribution precision: approximately 100 ps.

Timing performance	Min [ps]	Max [ps]
Channel-to-channel jitter RMS		5.95
Channel-to-channel skew	200	420

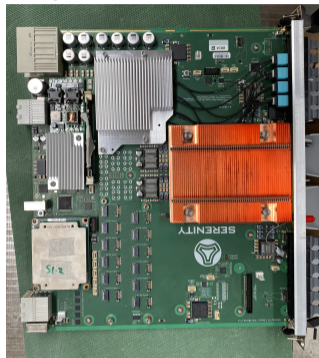
Signal integrity

- Downlink: 2.56 Gbps LpGBT eye diagram.
- Uplink: 5.12 Gbps eye diagram measured with the in-system IBERT core.
- Downlink eye opening: approximately 80%.
- Uplink eye opening: approximately 76%.

Provisional system



Final system



- Continue tests and early on-detector installation with the provisional HTG-940 system.
- Port the HDL design to Serenity hardware.
- Perform detector integration tests by the end of 2026.

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DT Phase-2 Upgrade

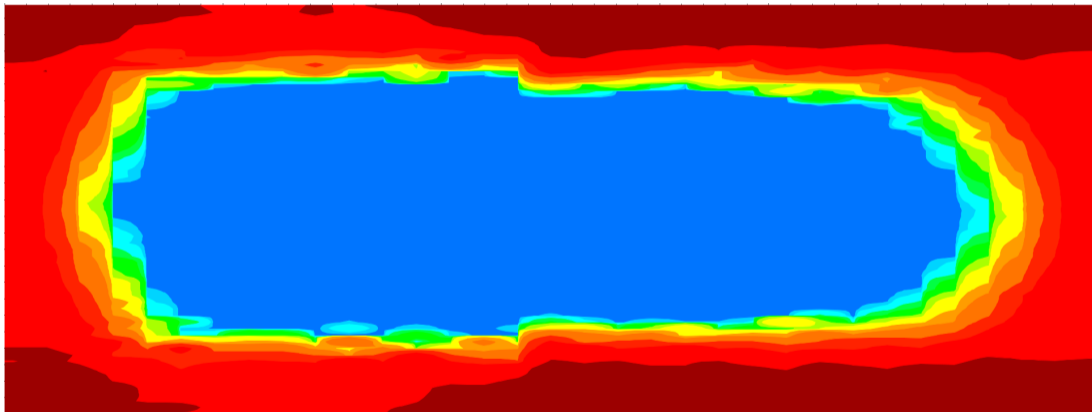


Figure 4: 5.12 Gbps uplink eye diagram produced by the in-system IBERT core, bit error rate (BER) $< 10^{-6}$.

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DT Phase-2 Upgrade

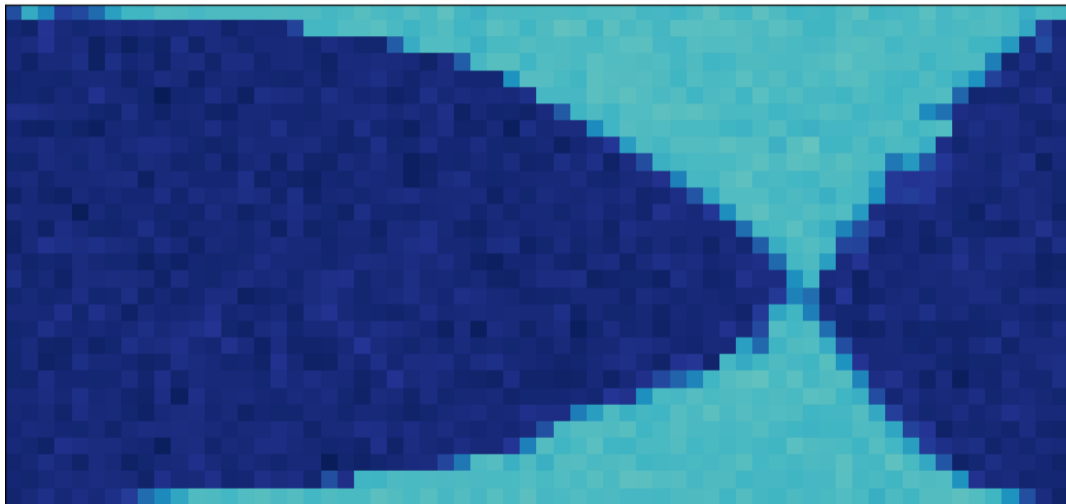


Figure 5: 2.56 Gbps Downlink eye opening diagram produced by the LpGBT chip; the eye is not centered due to chip limitations.

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DT Phase-2 Upgrade

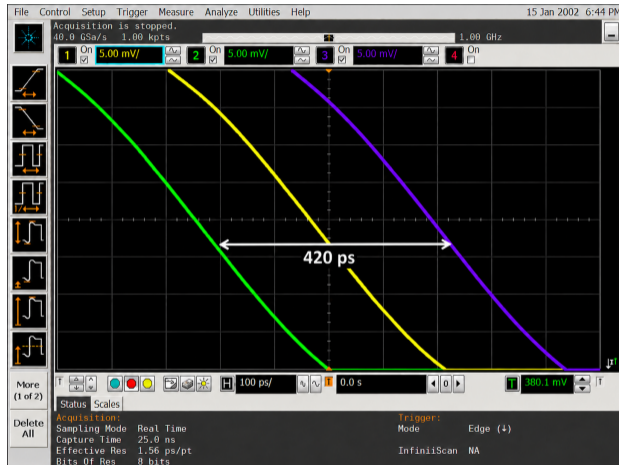


Figure 6: The oscilloscope screenshot showing signals from a synchronous event acquired on three OBDT channels connected to the backend system. The horizontal time scale is set to 100 ps/div.