

A Timing-Oriented Pixel Detector ASIC With Delay-Chain-Based Outputs for Three-Dimensional Particle Track Reconstruction

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Pixel level

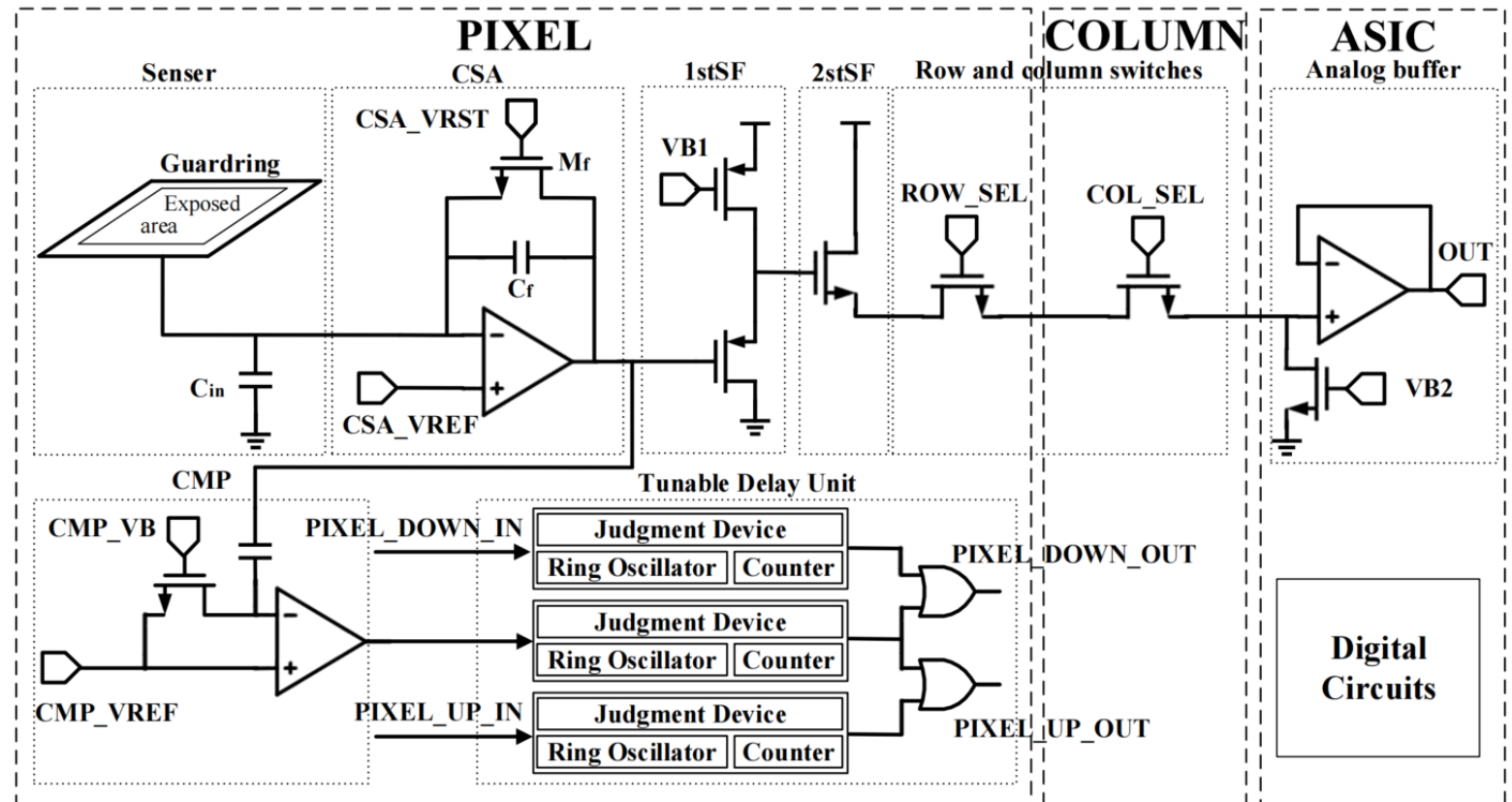
- Charge-sensitive amplifier (CSA)
- Comparator (CMP)
- Tunable delay unit (TDU)
- Two cascaded source followers (1stSF and 2ndSF)
- Row selection switch

Column level

- Column selection switch

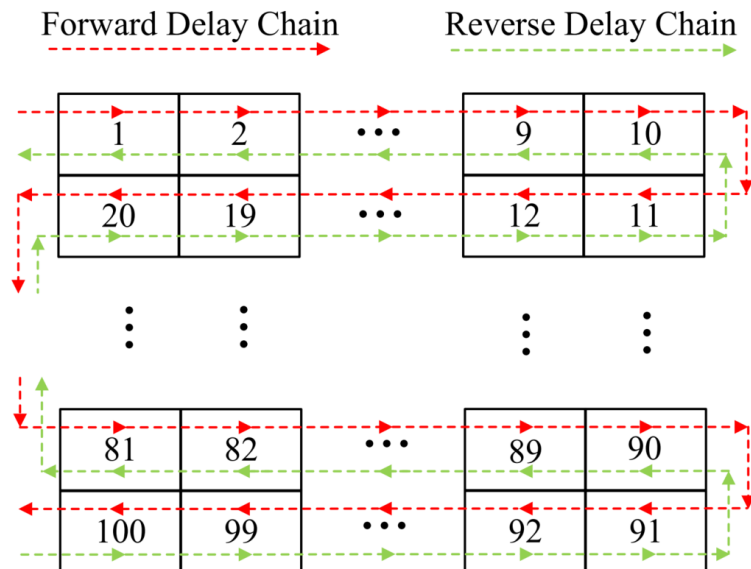
ASIC level

- Analog output buffer
- Digital circuit



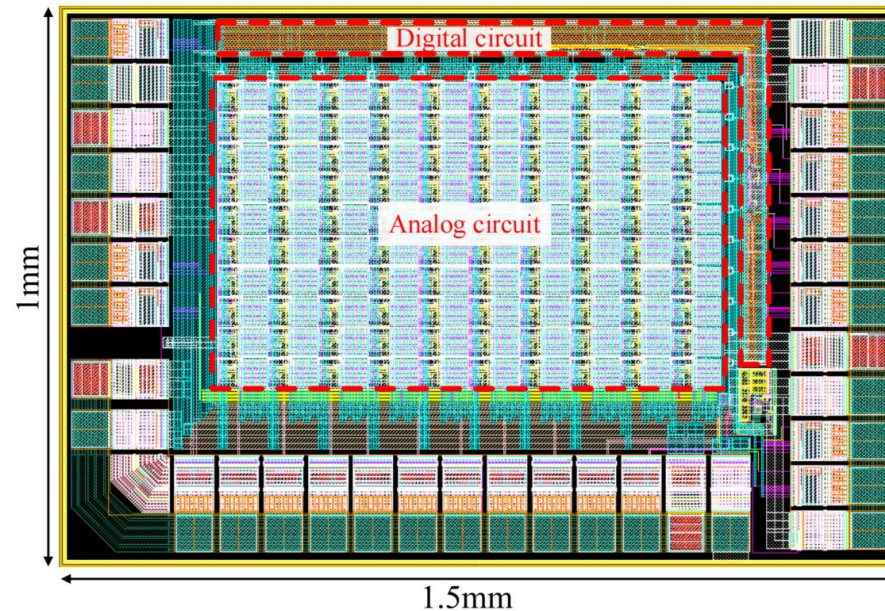
Chip details and results

In the design, strategies involving bidirectional paths (down and up)



Chip Layout Summary

- GSMC 130 nm CMOS technology
- Die size: 1 mm × 1.5 mm
- Pixel array: 10 × 10
- Pixel size: 90 μm × 50 μm



Achieved 3D particle track reconstruction using on-chip timing outputs

