Temperature-Induced Delay Drift in Xilinx FPGA Multi-gigabit Transceivers

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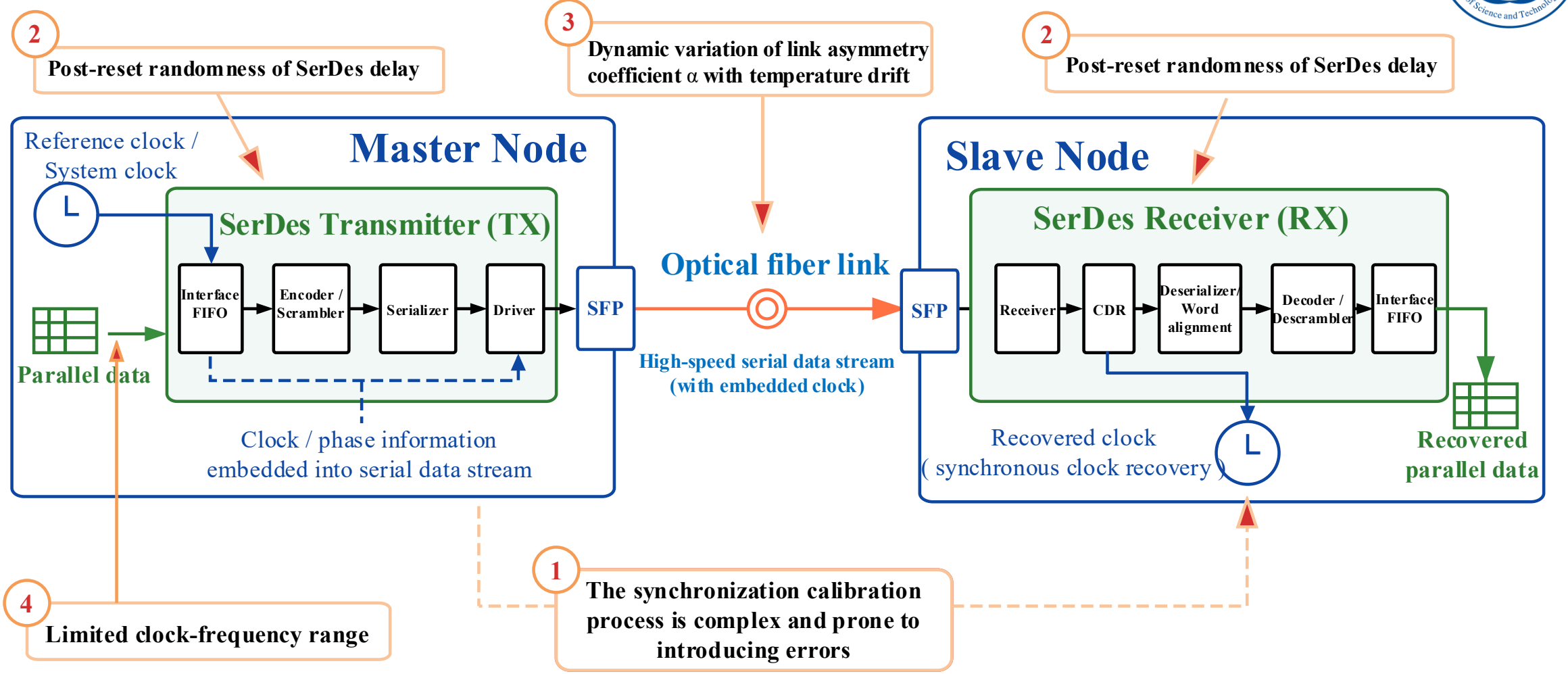
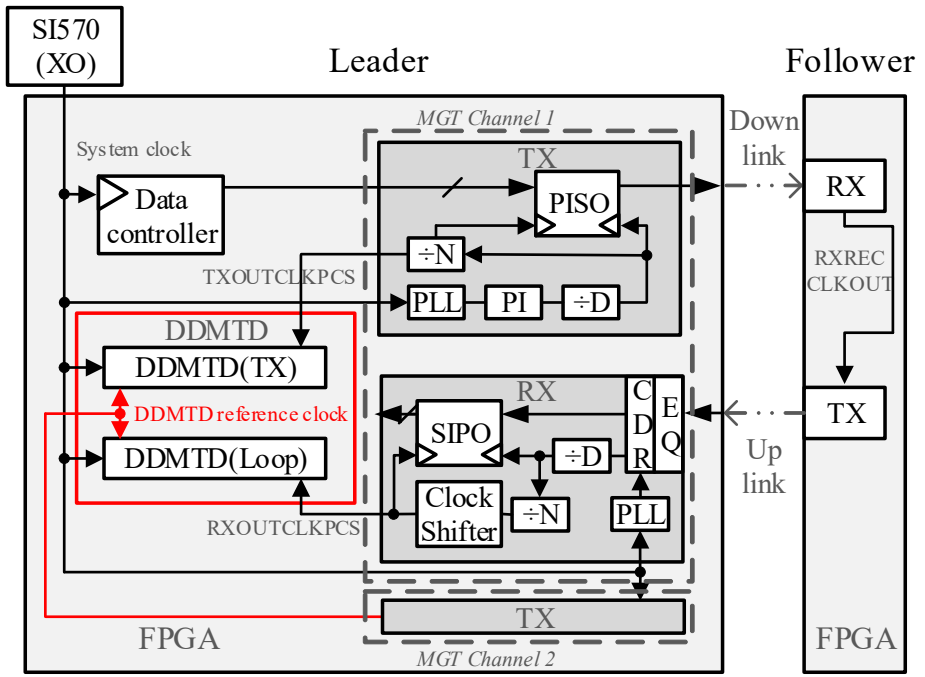
SerDes Based Clock Distribution and Synchronization

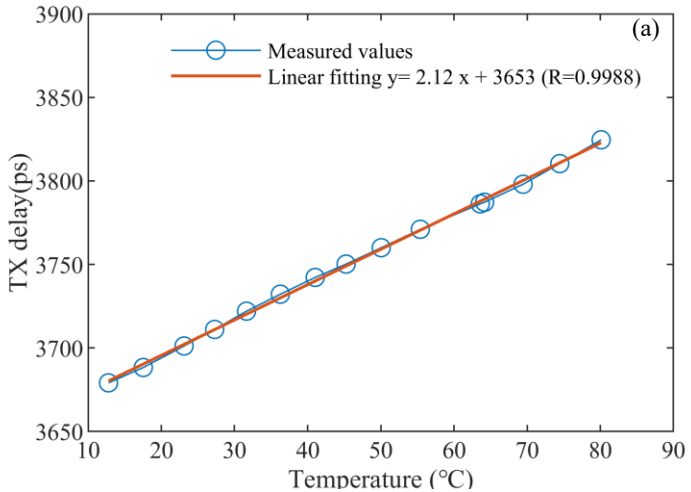


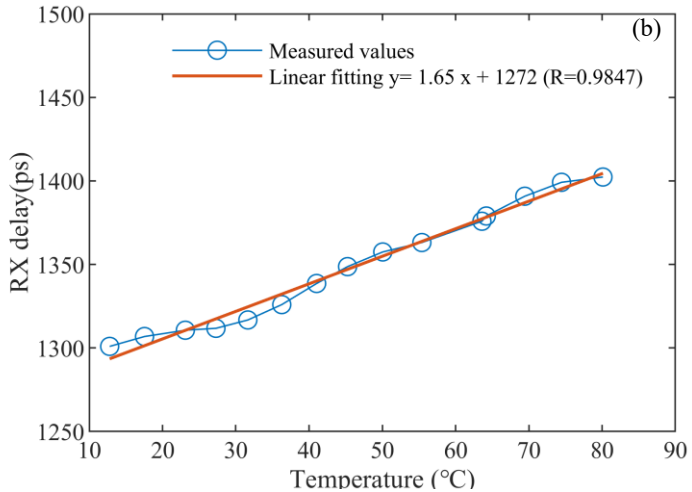
The master node transmits clock / phase information together with the high-speed serial data stream, and the slave node uses CDR to recover the clock and restore the data.

Delay Drift Measurement of TX & RX

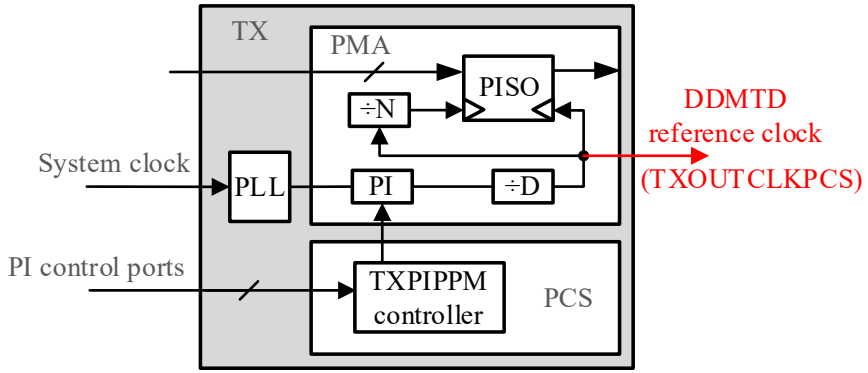


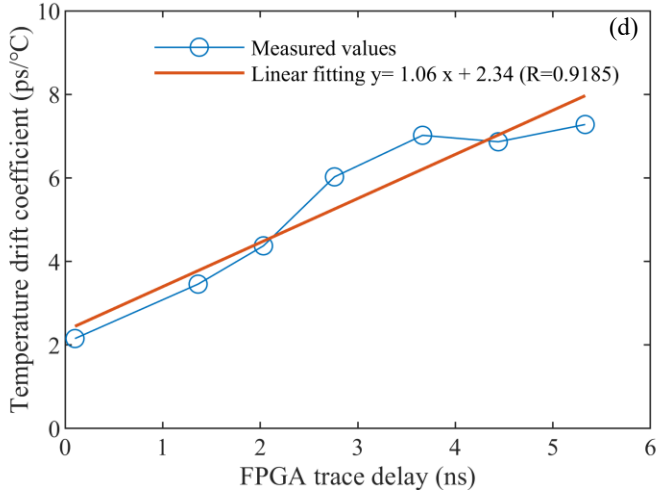
- ✓ Linear relationship – can be compensated
- ✓ Temperature coefficient: TX 2.21 ps/° C, RX 0.71ps/° C

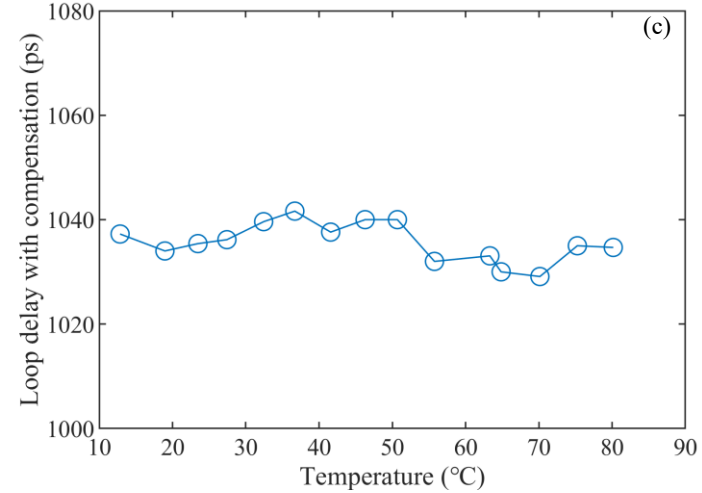




Temperature-robust DDMTD







Thanks for Attention!

Welcome to the poster !