Temperature-Induced Delay Drift in Xilinx FPGA Multi-gigabit Transceivers

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The Hidden Threat to MGT-Based Picosecond Synchronization

➢Background

- FPGA Multi-Gigabit Transceivers (MGTs) are a prevalent choice for high-precision clock distribution and synchronization due to their simplicity and flexibility.

➢The Overlooked Problem

- Electronics are usually housed in temperature-controlled environments, so their thermal delay drift is often neglected.
- However, we observed that this delay exhibits a severe linear dependence on the operating temperature, which poses a significant challenge to synchronization stability at picosecond levels.

TX Drift: 1.42 ps/°C RX Drift: 0.59 ps/°C

➢MGT-Based Synchronization

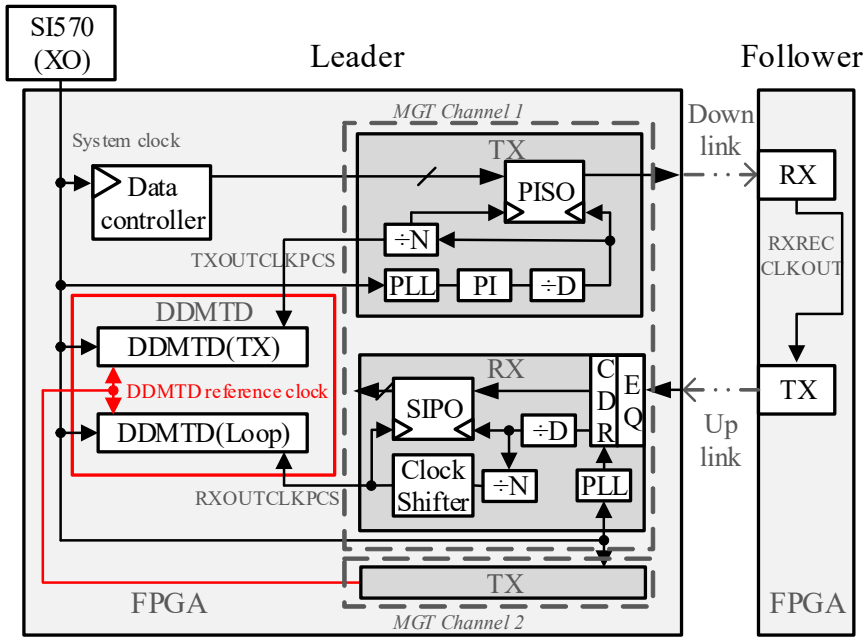
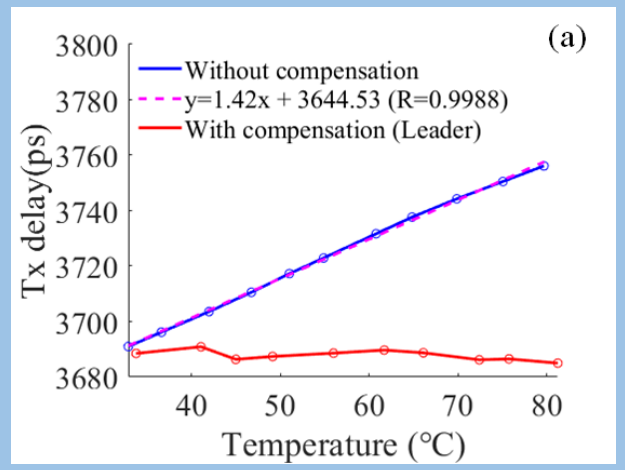
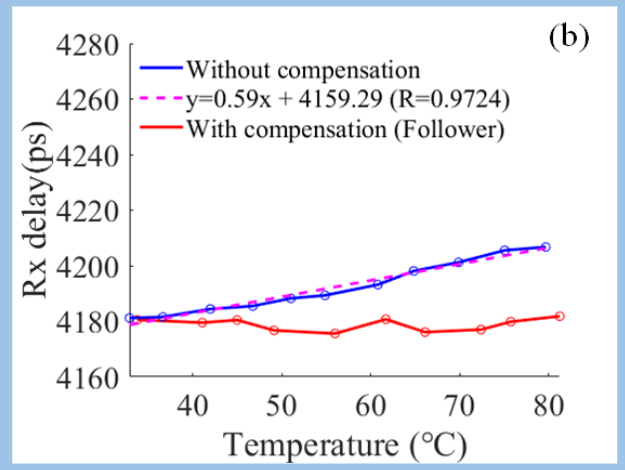
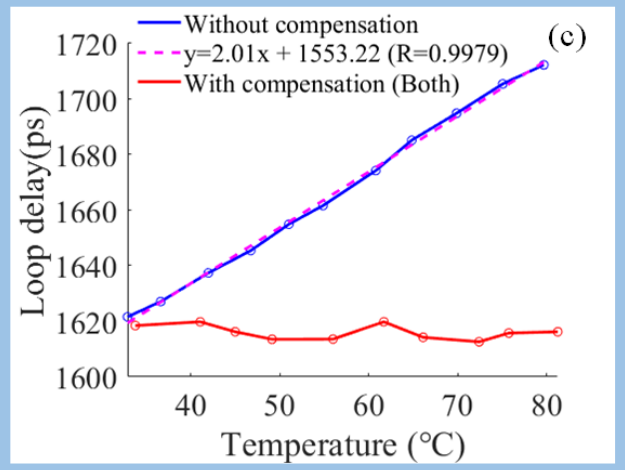


Fig. 1. Block diagram of the FPGA MGT-based clock distribution and synchronization system for temperature effects characterization and compensation.

On-Chip Compensation & Dramatic Improvement

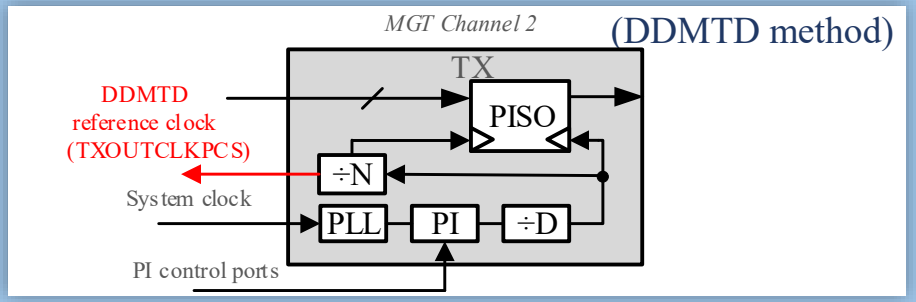






TX drift attributed to the PLL's steady-state error

$$\theta_e(\infty) = \lim_{s\to\infty} \frac{s^2 \cdot 2\pi f_{in}}{s^2(s + K_0 K_d F(s)/N)} = \frac{Na \cdot 2\pi f_{in}}{K_0 K_d b}$$



➢ Our Solution

- A temperature-robust, completely on-chip DDMTD method for bidirectional compensation.

➢ Compensation Result

- Maximum loop drift slashed from 90.7 ps to 7.6 ps (35℃ to 80 ℃)

THANKS

For Your Attention