A Low-Dead Time Wave Union FPGA TDC for Optical Beam-Loss Monitor System

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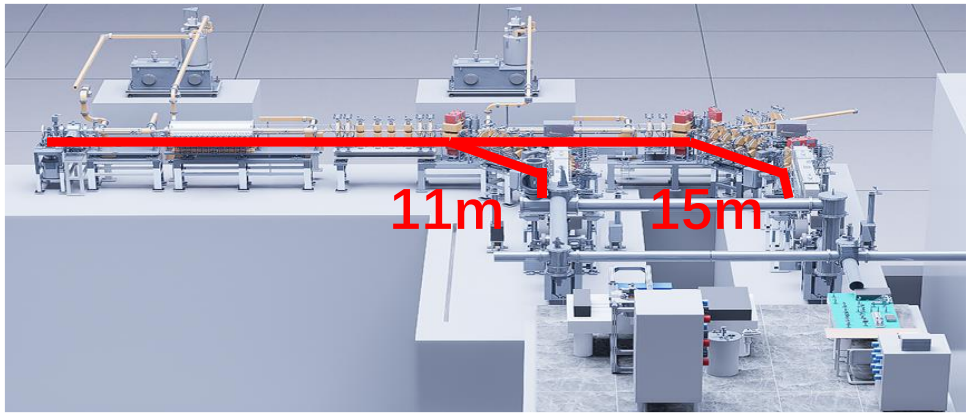
Background



Anhui University IR-FEL facility

"Beam-Loss" Light Timing → Position Reconstruction

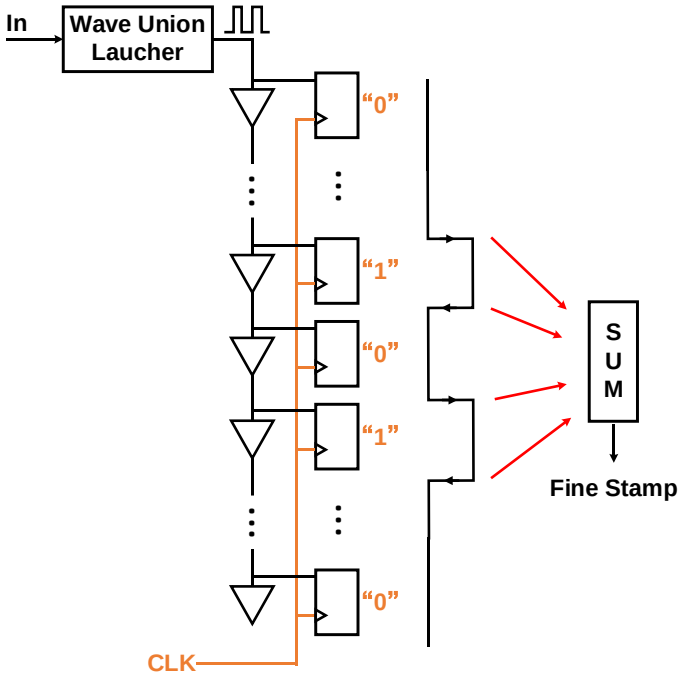
PMT → TIA → CMP → TDC

Compact Accelerator

Multi-bunch Pulse Structure

→ High Precision

→ Low Deadtime



Multiple Transitions

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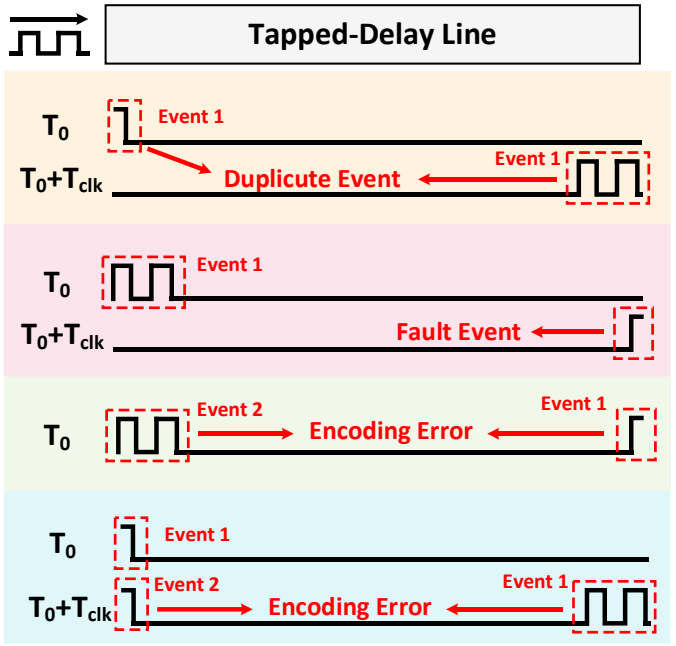
Multiple Measurements

↓

High Precision



Multi-Event Edge Mixing

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Forced Next-Cycle Invalidation

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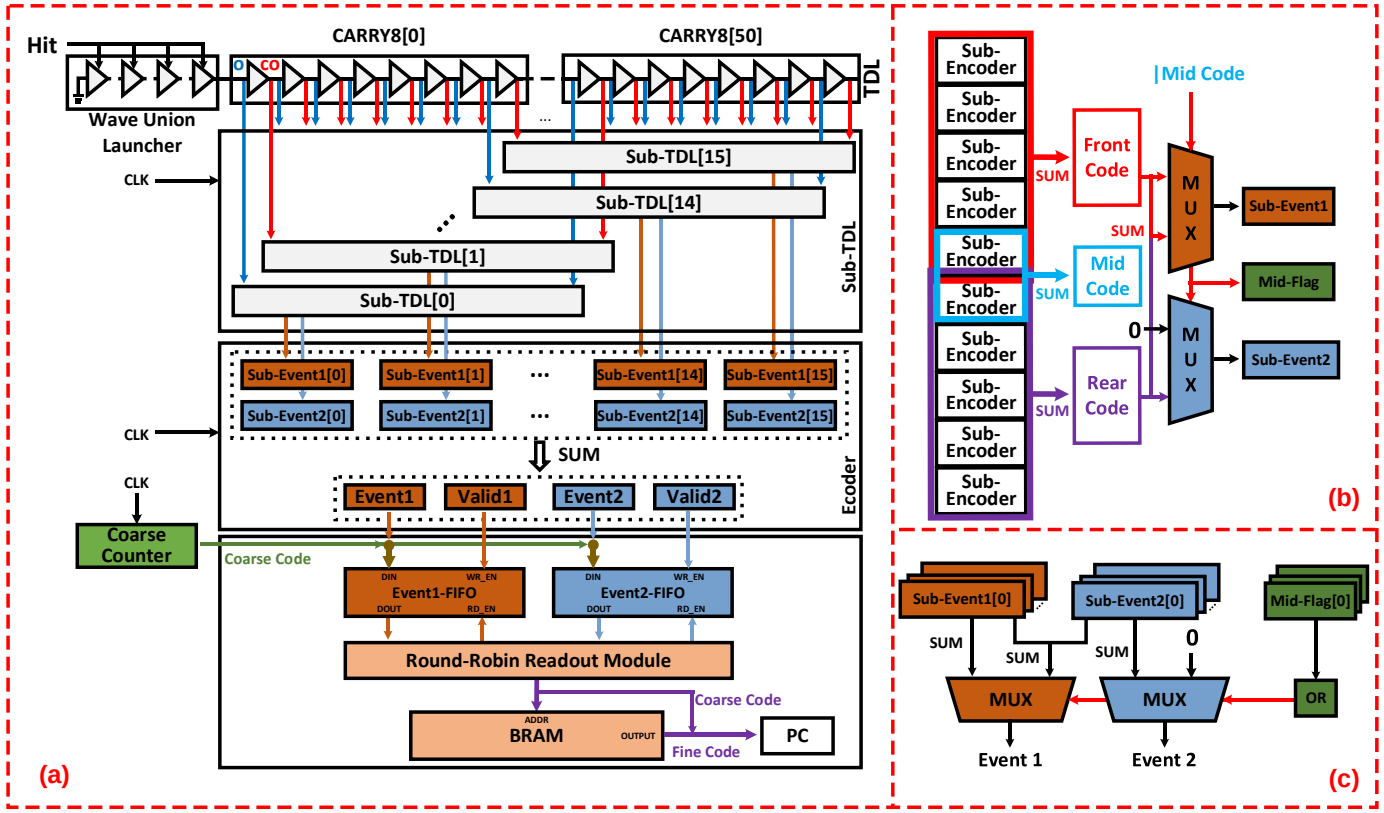
2-Cycle Dead-Time

Implementation

The proposed TDC has been implemented on an AMD UltraScale+ ZU3EG FPGA and operates at a 750 MHz system clock.

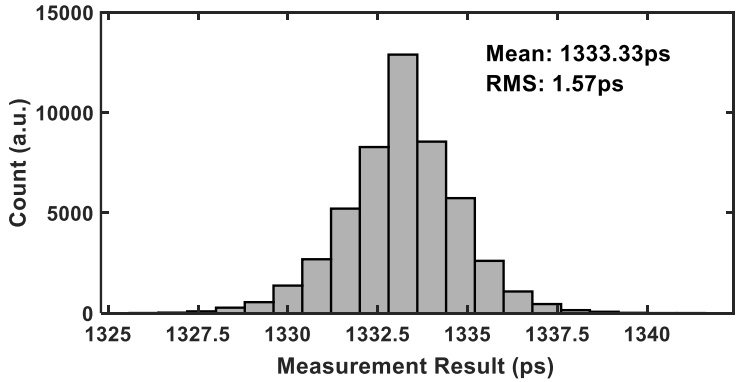


Block diagram of the proposed TDC

	Coarse	Event1 Valid	Event1 Fine	Event2 Valid	Event2 Fine	
Case 1	47	0	0	1	2593	← Pulser1
	48	0	0	1	2596	← Pulser2
	...					
Case 2	2	1	88	0	0	
	3	1	88	0	2887	
	4	0	0	0	2889	
	...					
Case 3	40	1	494	0	0	
	41	1	498	0	766	
	42	0	0	0	766	
	...					
Case 4	25	1	50	1	2811	
	26	0	0	0	2811	

Duplicute

Encoding results



Histogram of the measured 1.33ns time interval