# FPGA-Accelerated Pattern Recognition for the ATLAS Event Filter at the HL-LHC

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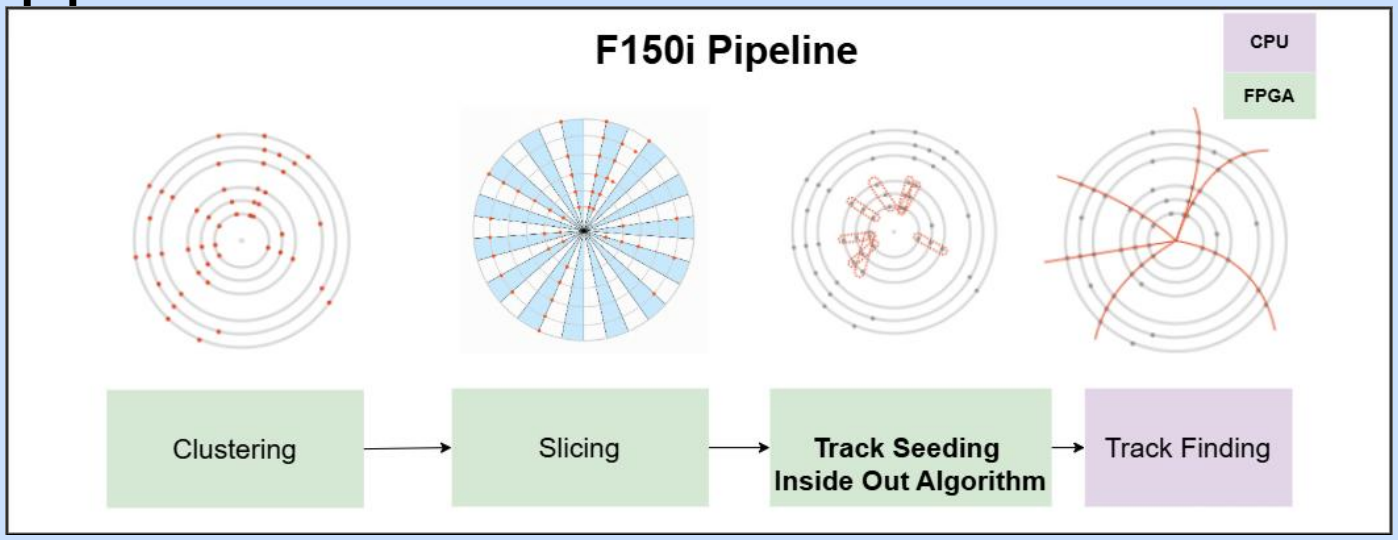
The HL-LHC will deliver ten times the instantaneous luminosity of the current LHC. The resulting increase in pileup and raw data rates creates an enormous computational burden on the ATLAS Event Filter farm — most critically in the processing of pattern recognition algorithms, where the complexity grows significantly.

The Event Filter Farm requirements include:

- **Throughput**
  - Regional tracking on the Level-0 readout data at 1 MHz
  - Full event tracking runs at 150 kHz
- **Power**
  - The EF farm has a power budget of 2.5 MW with maximum of 101 racks
- **Cost -** 8.8 MCHF

To meet these requirements, the EF Tracking community has been investigating heterogeneous platforms.

- The FPGA-based **F150i** pipeline moves **50% of the tracking pipeline into FPGAs**



# F150i Development Framework