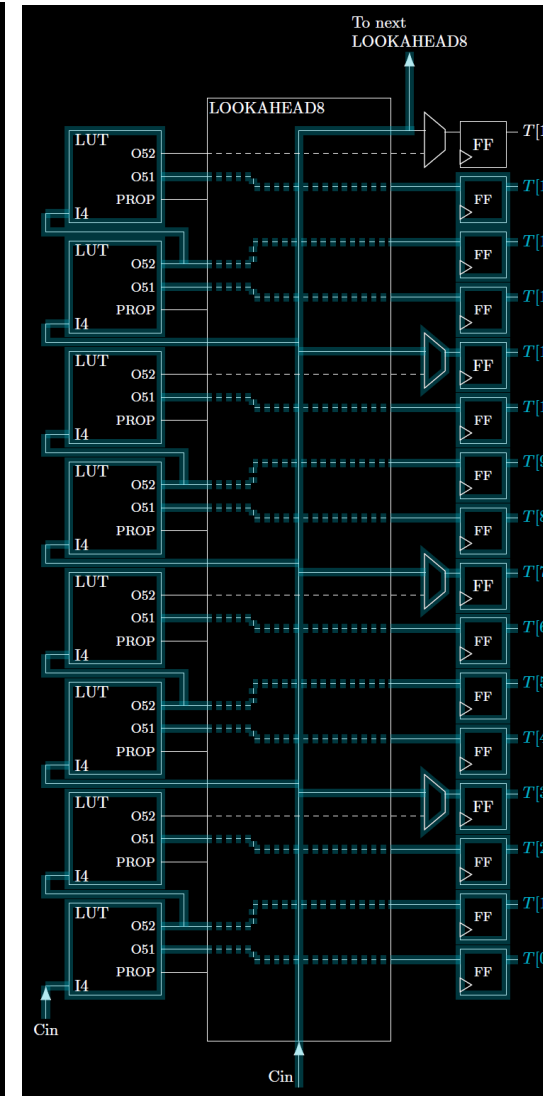
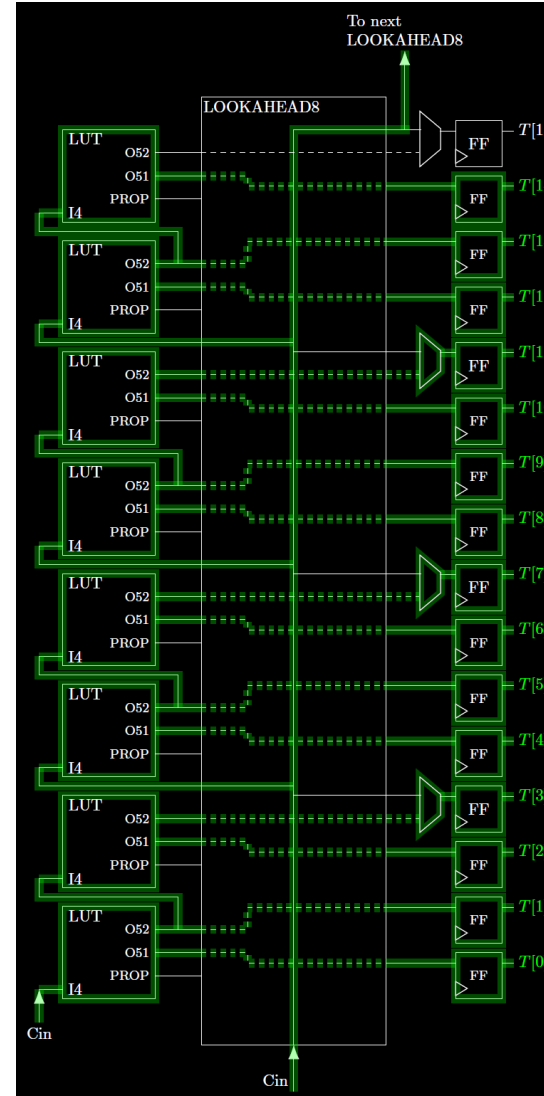
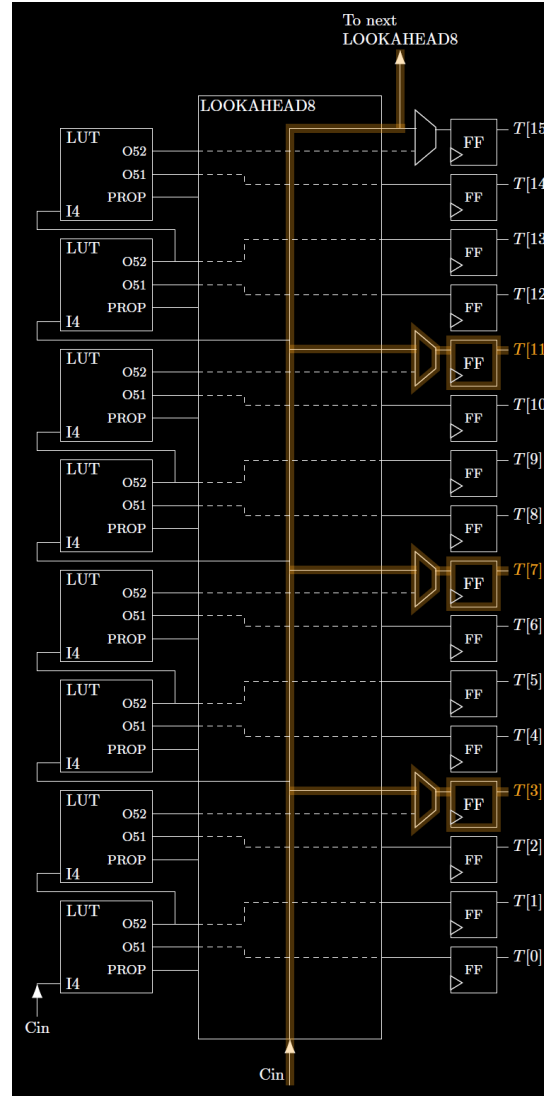


Rationale and design

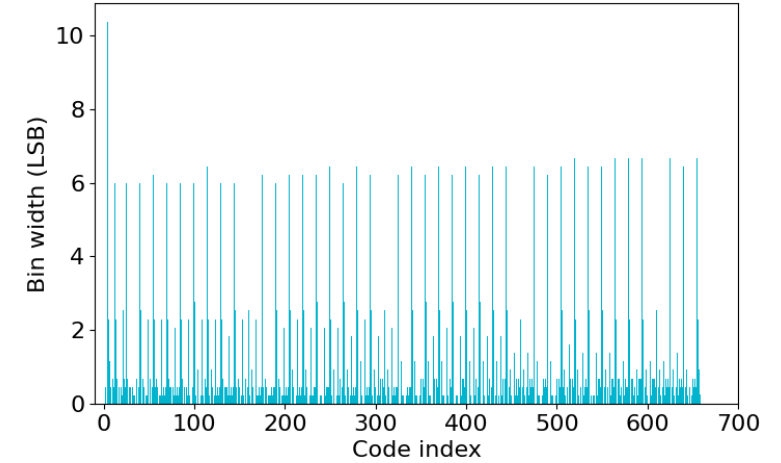
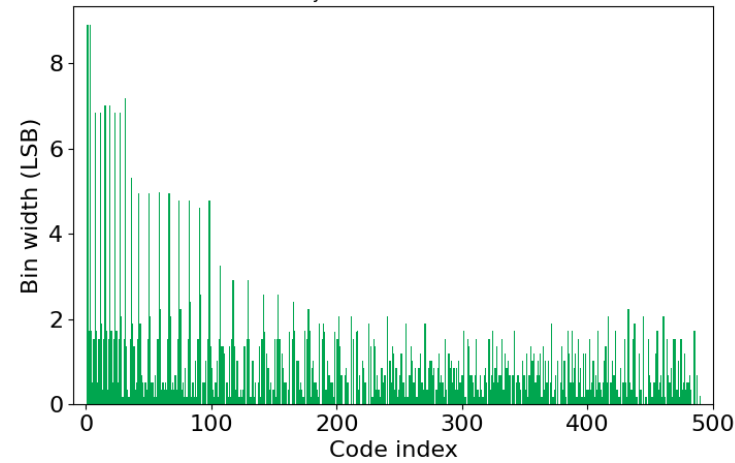
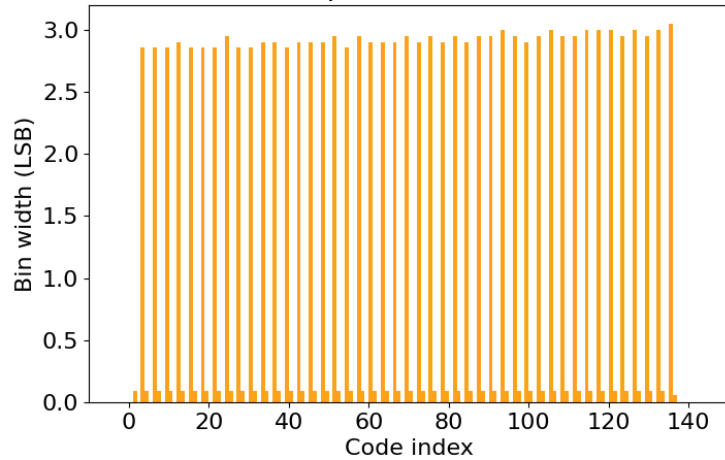
Goal: Evaluate the Versal architecture potential for TDC in FPGA.

Architecture	Fabrication process	Precision (ps RMS)
Virtex-7	28 nm	~ 10
UltraScale	20 nm	~ 5
UltraScale+	16 nm	~ 2.5
Versal	7 nm	?



Results

Code density



	Reference UltraScale+	Only Lookahead	Only LUT	Hybrid
Resolution (ps)	1.8	10.5	2.9	2.9
Q error (ps)	1.3	8.7	2.9	2.9
Precision (ps)	2.7	12.5	4.5	4.5