Readout Electronics System for the ECAL of the VLAST-P Payload

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***Abstract*—The VLAST-P (Very Large Area gamma-ray Space Telescope-Pathfinder) is a miniaturized space detector designed for the observation of solar high-energy gamma-rays in the MeV to GeV energy range, as well as energetic protons associated with solar flares. The electromagnetic calorimeter (ECAL) is a key sub-detector for precise energy measurement of incident photons and for providing hit information used in trigger decisions. A low-power, wide-dynamic-range, low-noise, and radiation-tolerant readout electronics system has been developed for the ECAL, consisting of four Front-End Electronics (FEE) modules and one Preamplifier Module (PAM), with a total power consumption of approximately 23 W. Signals from Avalanche Photodiodes (APDs) are processed by charge-sensitive amplifiers (CSA) and split into high- and low-gain channels to achieve a wide dynamic range. The FEEs digitize 100 analog channels, perform onboard data buffering, generate hit signals, and transmit scientific data to the payload electronics control unit (ECU). To assure long-term reliability in the harsh space environment, radiation hardness, thermal design, components and board level quality control were carefully considered. In addition, the key indexes of linearity, noise level, and dynamic range were preliminarily studied. Experimental results show that the equivalent noise charge (ENC) of the high-gain channels is below 4 fC, and the system achieves an equivalent noise energy (ENE) of 0.33 MeV. The low-gain channels provide a linear measurement range up to approximately 100 pC, corresponding to a maximum measurable energy of 9.2 GeV. These results demonstrate that the system satisfies the physical requirements of the detector.**

***Index Terms*—Calorimeter, Cosmic rays, VLAST-P, Readout electronics, space electronics.**

I. Introduction

HIGH-ENERGY gamma-ray observations play an important role in studies of dark matter, cosmic-ray physics, and high-energy time-domain astrophysics. Dark matter can be detected indirectly through gamma-rays produced by the annihilation or decay of dark matter particles. The Fermi Large Area Telescope (Fermi-LAT) has provided invaluable long-term observation data for over a decade, establishing a global benchmark for gamma-ray space probes [1]. The Astro-rivelatore Gamma a Immagini Leggero (AGILE) has delivered substantial advancements in high-energy gamma-ray astrophysics [2]. Concurrently, the DArk Matter Particle Explorer (DAMPE) has achieved unprecedented energy precision in measuring high-energy cosmic electrons and gamma rays up to tens of TeV [3], [4], [5]. Other prominent missions, such as the Alpha Magnetic Spectrometer (AMS-02) [6] and the Calorimetric Electron Telescope (CALET) [7], have similarly enhanced the direct measurement of primary cosmic-ray spectra, while the upcoming High Energy cosmic-Radiation Detection (HERD) facility planned for the China Space Station will specifically target high-precision cosmic-ray composition measurements [8], [9].

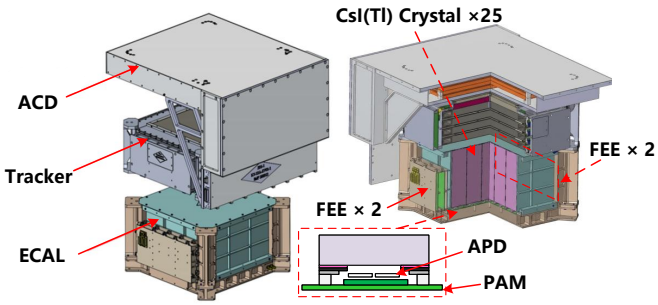

Fig. 1. The schematic of the VLAST-P detector payload.

To overcome the geometric acceptance constraints of current telescopes, the Very Large Area gamma-ray Space Telescope (VLAST) has been proposed as a next generation, world-leading instrument. Compared to current space-borne observatories, VLAST features a significantly higher effective acceptance and unparalleled measurement precision [10]. To systematically validate the core detection and electronic methodologies of VLAST, the VLAST-Pathfinder (VLAST-P), a compact version of the baseline detector, is scheduled for launch in late 2026. The primary scientific objectives of VLAST-P are focused on addressing critical gaps in high-energy solar physics by detecting gamma-rays within the 50 MeV to 5 GeV energy range and capturing high-energy proton signatures during solar flares. Furthermore, it will conduct coordinated observations with China's Advanced Space-based Solar Observatory (ASO-S) to enable comprehensive multi-wavelength synergetic studies.

As shown in Fig. 1, the payload consists of three sub-detectors: an anti-coincidence detector (ACD), a tracker, and an electromagnetic calorimeter (ECAL). The ECAL, which is composed of 25 CsI(Tl) crystal bars with a size of 6 cm ×

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6 cm × 20 cm for each, is a crucial sub-detector with a longitudinal depth of about 10 radiation lengths. It is designed to perform high-precision energy measurements of incident gamma-rays and to provide trigger information. To ensure reliability and compactness, two independent Avalanche Photodiodes (APDs), configured as a primary/redundant pair, are air-coupled to the bottom of each crystal with a 4.4-mm gap. Considering the energy measurement range and the on-orbit radiation environment, this paper presents a large-dynamic-range, high-reliability readout electronics system for the ECAL of the VLAST-P payload.

The main function of readout electronics is to measure the signals of APDs. Bench test results of the crystal assembly reveal that when the APD is air-coupled to the light output window of a CsI(Tl) crystal bar at a distance of 4.4 mm and operated at a gain of 50 (S8664-1010 from Hamamatsu [11]), the stable light yield reaches approximately 1450 p.e./MeV. Based on the physical requirements of the detector system, the calorimeter must provide an unbiased trigger threshold of 1.8 MeV and an upper energy measurement limit of 5 GeV. Simulation results suggest that the maximum energy deposition in a single crystal for a 5 GeV photon is around 4.1 GeV [12]. To achieve a high signal-to-noise ratio (SNR) of 5 at the minimum threshold, the equivalent noise charge (ENC) of the front-end electronics is required to be below 4.2 fC. The dynamic range requirement extends to approximately 48 pC.

II. System Architecture of Readout Electronics

The architecture of the readout electronics for ECAL is presented in Fig. 2. Photoelectric conversion for the 25 CsI(Tl) crystal bars is performed by 50 independent APDs. To process these detector signals under strict noise constraints, the readout electronics system is structurally partitioned into a Preamplifier Module (PAM) positioned at the bottom adjacent to the detectors, and four Front-End Electronics (FEE) modules mounted on two sides. High-voltage bias for the APDs and low-voltage rails for both the PAM and FEEs are supplied by a dedicated High-Voltage (HV) Supply Board and a Secondary Power Supply Board located within the Electronics Control Unit (ECU), respectively.

To implement a robust hot redundancy architecture, the 25 primary and the 25 redundant APDs, along with their respective readout electronic channels, are connected to two separate pairs of FEEs. These two structures are powered by isolated power paths, thereby ensuring complete electrical and functional redundancy across the entire electronics architecture.

The PAM performs charge integration on current pulses from the APDs and subsequently splits them into high-gain and low-gain differential voltage signals, yielding a total of 100 independent analog signal channels. Each pair of FEEs independently takes charge of the digitization, data buffering, and control tasks for 50 of these channels.

Each FEE has two dedicated hit generation channels. Based on the designated threshold and logic within each hit channel, a board-level hit signal is determined and generated, which is

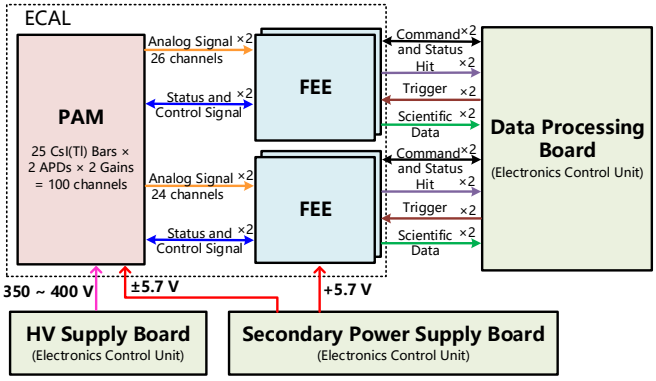


Fig. 2. Architecture of the readout electronics system for the ECAL.

then formatted into an RS-422 negative pulse with a width of 160 ns and transmitted to the ECU. A trigger board located inside the ECU receives all hit signals from the ECAL and combines them with hit inputs from other sub-detectors to decide whether to issue a global trigger signal.

Upon receiving the global trigger, the FEE caches the current event's waveform data into its internal RAM for subsequent retrieval and processing. The processed data is subsequently packed and transmitted to the ECU via a user-defined serial protocol based on Low Voltage Differential Signaling (LVDS) at a clock frequency of 25 MHz.

Command transmission from the ECU to the FEEs and status parameter monitoring from the FEEs back to the ECU are both conducted via an RS-422-based 115.2 Kbps half-duplex serial bus. In addition, the FEE architecture supports on-orbit electronic linearity calibration to track and compensate for channel gain variations over long-term space operation.

III. Design of the PAM

Currently, no space-qualified, radiation-hardened Application-Specific Integrated Circuit (ASIC) can simultaneously cover such an extensive dynamic range (4.2 fC to 48 pC). As shown in Fig. 3, to meet the wide dynamic range requirement, a dual-gain design with gain ratio of approximately 10 is implemented. To achieve better energy resolution, the high-gain channel is employed for small signals ($<$1 pC), while the low-gain channel is simultaneously used for large signals ($>$1 pC).

To achieve low-noise performance, a Charge-Sensitive Amplifier (CSA) characterized by minimal sensitivity to input capacitance variations is utilized for charge integration and charge-to-voltage conversion. Owing to the large input capacitance of the APD (approximately 270 pF), a low-noise Junction Field Effect Transistor (JFET) is integrated at the immediate input stage of the CSA.

The noise of the input JFET is composed of channel thermal noise, $1/f$, and leakage current shot noise [13]

$$ENC_T^2 = \frac{1}{e^2}\left[A_1\frac{1}{\tau}\gamma\frac{2kT}{g_m}C_\Sigma^2 G_C + A_2\pi A_F C_\Sigma^2 + A_3\tau e I_{LT}\right] \quad (1)$$

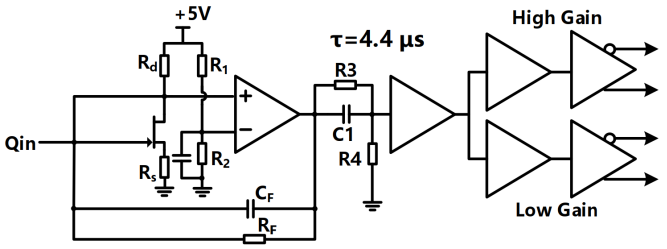


Fig. 3. The schematic diagram of the PAM single APD readout electronics.

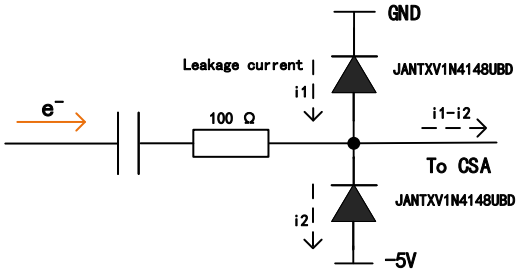


Fig. 4. The schematic diagram of the protecting circuit.

where g_m is the transconductance of the transistor, τ is shaping time, G_C is a factor related to the induced gate current noise of the transistor, γ is the thermal noise factor of the channel, A_F is a factor of the $1/f$ noise [14], I_{LT} is the gate leakage current of the transistor, and C_Σ is the total capacitance of the input terminal of the preamplifier. The parameters except C_Σ are only related to the characteristics of the transistor itself. The channel thermal noise and the $1/f$ noise have a common coefficient $C_\Sigma/\sqrt{C_T}$, and owing to:

$$C_\Sigma = C_T + C'_D = C_T + C_D + C_S + C_f + C_{die} + C_t \quad (2)$$

$$\frac{C_\Sigma}{\sqrt{C_T}} = \frac{C_T + C'_D}{\sqrt{C_T}} = \sqrt{C'_D}\left(\sqrt{\frac{C'_D}{C_T}} + \sqrt{\frac{C_T}{C'_D}}\right) \quad (3)$$

The lowest noise can be attained when the transistor capacitance C_T equals the input capacitance C'_D [15]. Yet, capacitance matching is not the sole critical factor in transistor selection; a higher transconductance g_m and a larger equivalent saturated drain current I_{DSS} of the JFET contribute to a lower noise [16]. Considering the large junction capacitance of the APD and the harsh space radiation environment, the military-grade IFN147 JFET is selected for the design. It features a large input capacitance of 75 pF and a high transconductance of 30 mS. Notably, the IFN152, a component from the same product series, has been successfully utilized in the Tianwen-1 mission [17].

Owing to the long scintillation decay time of the CsI(Tl) crystal (approximately 1.3 μs), the current pulse generated by the APD is an exponentially decaying signal. To maximize charge collection efficiency while mitigating event pile-up, the shaping time is optimized and set to 4.4 μs.

Following amplification across the dual-gain channels, the signals are converted into a differential format before transmission to the FEE, enhancing immunity to external interference and ensuring matching with the differential inputs of the ADCs. Additionally, during the single-ended-to-differential conversion process, the DC bias can be adjusted to maximize the utilization of the ADC's full-scale dynamic range. To mitigate crosstalk between the dual-gain channels, the high-gain and low-gain signals are connected to the FEE through separate, dedicated connectors.

To safeguard the sensitive JFET input stage against transient voltage spikes from APD bias HV fluctuations or Electrostatic Discharge (ESD) during handling, a protection circuit is implemented at the input. As illustrated in Fig. 4, the circuit consists of a series resistor and a pair of clamping diodes. Standard TVS devices are rejected here due to their excessive leakage currents, which would induce baseline shifts due to the large feedback resistor of the CSA. Instead, the Microsemi JANTXV1N4148UBD, a high-reliability dual-diode component, is employed. Benefiting from its ultra-low leakage current and exceptional symmetry, this configuration provides robust transient voltage clamping while preserving the low-noise performance of the readout electronics.

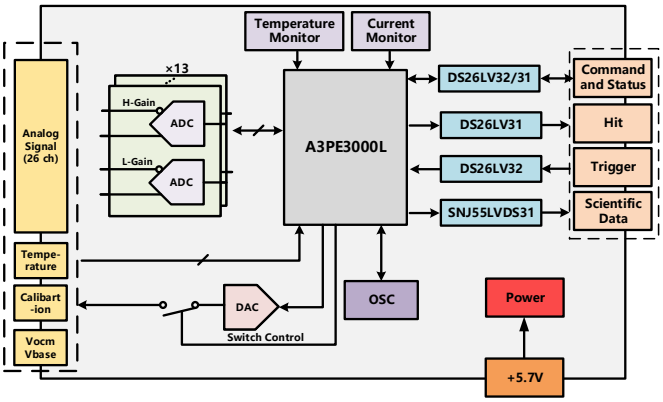


Fig. 5. The schematic diagram of the FEE module.

IV. Design of the FEE Module

The ECAL has four FEE modules, with two modules positioned on each side. On one side, FEE-1 and FEE-2 are respectively connected to the primary and redundant 26 differential analog signals of 13 crystal bars. On the opposite side, FEE-3 and FEE-4 handle the remaining 12 crystal bars, respectively receiving 24 differential analog signals from the primary and redundant paths. All four FEEs utilize an identical electrical design, differing only in their physical hardware layouts. To maintain this hardware uniformity, the two unused ADC inputs on FEE-3 and FEE-4 are tied to the common-mode voltage V_{CM} to prevent floating states. FEE-1, FEE-3 and the primary APD readout channels of the PAM share one low-voltage secondary power supply channel, whereas FEE-2, FEE-4, and the redundant APD readout channels of the PAM are powered by another independent low-voltage secondary power supply channel. The schematic diagram of the FEE is given in Fig. 5. Its major parts will be described below in detail.

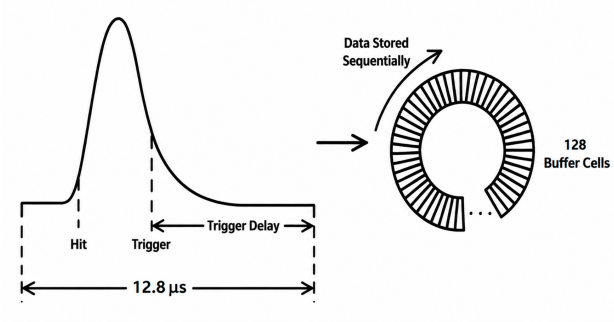


Fig. 6. The schematic diagram of the waveform circular buffer.

A. Digitization and Processing of Waveform

The CSA output pulse exhibits a 2 μs rising edge. To ensure precise peak estimation and event triggering, an ADC is required. Given the limitations in integration density and power consumption for high-speed space-qualified ADCs, a 16-bit AD9266-EP from ADI is selected. This enhanced-product device supports defense and aerospace applications (AQEC standard), featuring a compact 5 mm $\times$ 5 mm package. It allows for a configurable sampling rate from 10 MSPS to 65 MSPS, with power consumption of approximately 70 mW at 10 MSPS [18]. This configuration provides over 20 samples along the rising edge, enabling precise pulse amplitude determination and minimizing sampling-induced timing jitter.

To preserve the complete waveform information of individual events, each channel employs a circular buffer implemented with a 128-deep, 16-bit wide dual-port RAM, corresponding to a continuous acquisition window of 12.8 μs. As illustrated in Fig. 6, during normal operation without a trigger, the circular buffer continuously stores the latest samples. Upon reception of a valid trigger signal from the ECU, the write operation is maintained for a trigger delay time, which can be configured in orbit, to ensure complete waveform capture, after which the buffer is frozen and the stored samples are transferred for downstream processing.

In the normal data acquisition mode, only reduced event parameters, such as pulse amplitude and baseline mean value, are extracted and transmitted to reduce data bandwidth requirements. The baseline is estimated independently for each event from the corresponding waveform window to compensate for slow baseline drifts. Conversely, for dedicated noise evaluation, fixed-position samples from the full waveform window are utilized to ensure an accurate assessment of baseline noise characteristics, ensuring a statistically unbiased evaluation of the noise level.

B. Hit Signal Generation

As shown in Table I, the payload requires hit information from the ECAL for trigger selection across four operational modes. Each FEE features two hit output channels. When both the primary and redundant ECAL readout electronics operate normally, the redundant subsystem functions as an independent, concurrently operating detector, allowing the primary and redundant hit outputs to be mapped to different hit generation logics. Furthermore, each FEE hit output is fully configurable to any hit logic, thereby providing mutual backup capability in case of operational anomalies.

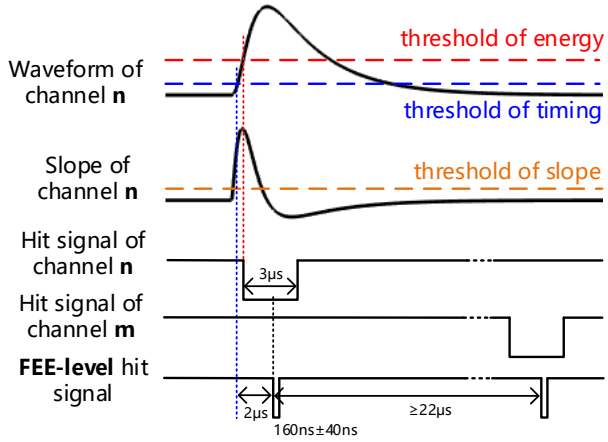


Fig. 7. The hit generation mechanism for unbiased triggering.

Fig. 7 illustrates the hit generation mechanism for unbiased triggering. Due to the varying energy thresholds across different hit logics and the slow pulse rising edge (approximately 2 μs), a fixed, low threshold for timing set at 5 σ of the noise floor is applied to minimize time walk. A slope threshold is also introduced to suppress noise and ensure leading-edge triggering. A channel-level hit is declared only when all three conditions are satisfied: the timing threshold is exceeded, the energy threshold is exceeded, and the slope threshold is crossed for three consecutive samples. The system performs the logical judgment at a fixed delay of 2 μs after the timing threshold is exceeded. If the channel-level hit complies with the generation logic, a valid board-level hit is generated and transmitted to the ECU. Following the output of a valid hit signal, further hit judgment is inhibited for a 20 μs dead-time window.

TABLE I
ECAL HIT GENERATION CONFIGURATION

Working Mode	Hit Logic	Energy Threshold
MIPs Trigger (logic-1)[1]	Logical OR of FEE-2 and FEE-4 channels	0.3 MIP[3]
MIPs Trigger (logic-2)[2]	Two-layer coincidence in both FEE-2 and FEE-4	0.09 MIP
Gamma Trigger	Logical OR of FEE-1 and FEE-3 channels	0.045 MIP
Unbiased Trigger	Logical OR of FEE-1 and FEE-3 channels	0.015 MIP

[1] For longitudinal particle incidence.
[2] For Transverse particle incidence.
[3] One minimum ionizing particle (MIP) is defined as depositing 120 MeV of energy.

C. Calibration Circuits

To monitor the in-orbit performance of the electronics and calibrate the gain and linearity of the CSA, a charge injection calibration circuit is implemented. As illustrated in Fig. 8, the

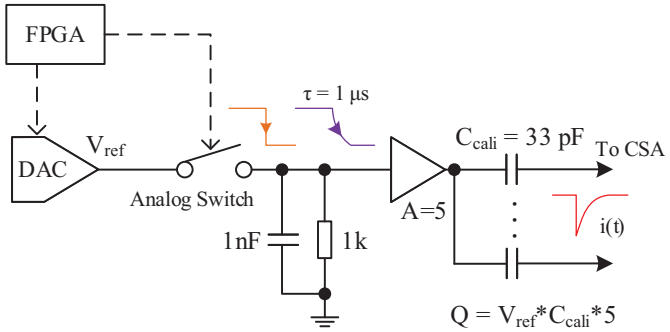


Fig. 8. The schematic diagram of the calibration circuit.

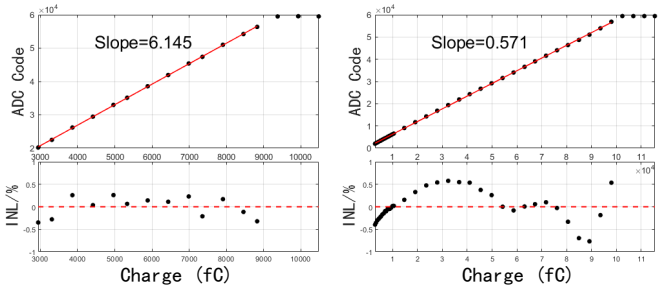


Fig. 9. The calibration curves for the high-gain channel (left) and low-gain channel (right) of an APD.

calibration circuit comprises a DAC, an analog switch, and an RC shaping network.

In calibration mode, the analog switch is normally closed. Upon receiving an external trigger signal, the switch opens to generate a falling step pulse, which is subsequently converted into an exponentially decaying waveform by the RC network. After amplification, this signal is injected into the CSA input as a current pulse through a 33 pF capacitor. The RC shaping network preserves the total amount of injected charge, modifying only the temporal distribution of the current pulse to approximate the actual current pulse characteristics of the detector output.

By adjusting the DAC output value to generate current calibration pulses with varying amounts of injected charge, the calibration curves for all PAM channels are obtained. Fig. 9 displays the calibration curves for the high and low-gain readout channels of an APD. The high-gain channel exhibits a linear range of 0 to 900 fC, a calibration gain of approximately 6.145 ADC code/fC, and an integral non-linearity (INL) of less than 0.5%. Conversely, the low-gain channel features a linear range of 0 to 100 pC, a calibration gain of approximately 0.571 ADC code/fC, and an INL of less than 0.8%.

D. Monitoring Circuits

Each FEE incorporates two current monitoring channels, designated for monitoring the +1.8 V supply current of the AD9266 ADC and a specific power current of the PAM. As illustrated in Fig. 13, within the primary electronics subsystem, FEE-1 monitors the +5 V supply current of the primary PAM electronics, while FEE-3 monitors the -5 V supply current. The current monitoring circuit consists of sample resistors, operational amplifiers, and a multi-channel ADC shared with the temperature monitoring system.

Each FEE utilizes four thermistors: two are allocated for measuring the temperatures of the FEE board surface and the FPGA, while the remaining two are dedicated to APD temperature measurement. Consequently, a total of eight APD-monitoring thermistors are uniformly distributed across the readout electronics surface beneath 8 out of the 25 crystals, capturing the spatial temperature distribution of the APDs on the PAM.

In addition to current and temperature telemetry, the operational status parameters within the FPGA logic are also reported. The ECU queries the FEE once per second, and a total of 59 bytes of telemetry data, comprising the current values, temperature readings, and status parameters, are transmitted to the ECU via an RS-422-based command/status interface.

V. Radiation Protection

VLAST-P will operate in a low Earth orbit (LEO) at an altitude of approximately 500 km. Therefore, the electronics design must account for three categories of radiation effects: total ionizing dose (TID), single-event upset (SEU), and single-event latch-up (SEL).

A. TID Protection

To ensure a sufficient radiation design margin (RDM), the TID design specification for the ECAL electronics is set at 20 krad, which is satisfied by most conventional components.

For the industrial grade AD9266 and THS4524 devices being used for their first space application, multiple TID irradiation experiments were conducted at the end of 2025 to evaluate their tolerance. Utilizing a ^{60}Co γ-ray source, the test profile comprised an initial 10 krad dose, an intermediate annealing process, and a subsequent exposure exceeding 30 krad, with a dose rate of 5 krad/h and a non-uniformity of less than 10%. The results show that the electrical performance and supply currents of both devices remained stable.

Additionally, the detector mass provides inherent radiation shielding across 2π solid angles, while the system enclosures and satellite support structures offer favorable shielding conditions for TID protection.

B. SEU Mitigation Design for the FPGA

SEU mitigation measures have been comprehensively integrated into the sequential logic and storage structures. The FPGA employed is the Flash-based ProASIC 3L series A3PE3000L from Actel. This FPGA utilizes a floating-gate structure to store configuration information for logic cells, inherently offering high immunity to SEU [19].

However, the registers and RAM within the logic cells remain susceptible to SEU, where a single-bit error can lead to soft errors or even infinite loop states. As shown in Fig. 10, the FPGA is composed of 9 modules, including scientific data module, reset module, control module, calibration module, status manager module, current monitoring and SEL protection module, trigger receiving module, hit detection module and

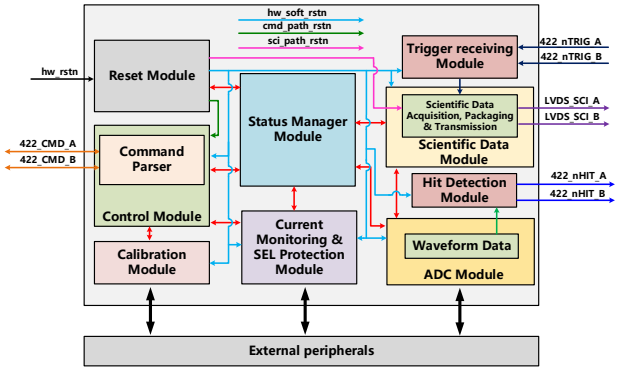


Fig. 10. The schematic diagram of FPGA structure.

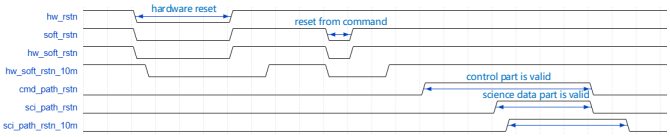


Fig. 11. Multi-domain reset signal. The hw_rstn is the global hardware reset signal; soft_rstn is the global software signal; cmd_path_rstn and sci_path_rstn are used to reset the control part and the scientific data acquisition part respectively.

ADC module. The scientific data module and the control module implement the primary function of the FPGA and rely on external input signals for finite state machine (FSM) state transitions. When a trigger signal from the ECU arrives, the science data module buffers, packs, and transmits the science data packet. When a command from the ECU arrives, the control module verifies the validity of the command, executes it, and provides the corresponding response. Therefore, multi-domain and multi-level reset mechanisms are introduced for these two modules [20]. As shown in Fig. 11, when an external input signal is valid, no reset is applied and the corresponding module begins the process. When these modules are idle or after a process concludes, the corresponding local reset signals remain asserted to hold them in a reset state, thereby minimizing SEU impacts without excessive logic resource consumption.

For other internal FSM, watchdogs are applied to prevent infinite loops. For critical registers and RAM, triple modular redundancy (TMR) is implemented to guarantee data integrity [21], with the three redundant cells manually distributed across distinct physical regions to enhance spatial separation and radiation tolerance. Furthermore, to ensure the integrity of critical register data, their states are continuously monitored online as telemetry parameters. After implementing TMR, the FPGA resource utilization is 75.39%, and the maximum operating speed is approximately 35.656 MHz. These figures satisfy the system derating requirements for both resource usage and clock frequency.

C. SEU Mitigation Design for the AD9266

The configuration registers of the AD9266 are also sensitive to SEU. Testing indicated that at a linear energy transfer (LET) value of 15 MeV $\cdot$ cm^2/mg and a fluence of 10^7 ion/cm^2, 45 SEUs occurred within a 4-minute window.

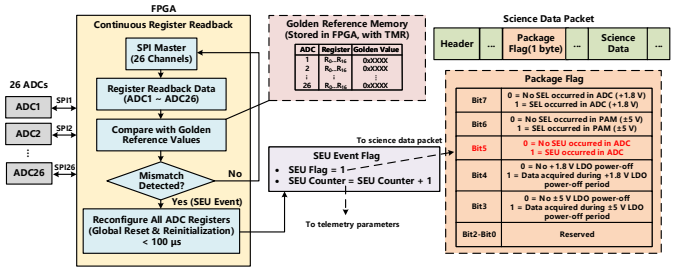


Fig. 12. Schematic of the SEU Mitigation Design for the AD9266.

Therefore, SEU mitigation is also required for the AD9266. As shown in Fig. 12, the register values of each AD9266 are continuously read back and compared to the TMR-protected reference registers within the FPGA to detect SEU and trigger reconfiguration. The entire reconfiguration process is completed within 100 μs. In addition, an ADC SEU flag is embedded into the science data packet to indicate whether an SEU occurred during the acquisition of a specific event. The number of SEU is recorded in an SEU counter and transmitted via telemetry parameters.

D. SEL Protection Design

Although heavy-ion irradiation experiments demonstrated that no SEL occurred in the AD9266 and THS4524 at an LET value of 37.4 MeV $\cdot$ cm^2/mg and a fluence of 10^7 ion/cm^2, SEL protection is still implemented for these critical devices and another industrial-grade operational amplifier, the AD8032. This precaution accounts for their component grades, maiden in-orbit application, and vital roles within the readout electronics.

As illustrated in Fig. 13, the monitoring circuit samples the supply currents of these three chips with a 100 μs period. When any current exceeds its preset threshold (set to 1.5 times the operating current), the FPGA immediately sends a control signal to the corresponding low-dropout (LDO) regulator to cut off the power supply. Specifically, if the current on either the $+5$ V or -5 V rail of the PAM exceeds the threshold, both rails are powered down simultaneously, as both ± 5 V LDO are controlled by FEE-1. Approximately 1 s later, after confirming that the SEL condition has cleared, the FPGA re-enables the power supply.

If three consecutive overcurrent protection events occur within 5 seconds, the readout electronics system is considered faulty. The FPGA then forces the corresponding LDO into a permanent power-off state, pending ground commands for power restoration and threshold adjustment, thereby preventing more severe damage to the circuit. In addition, during science data acquisition, flags indicating the occurrence of an SEL event and the forced power-off are embedded into the current event's science data packet, as indicated by the package flag in Fig. 12. The number of SEL occurrences is also recorded in the telemetry parameters and transmitted.

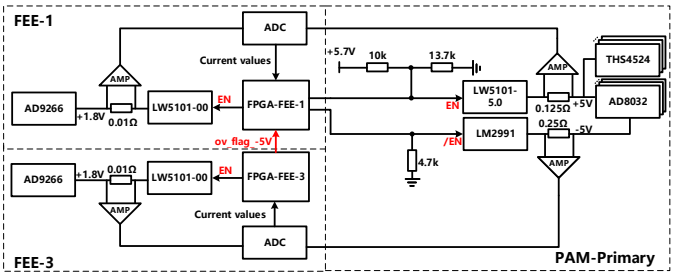


Fig. 13. The schematic diagram of current monitoring and SEL protection circuits.

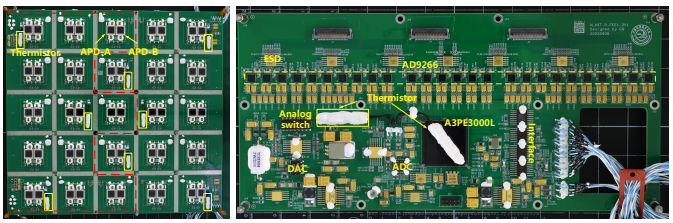


Fig. 14. Photograph of the PAM and FEE modules. (Left) Top view of the PAM. (Right) FEE module.

VI. Challenges and Solutions

The high channel count, wide dynamic range of the detector, and harsh space environment pose significant challenges to the design of the readout electronics.

A. High Integration Level and Low Power Consumption

The payload imposes stringent constraints on the power consumption, mass, and volume of the ECAL. Given the primary/redundant electronics architecture of the ECAL yielding a total of 100 readout channels powered by independent primary and redundant supplies, achieving high integration and low power consumption for the discrete-component-based charge measurement and waveform digitization circuits poses a major challenge.

The PAMs are coupled to the bottom of the crystals, with their primary and redundant readout electronics partitioned on the same PCB to allow independent power distribution. The utilization of multi-channel operational amplifiers and fully differential amplifiers (FDAs) enables a single crystal footprint (3 cm $\times$ 3 cm) to accommodate the dual-gain readout electronics for two APDs. HV is routed to each APD via flying wires to mitigate the impact of high-voltage creepage. Structurally, every two FEEs are stacked within a box located on both sides of the ECAL. Signal transmission between the PAMs and FEEs is implemented via high-density flexible printed circuit (FPC) connectors. Consequently, the FEEs have no direct thermal contact with the internal detector. Furthermore, the low power consumption and uniform heat distribution of the PAMs ensure a more symmetric and homogeneous temperature field within the detector. The ultra-compact footprint of the AD9266 also allows a single FEE board to accommodate 26 ADC chips.

Compared to conventional space-grade ADCs and FDAs, the selection of industrial-grade AD9266 and THS4524 devices substantially lowers the power consumption of the readout electronics. The power consumption is 7 W for the PAM and approximately 4 W for each FEE, leading to a total power consumption of about 23 W for the ECAL readout electronics system, which fully satisfies the system constraint of less than 46 W.

B. High Reliability in Space Environment

To ensure stable operation in the harsh space environment, the electronics must possess robust radiation tolerance alongside sound thermal design and control. Thermal simulations were performed on the ECAL to verify that all components operate stably within safe temperature limits. Furthermore, single-event effect (SEE) and TID tests were conducted on the industrial-grade AD9266 and THS4524 devices making their maiden flight. Based on the experimental results, multiple SEU and SEL mitigation strategies were implemented.

System-level hot redundancy within the readout electronics equips each crystal with two independent electronics subsystems for dual readout, substantially enhancing both system and data reliability. Moreover, a dual-channel hot-redundancy configuration is applied to all power supply cables and interface circuits connecting to the ECU, further bolstering system reliability and fault tolerance.

Additionally, the FEE adheres to relevant aerospace electronic design standards, incorporating ESD protection, electromagnetic compatibility (EMC) design, and Grade 1 derating design, to guarantee long-term operational reliability.

VII. Mass Production and Integration

A. Mass Production and Electronics Tests

The flight model of the ECAL was assembled in the first half of 2026. All FEEs and PAMs underwent stringent board-level testing procedures and successfully passed environmental stress screening (ESS) tests, which comprised 18 thermal cycles from -45°C to +75°C under ambient pressure.

Fig. 14 shows photographs of the PAM and FEE-1. The readout electronics components for the APDs are all populated on the backside. Specifically, the PAM readout electronics for the 13 crystals on the left are connected to FEE-1 and FEE-2, whereas those for the 12 crystals on the right are connected to FEE-3 and FEE-4. Following the installation of the PAM and FEEs onto the ECAL, the flight model (as shown on the left of Fig. 15) underwent a comprehensive series of subsystem-level environmental tests, including thermal cycling, high-temperature burn-in, thermal vacuum, vibration, Electromagnetic Compatibility (EMC), and magnetic tests. Subsequently, the integrated assembly was configured (as shown on the right of Fig. 15) to conduct a series of system-level integration tests. The results demonstrate that the ECAL is fully compatible with other satellite subsystems, and both the FEEs and PAM operate reliably within the required operational temperature range in space.

Under normal operating conditions for all subsystems, the baseline of the ECAL was acquired without any signal input. As shown in Fig. 16, the results indicate that the ENC is less than 4 fC for the high-gain channels and less than 14 fC for the

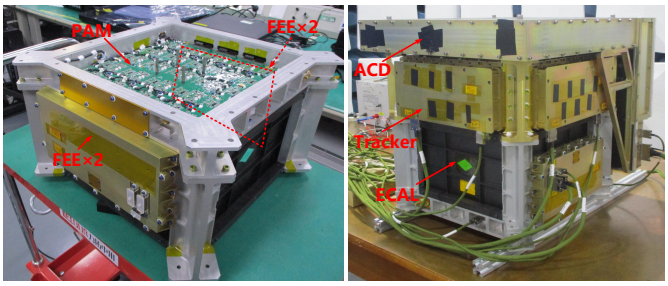


Fig. 15. Photograph of assembled flight models. (Left) Inverted view of the ECAL flight model. (Right) Integrated flight model of the VLAST-P payload.

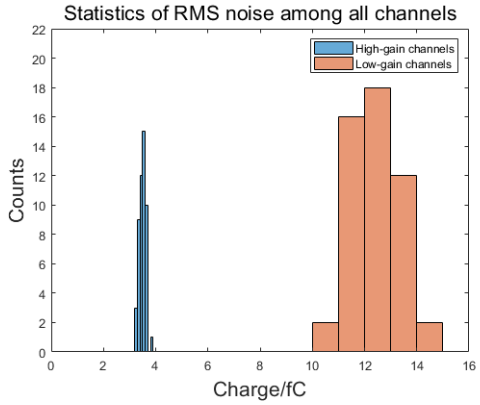
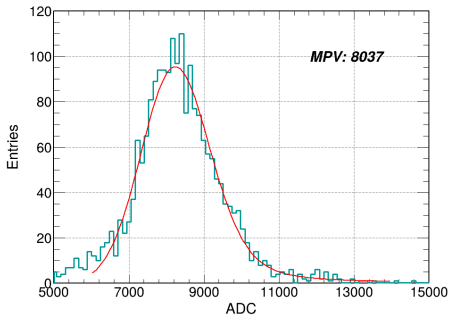
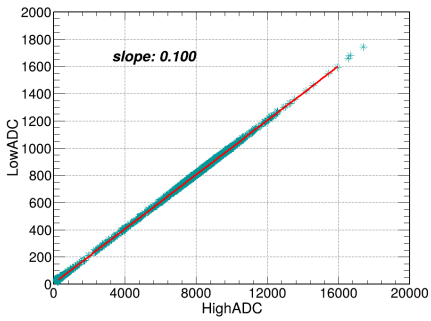


Fig. 16. Noise measurement results of all channels.



(a)



(b)

Fig. 17. Cosmic-ray test results of the high-gain channel for the primary APD of a representative crystal. (a) A typical MIPs distribution from a detector unit. (b) The linear fitting results between high and low-gain channels.

low-gain channels. Notably, the ENC of the high-gain channels is well below the ECAL threshold for a 0.015 MIP signal (21 fC), thereby fully complying with the design specifications.

B. Cosmic Ray Test

The ECU issues trigger signals based on the hit information provided by the three sub-detectors under the MIP trigger logic 1 mode to conduct cosmic ray tests. Fig. 17 illustrates the cosmic ray test results of the high-gain channel for the primary APD of a representative crystal. The MIP signal corresponds to an input charge of approximately 1308 fC. Consequently, the equivalent noise energy (ENE) of the high-gain channel is approximately 0.33 MeV, and the upper limit of the energy measurement for the low-gain channel can reach 9.2 GeV. Furthermore, an excellent linearity is maintained between the high- and low-gain channels, fully satisfying the ECAL dynamic range requirement of 1.8 MeV to 4.1 GeV for a single crystal.

VIII. Conclusion

This paper presents the design and implementation of a wide-dynamic-range, low-power, low-noise, and radiation-tolerant readout electronics system for the ECAL of VLAST-P. The system comprises one PAM and four FEE modules, with a total power consumption of 23 W. It achieves a dynamic range of up to 9.2 GeV (with a corresponding charge upper limit of 100 pC) per detector unit, an ENC of less than 4 fC for the high-gain channels, and an ENE down to 0.33 MeV. Key aerospace engineering considerations, including thermal design, radiation tolerance, and quality control, were thoroughly addressed during the engineering implementation. ^{60}Co irradiation testing confirmed that the system possesses a TID tolerance exceeding 30 krad (Si), while a series of radiation hardening measures effectively mitigate the potential hazards of SEL and SEU. Currently, the electronics system has successfully passed a suite of space-grade ground environmental tests and operates compatibly with other subsystems in satellite-level integration tests. The VLAST-P payload is scheduled for launch in 2026.

In conclusion, the developed readout electronics system exhibits excellent linearity, low noise levels, and high reliability, aligning well with design expectations and satisfying the requirements of physics experiments. This work lays a solid and reliable technical foundation for the future VLAST mission.

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