Evaluation of Real-Time FPGA-Based Thomson Scattering Diagnostic with Diagnostic-to-Interlock Communication For Enhanced Operational Flexibility at ASDEX Upgrade

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Outline

1. Motivation and Background

- ASDEX Upgrade Thomson Scattering Diagnostic

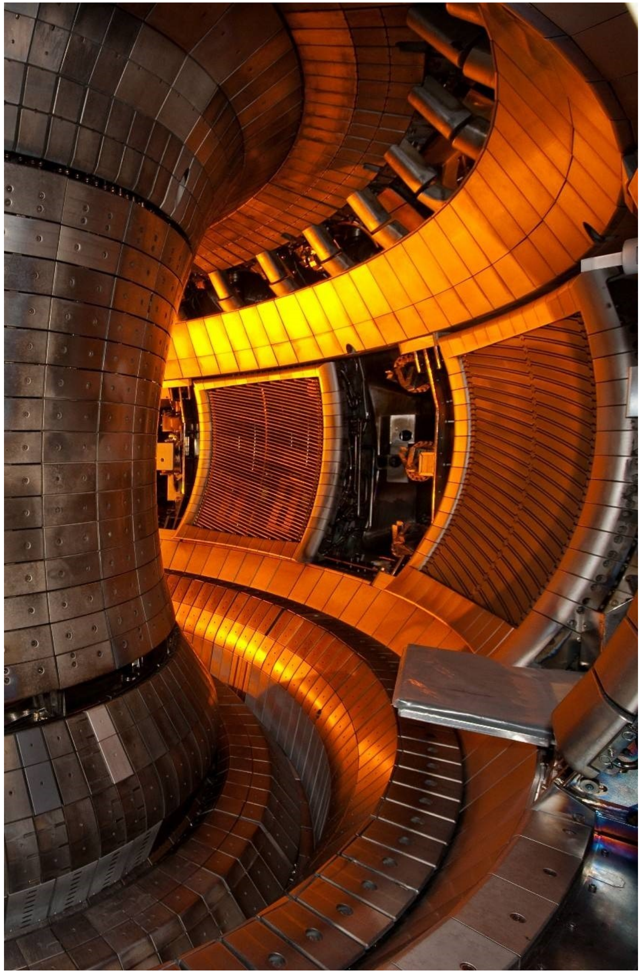
2. Work Objectives

- Device overview

3. Implementation

- Interface with the Proprietary Data bus Interface of HLS solution
- HLS implementation of the real-time Thomson scattering signal evaluation
- HLS implementation of the decision module for interlock
- DCS integration

4. Results
5. Conclusions



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MOTIVATION

- In a **tokamak**, the safe operation of plasma heating systems depends on monitoring the plasma state.

A key example:

ASDEX Upgrade (AUG) **Neutral Beam Injection (NBI)** works by firing high-energy neutral atoms into the plasma to transfer energy.

In low-electron-density plasma the beam passes through without being absorbed. It can damage the tokamak wall.

The control system cuts the beam when density drops below a threshold. **Today that threshold is conservative.**

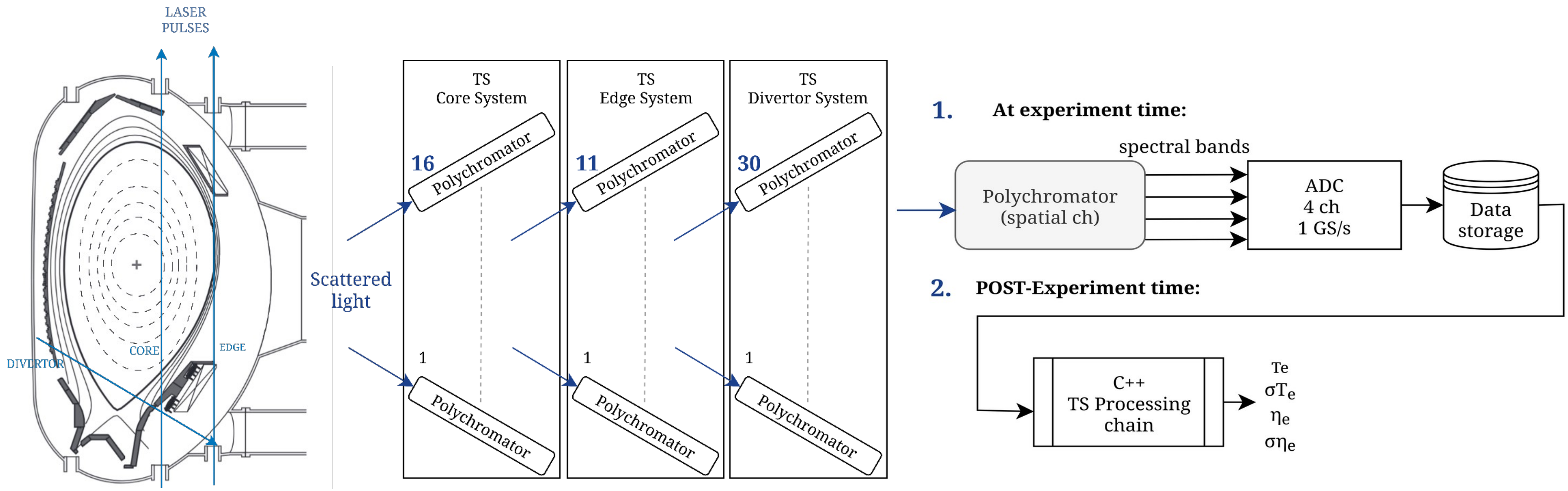
The beam is cut more often than necessary. This results in a considerable loss of experimental time, reduced heating efficiency, and fewer shots per campaign. **The root cause:** the current density measurement system is not qualified for interlock use.

Goal: a plasma electron density measurement that is valid, accurate and bounded in time.

AUG THOMSON SCATTERING DIAGNOSTIC

- At ASDEX Upgrade, Thomson scattering diagnostic (TS) provides local electron density (η_e) and temperature (T_e) profiles with high spatial resolution. Signal evaluation is performed offline

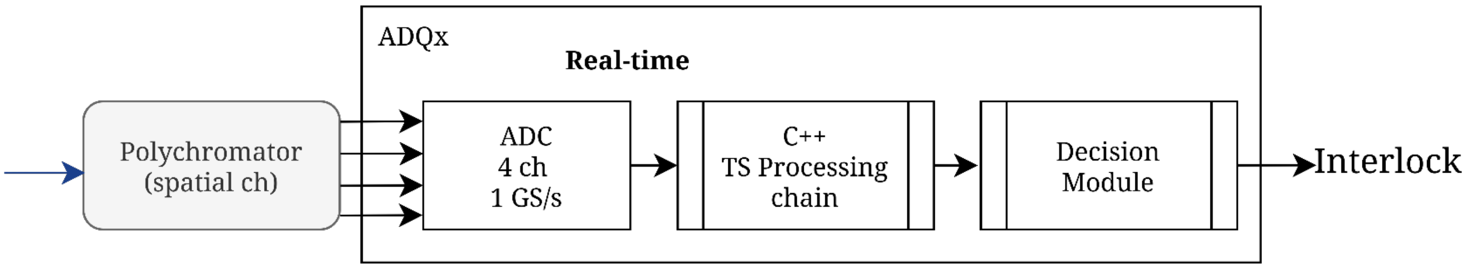
Diagnostic data acquisition



OBJECTIVE

- Evaluate the feasibility of migrating the AUG TS processing chain to a real-time FPGA-based implementation, to assess whether the resulting system can serve as a reliable source for the interlock.

- Based on:
  - Teledyne SP Devices ADQ3x.[1]



  - HLS implementation for the data analysis.

1. Teledyne SP Devices, “**Datasheet adq32**”, Jun. 2025. [Online]. Available: https://www.spdevices.com/en-us/Products_/Documents/ADQ32/20-2378%20ADQ32%20datasheet.pdf

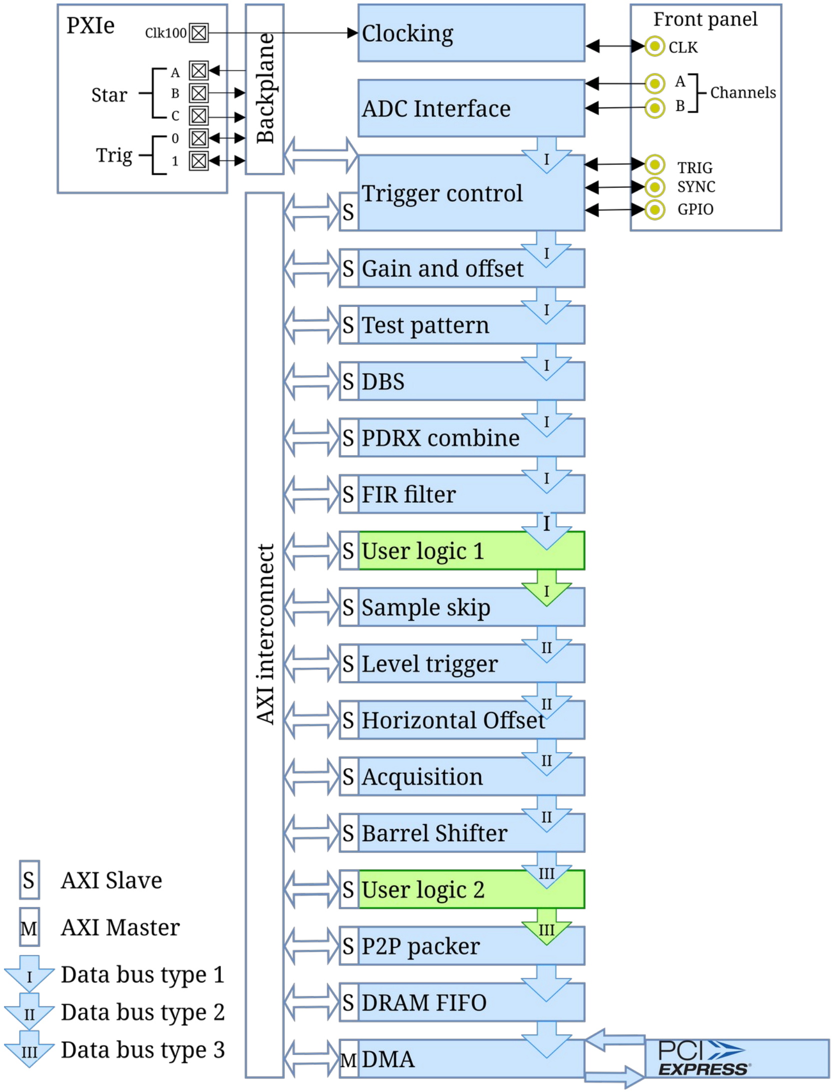
TARGET DEVICE

- The ADQ3x runs **FWDAQ**, which implements the complete acquisition data path.

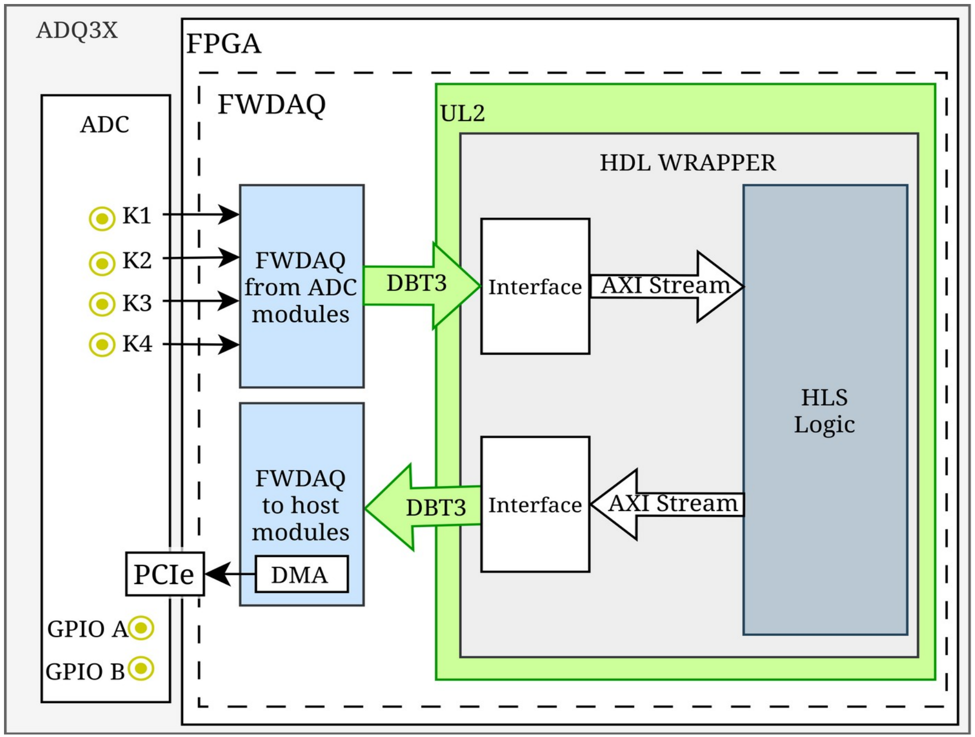
- **User Logic 1** operates on the continuous stream at the full ADC rate.
- **User Logic 2** operates after the record framing and data reduction.

- Data records arrive at UL2 over a data bus defined by the manufacturer (**DBT3**).

- To preserve the HLS abstraction level, data must be presented as AXI4-Stream.



IMPLEMENTATION I: INTERFACE WITH DBT3

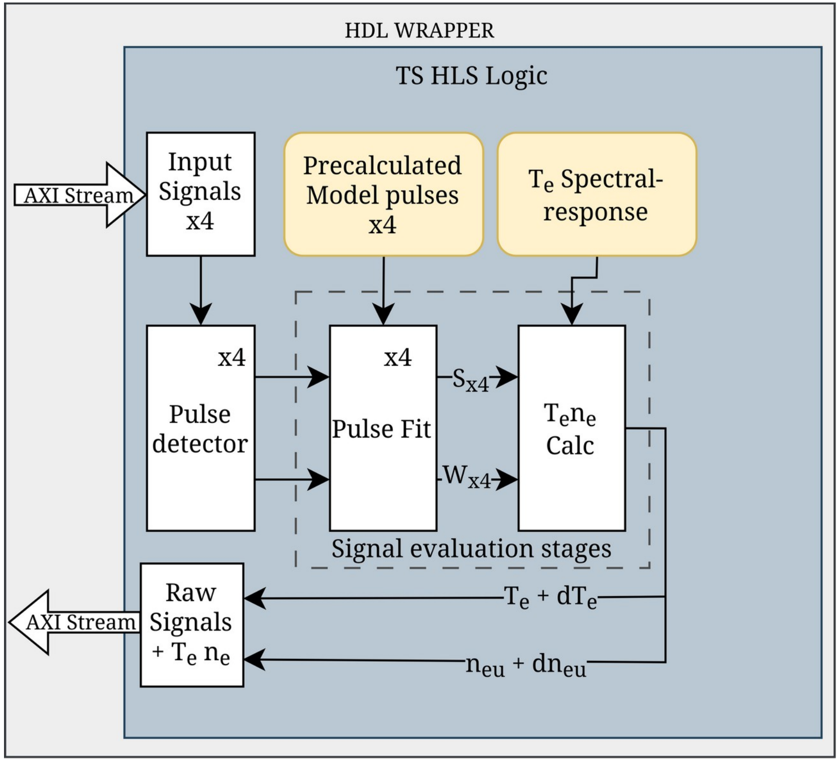


- Development of the HDL wrapper to access the proprietary DBT3 bus and bridge to AXI4-Stream.
- This enables an easy integration of the HLS implementation.

IMPLEMENTATION II: HLS TS SIGNAL EVALUATION

- The ADQ3x digitizes the 4 spectral band signals from a polychromator. These ADC records enter the HLS signal evaluation chain.

- HLS Kernels solving:
  - Pulse detection: locates the scattering pulse withing each signal.
  - Pulse Fit: compares each pulse with pre-computed model pulses. Determines scaling factor and its variance for each of the 4 bands.
  - The four scaling factors are compared against pre-computed spectral responses to find the best fit T_e. η_e is then determined analytically.



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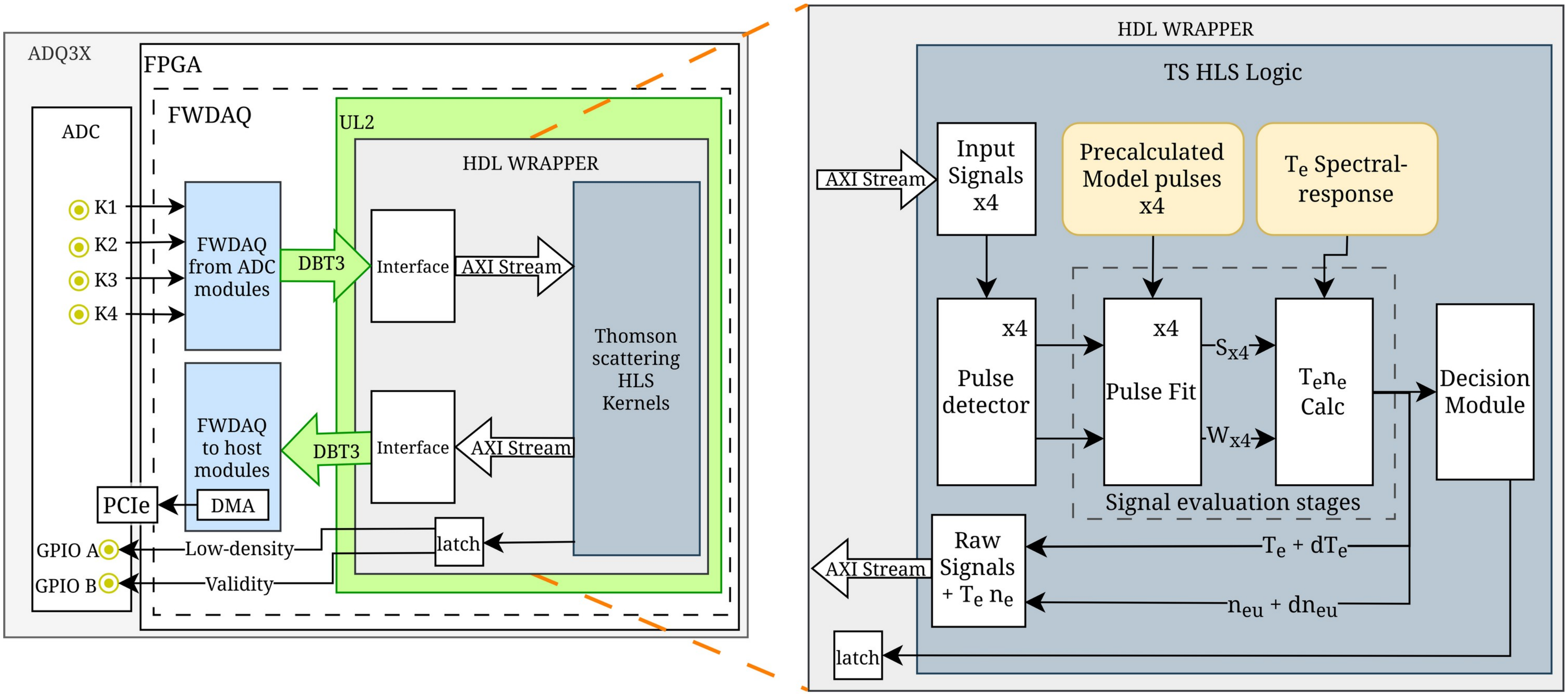
IMPLEMENTATION III: DECISION MODULE

- Receives the outputs of the evaluation chain and classifies each measurement into a validity state, producing an action that is delivered to the interlock system.

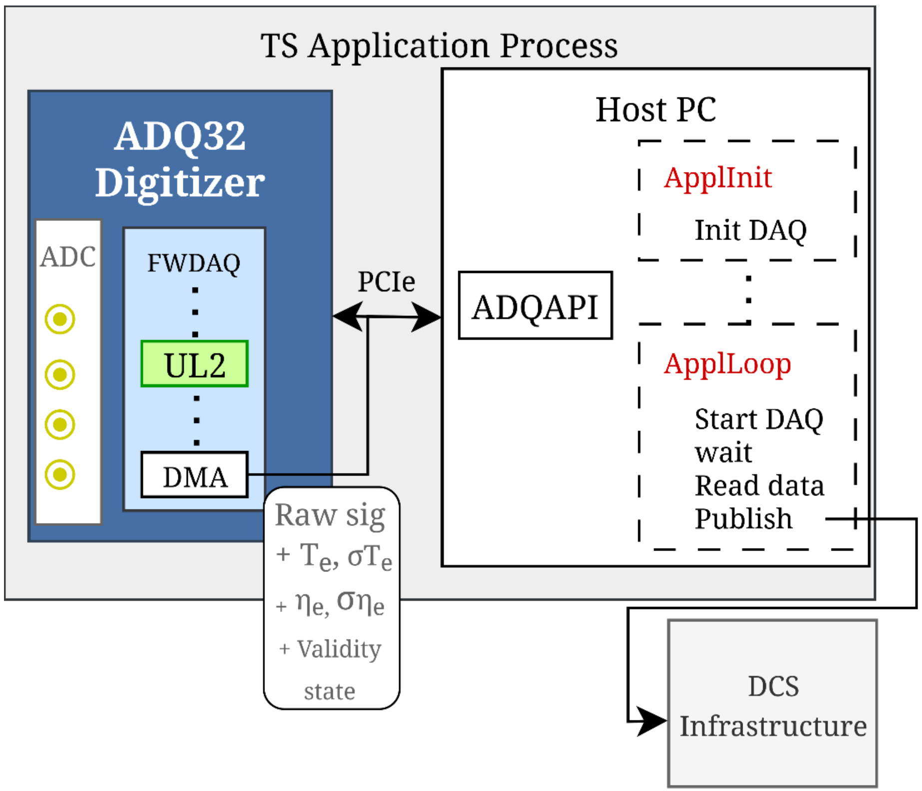
Pri.	State	Condition	Action
1	**PULSE NOT FOUND**	No TS pulse detected	INHIBIT
2	**FIT FAILED**	T_e or uncertainty are negative	INHIBIT
3	**UNRELIABLE**	T_e and/or η_e uncertainty are too high	INHIBIT
4	**LOW-DENSITY**	Valid measurement, η_e below interlock limit	TRIP
5	**DENSITY VALID**	η_e above threshold, measurement qualified	PASS

TRIP = density is genuinely low (physical condition) - **INHIBIT** = measurement is unreliable (diagnostic condition)

IMPLEMENTATION IV: FPGA HARDWARE



IMPLEMENTATION V: INTEGRATION IN AUG DCS

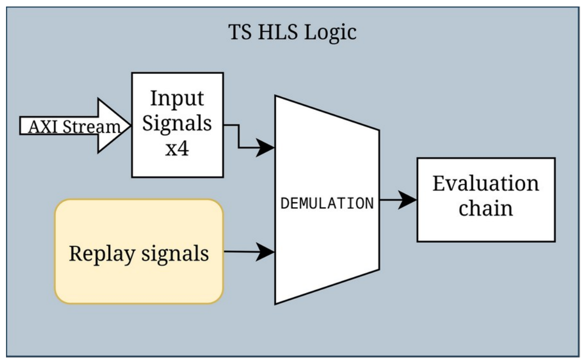


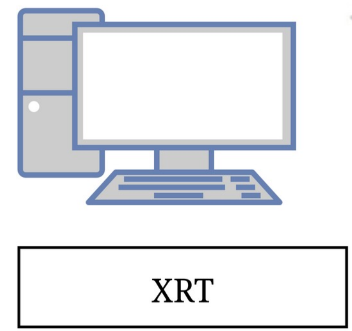
- A Discharge Control System (**DCS**) Application Process was developed to integrate the ADQ32 into the AUG control system.
- It communicates with the device via PCIe using the Teledyne **ADQAPI** library.
- It publishes raw signals, TS results, and validity state to the DCS infrastructure for each laser pulse.

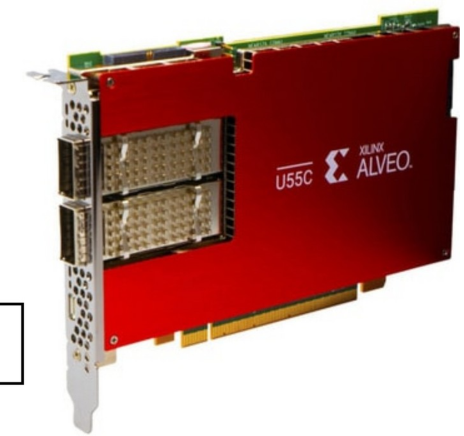
VALIDATION METHODOLOGY

- System validation was performed in two stages

1. **Portability verification:** the same HLS implementation was executed on both, the Alveo, and the ADQ3* with identical input signals. Results were identical on both platforms.







2. **Algorithm accuracy:** once portability was confirmed, 78 pulses form the 16 polychromators of the core system corresponding to shot #33712 were processed in the Alveo and compared with the offline reference chain.

RESULTS

Signal evaluation accuracy

+0.75%	T_e median relative deviation
−1.31%	η_e median relative deviation
0.998	Pearson r — both T_e and η_e

Processing latency

25.73 µs

deterministic · 8 042 clock cycles @ 312.5 MHz

FPGA resource utilization

LUT	**67.6%**	38.4%* + 29.2%
FF	**53.5%**	33.8%* + 19.7%
BRAM	**30.8%**	29.4%* + 1.4%
DSP	**23.8%**	9.8%* + 14.0%

Kintex UltraScale xcku040

* FWDAQ base utilization

CONCLUSIONS

- **AUG TS evaluation chain has been migrated to a real-time FPGA implementation**, validated against the existing offline processing chain with acceptable median relative deviation.
- **25.73 µs** total processing time confirms the bounded-latency operation. It is fast and predictable enough to serve as a reliable protection actuator for plasma heating systems.
- The decision module classifies each measurement into one of five validity states, **allowing the protection system** to distinguish between a genuinely low-density and a missing or unreliable measurement.
- The interlock signal is latched on the GPIO and transmitted to the interlock system without host intervention, keeping **the protection path independent of the software infrastructure**.

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Thank you for your attention

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