



# Status and testing of the MDT Trigger Processor for the ATLAS Level-0 Muon Trigger at HL-LHC

Rimsky Rojas (CERN) on behalf of the ATLAS collaboration  
25th IEEE Real Time Conference - Isola d'Elba May, 2026

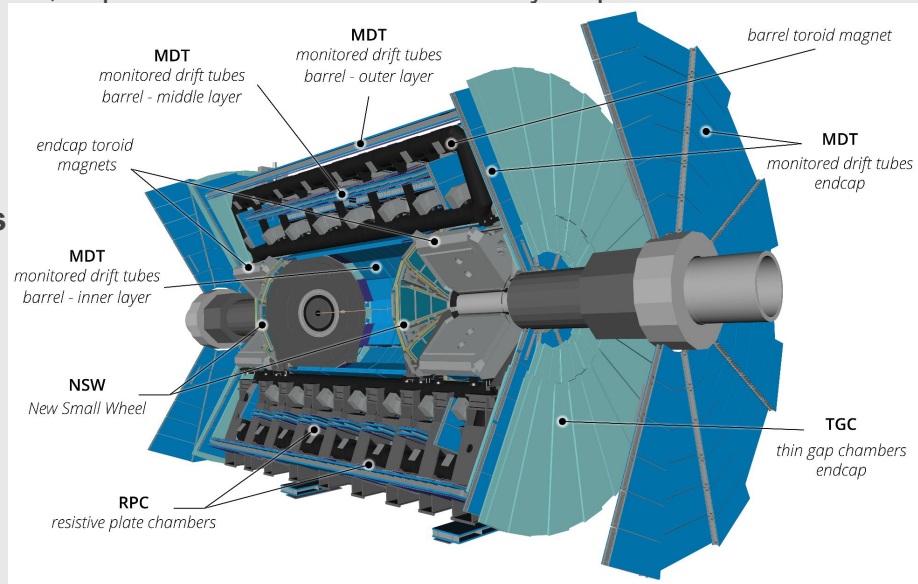


# Introduction to ATLAS MDT

The MDT Trigger Processor (MDT-TP) is a critical component of the ATLAS L0 Muon Trigger upgrade for the HL-LHC. It integrates Monitored Drift Tube (MDT) detectors directly into the Level-0 trigger logic to improve muon  $p_T$  resolution, reduce fake trigger rates, and enhance capability for high pile-up. Moreover, its large FPGA enables the use of ML algorithm for possibly enhancing robustness, improve resolution and/or identify displaced muon signatures.

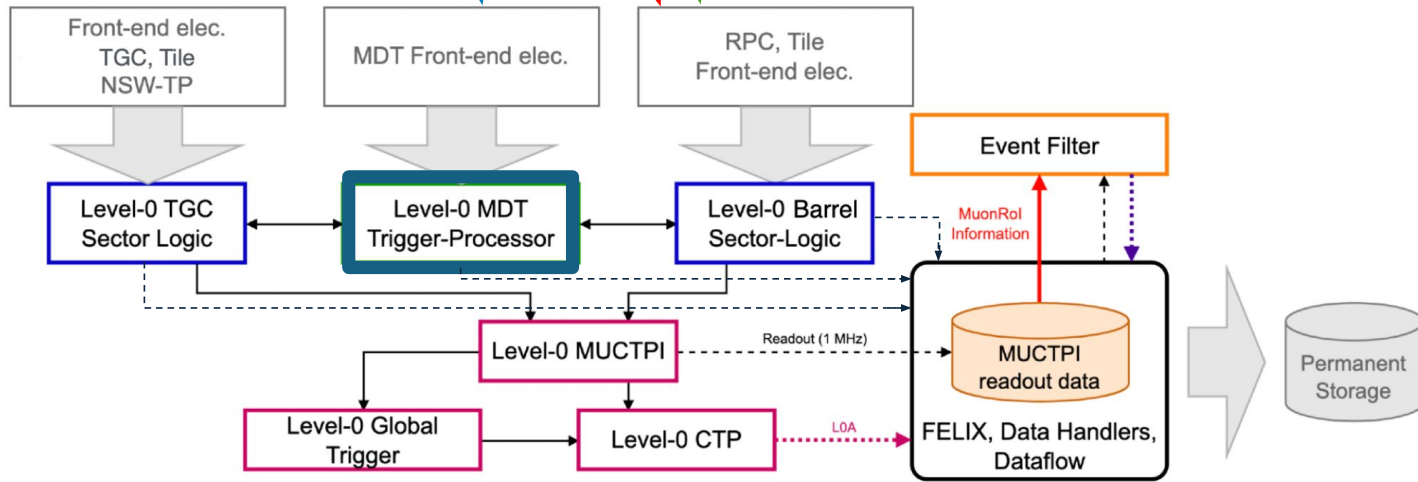
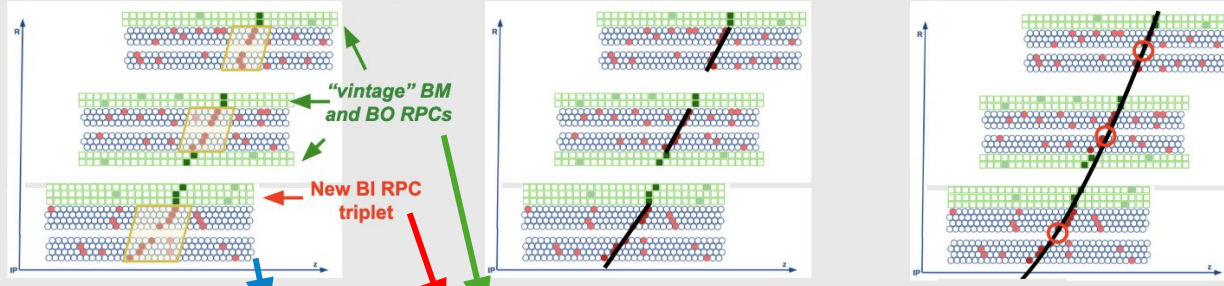
- **Based on the Apollo-LHC platform.** ATCA blade composed of a Service Module + Command Module.
- **It is the only communication path to front-end electronics** Thus, it configures, monitor and readout the FE. Enables the use of Machine Learning algorithms (displaced muon ID, improved  $p_T$  estimation).
- Prototypes are functional. Command Module v3 is under testing. **Target production: Late 2026.**

see [Niklas' talk](#) about ATLAS



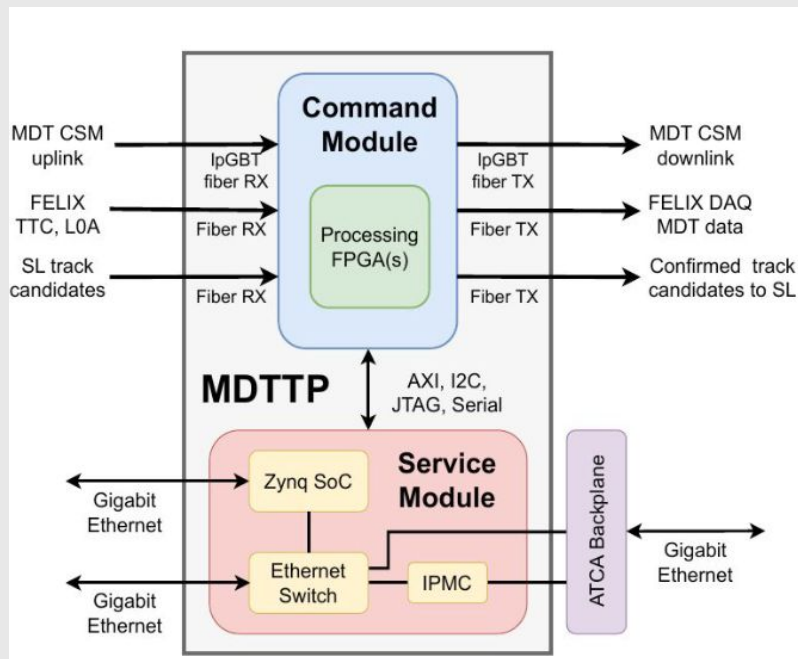
# Introduction to the MDT Trigger Processor

ATLAS Muon Barrel layout



DAQ path for the MDTs is also handled by the MDT Trigger Processor

# Hardware Overview

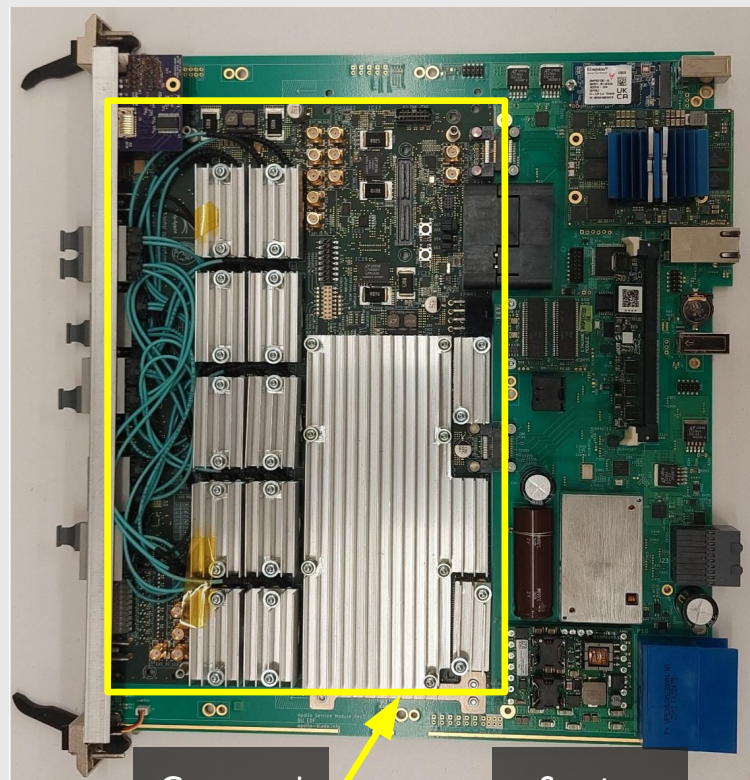


- All interfaces independently tested and working
- Hardware in pre-production stage - firmware development in parallel

28/05/2026

MDT-TP Status and testing

SM rev3 + CM prototype v1



Command Module

Service Module

Apollo platform



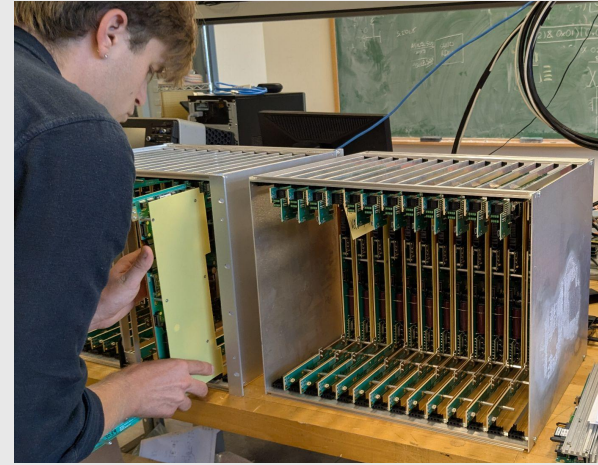
Apollo is Used in ATLAS & CMS

# Service Module pre-Production

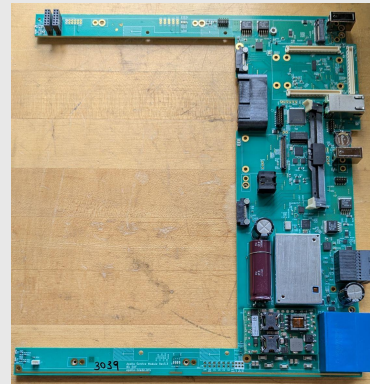
Produced and tested the SM pre-production boards rev3 received in June, tested in July and August 2025

- Designed and produced a dummy CM to test the SMs comprehensively prior to installing the final CMs
- Developed firmware and software for testing
  - Increasingly automating testing procedures
- Testing program includes
  - Inspection, power tests
  - Installation and programming of devices
  - IPMC, Zynq testing
  - Link loopback tests
  - Full power load testing
  - etc.
- 13 SM shipped to CERN for further testing with CM and to develop the networking strategy.
- Looking for a 2nd pre-Production with another PCB Manufacturer.

Tested boards in Massachusetts



Pre-production SM

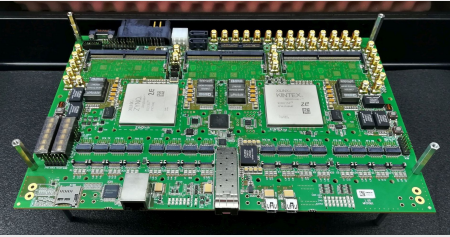


6 pre-prod. SM at CERN

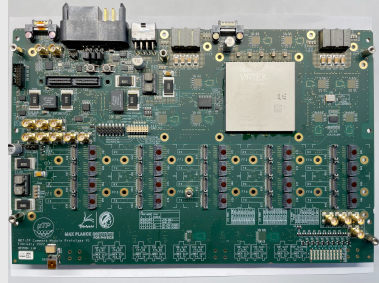


# MDT Trigger Processor Timeline - Command Module

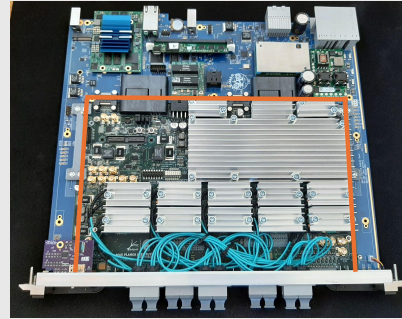
demonstrator CM  
*fabricated 2020*



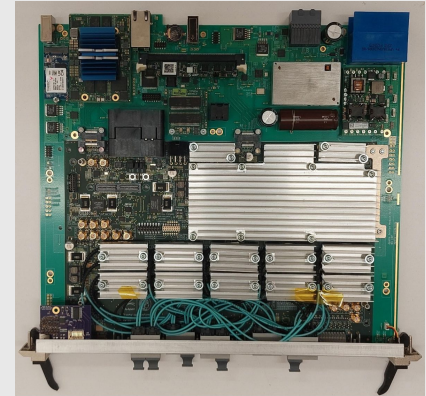
prototype v1 CM  
*fabricated 2022 & 2023*



prototype v2 CM  
*fabricated 2024 & 2025*



prototype v3 CM  
*April 2026*



Many changes between demonstrator and prototype v1

Simplified design with single large **Xilinx UltraScale+  
FPGA VUI3P**

Removed unused features (DDR4 memory, etc)

Single type of FireFly module capable of 14-16 Gbps

Simple and universal clocking scheme

Optimized cooling

Prototype v2 implements  
over-voltage/under-voltage and  
over-current **protections**, as well as a  
**few hardware configuration  
changes**  
(outcome of FDR)

Prototype v3 with an  
updated temperature  
sensor to fully validate  
the final layout

Small hardware changes in prototype versions

Tender for the (pre-)production CM earned by Prodesign - same company as prototypes

**All FPGAs and FireFly purchased and already safely stored at CERN.**

# Command Module testing

## PCB quality tested by PCB manufacturer:

- Electrical open/short test.
- Impedance control.
- D-Coupon test according to IPC-2221 and IPC TM-650.
- Thermal shock testing of board after soldering.
  - 0 .. 80 °C shock with high gradient.
  - Detailed inspection of ~ 40 representative solder joints.

## Tests performed by manufacturer

- Detailed electrical tests
- Essential: Power, I2C, buttons, LEDs
- Connections: Connections to all peripherals.
- MCU: HW test firmware used for testing.
- FPGA operation
- Optical connections: BER < 10<sup>-14</sup> at 14 Gbps
- Tested with loopback fibers
- Basic tuning of transceivers to achieve required BER.

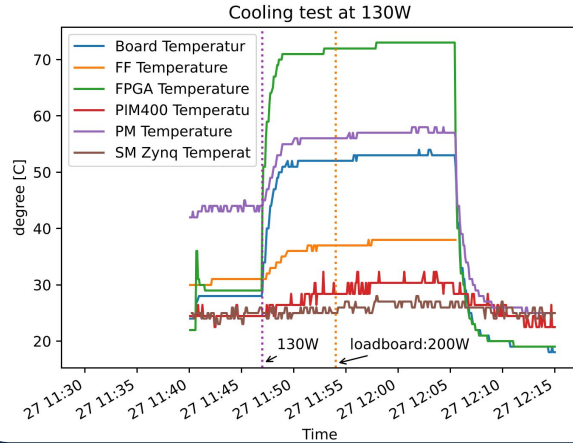
## Integration tests at CERN

Repeat some basic tests from manufacturer.

- Test connection with SM.
- Cooling test
- Fully automated test stand to exercise CM with production FW.
- Documentation
  - Database
  - Naming: Number from Pro Design, serial number, etc.

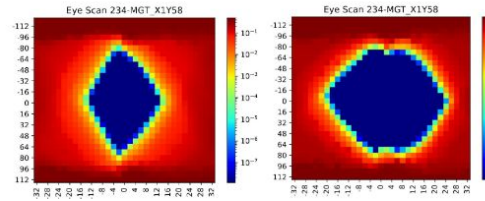
# Hardware: basic tests on full blade (SMrev3 + CMv1)

## Stress test



## Loopback IBERT tuning

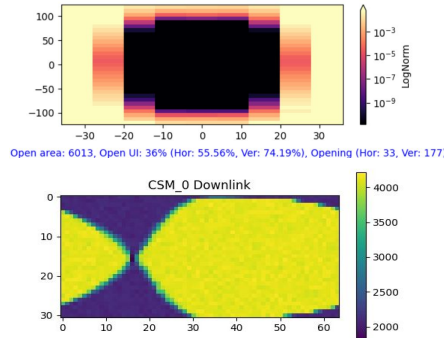
Default Improved parameters



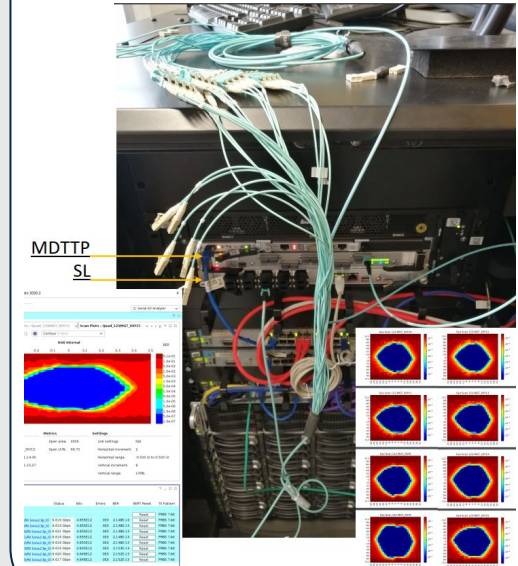
## FELIX connections

```
Link alignment status
Channel | 0 1 2 3 4 5 6 7 8 9 10 11
-----|-----
Aligned | NO NO NO NO NO NO NO NO YES YES YES YES
Channel | 12 13 14 15 16 17 18 19 20 21 22 23
-----|-----
Aligned | YES NO NO NO NO NO NO NO NO NO NO NO
pcat@lnswfelix02:~/afs/cern.ch/user/p/pgkounto
$
```

## MDTTP-CSM eyescans



## MDTTP-SL IBERT



# Chamber Service Module + FE / DAQ + Felix

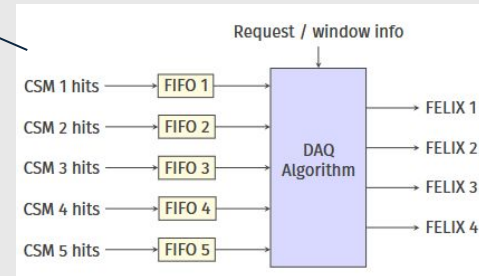
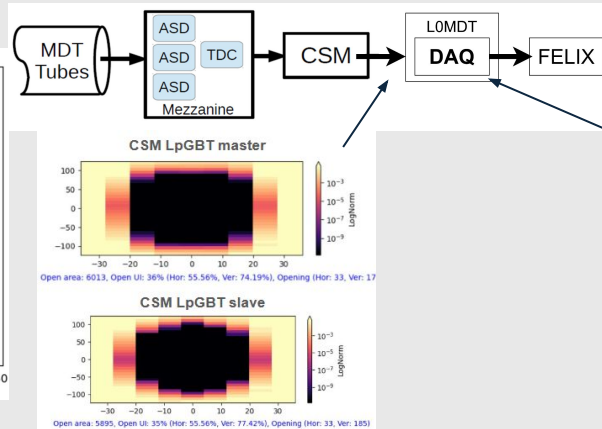
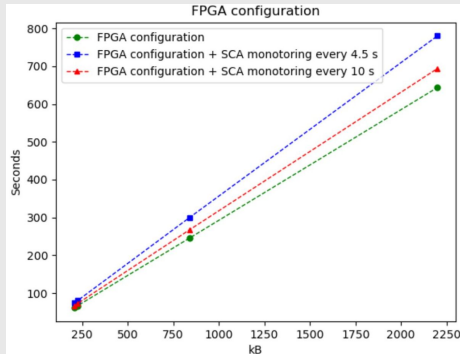
We have extensively tested the communication with the FEs by using individual scripts for configuration and monitoring CSM firmware download exercised as well. correct TDC hit extraction also verified Online eye scan

Felix communication exercised:

- using fixed pattern generation and fullmode protocol
- using a pass-through mode from TDC to FELIX using fullmode (muon events filtered using a scintillator)

TTC signals from Felix verified at FPGA

Currently integrating L0A readout test using spy buffer injecting simulated readout data.

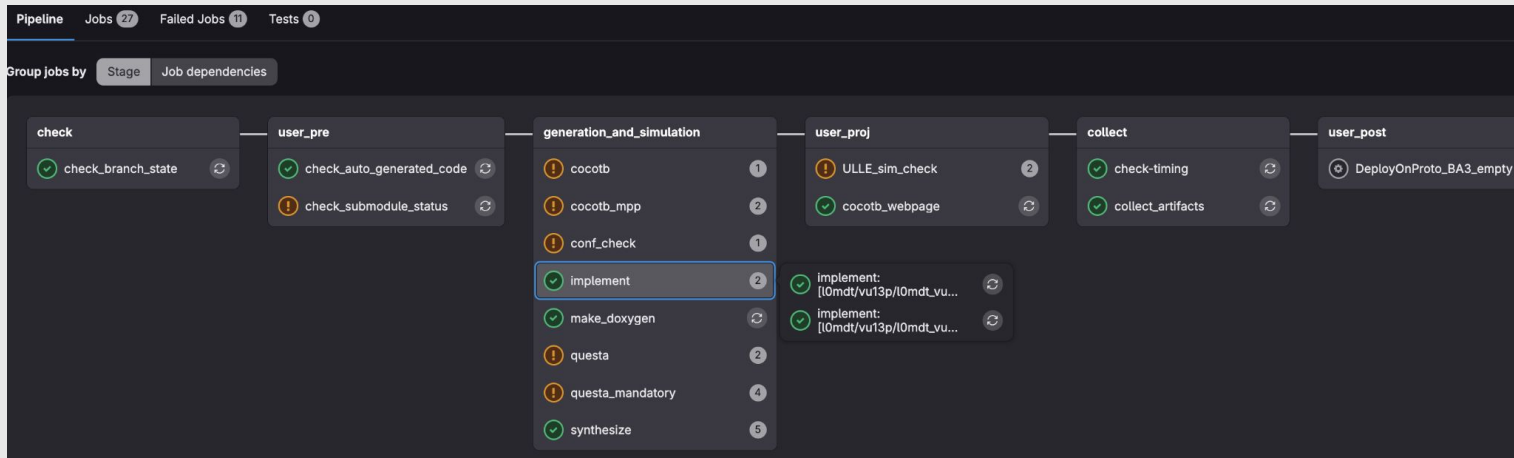


# Gateway validation

The logic blocks of the MDT-TP gateway are currently under debugging and validation, based on input events obtained from the Phase-II ATLAS simulation.

**The Continuous Integration pipeline** includes VHDL and cocotb testbenches, synthesis and implementation, and timing checks for several project configuration relying on **HDL-on-git (Hog)**. **Validation** is performed directly **on hardware**.

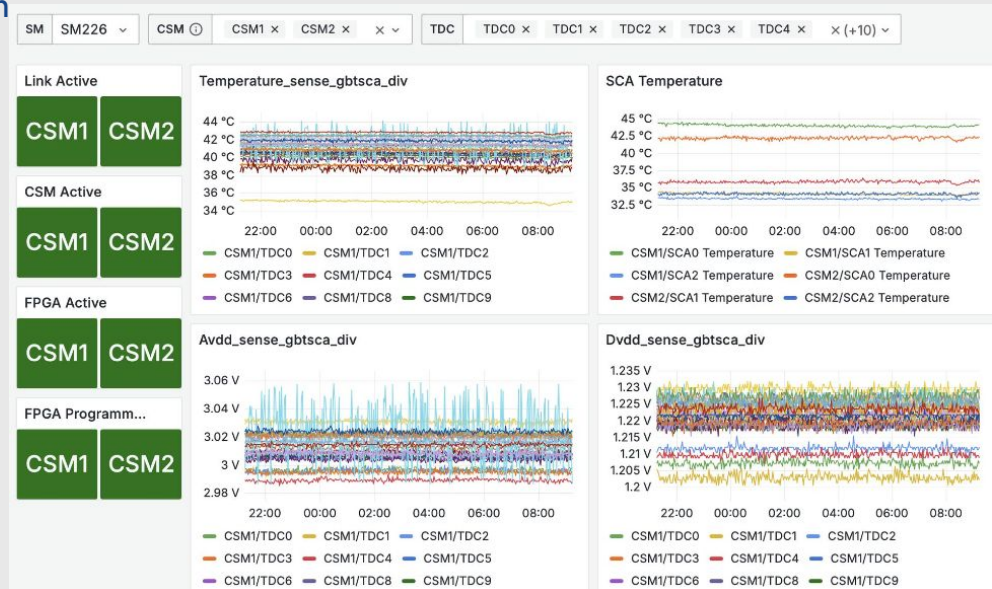
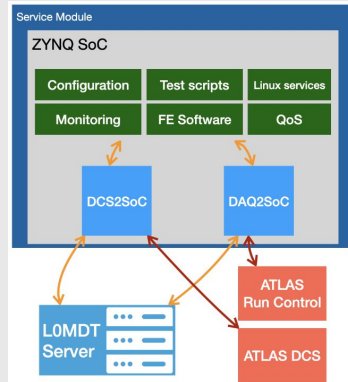
Further validation of some blocks is done using Fast Monitoring, relying on SpyBuffers that can inject and read data between different gateway blocks, allowing injection of more realistic data for a complete validation.



# Software

Software for commissioning and operations has been developed and tested:

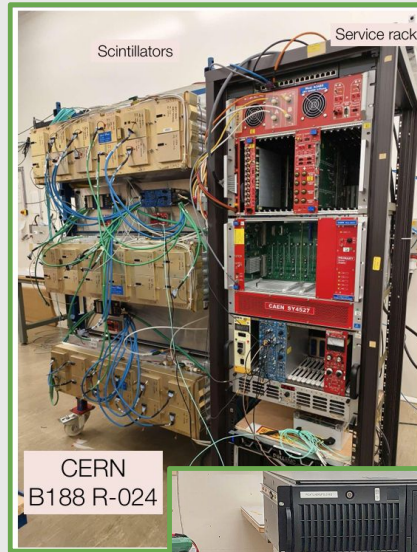
- **Apollo software:** provides dynamic load of the CM AXI Chip-Chip endpoint via xml files.
- **Dedicated I0mdt core software:** configure and monitoring of the CM hardware.
- **DAQ2SoC:** Software that will interact with ATLAS run control
- **DCS2SoC:** OPC server for the ATLAS Detector Control System. (Monitoring)
- **Maestro:** dedicated UI software to test the above list during commissioning



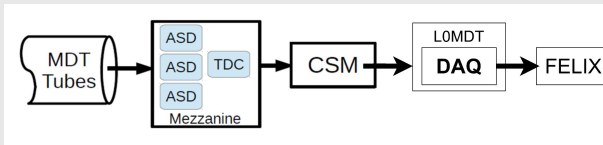
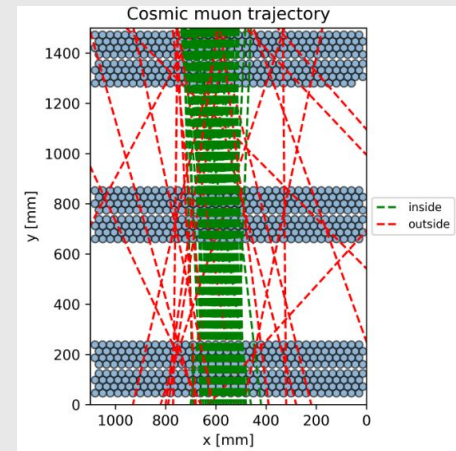
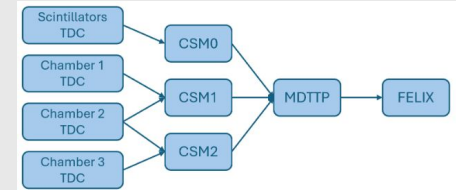
MDT-TP Status and testing

# MDT Electronics Chain

- Progress integrating the MDTP in the MDT electronics chain
  - Developments include testing single connections
- Final validation at cosmic ray test stands using real detectors in full chain
  - Currently able to
    - Read out the MDT chamber hit data via FELIX
    - Configure and monitor the MDT front-end electronics
- Successfully using the [FELIX-182](#) card see [Carlo's talk](#)
- Major goal is the development of the MDT readout logic for [FELIX](#)
  - Successfully developed, implemented & tested triggerless readout
  - Work ongoing to implement LOA processing



Cosmic muons captured with triggerless mode



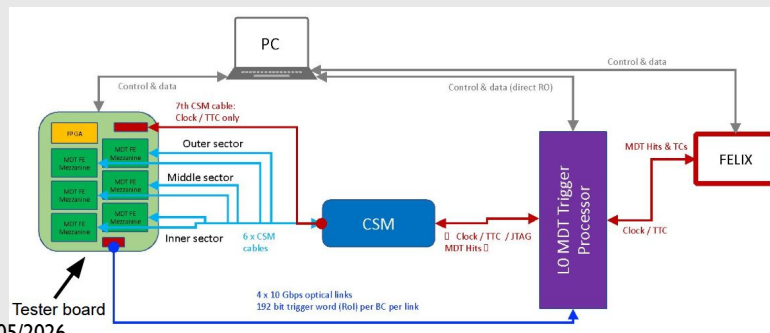
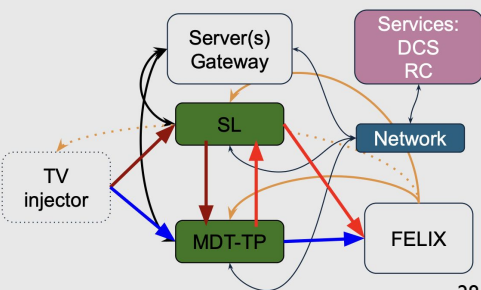
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# L0 Muon Chain Integration and Testing

- Leverage available test stands for single systems, including
  - MDTTP focused
  - Sector Logic focused
- Developing TDAQ test setup
  - Shared between all groups (Muons and others)
  - Thermal test rack
- Main types of tests
  - Board to board to FELIX Communication
  - SL to MuCTPi to Global
  - Experiment Services (DCS,RC)
  - TestVector injection, pulsed front end inputs



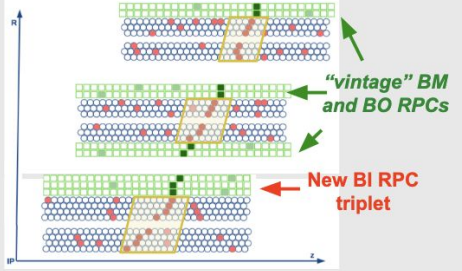
CERN - SRI  
Main location for integration tests



# NGT activities: R&D for Robustness & Exotic Signals

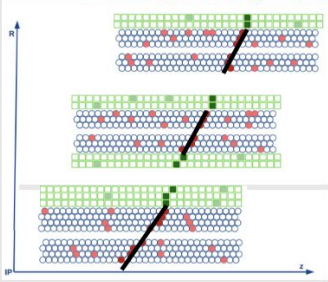
### Hit Extraction

RPCs provide seeds to identify MDT hits from a muon & set up segment fitting



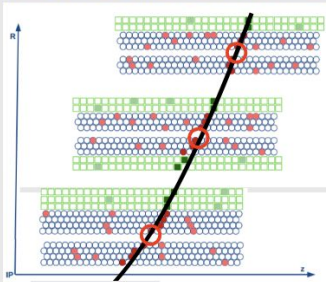
### Segment Fitting

RPCs provide timing to calibrate hits and derive segments



### Momentum Estimation

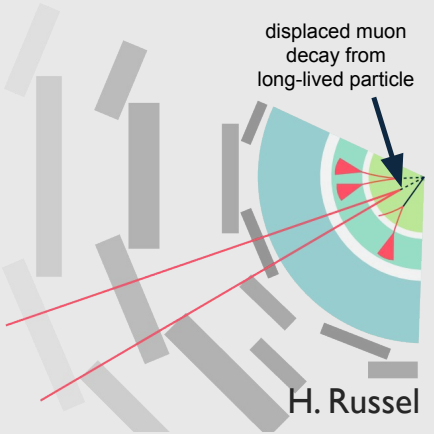
RPCs provide 2<sup>nd</sup> coordinate for the  $p_T$  estimate since B-field is non-uniform in phi



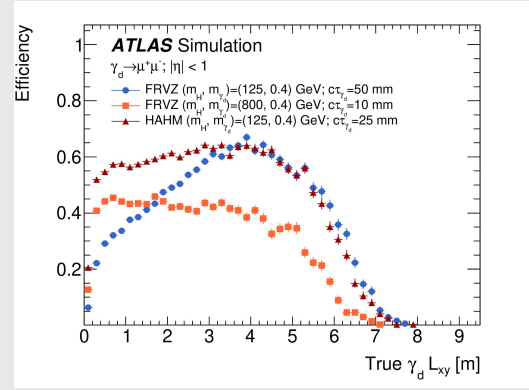
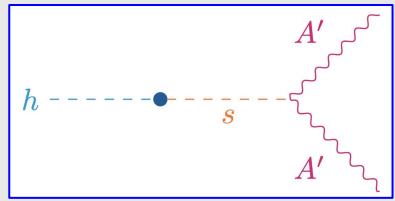
MDT Trigger with poorer seeds from RPCs (e.g. BI only) or no available seeds

**Baseline L0 Muon trigger in ATLAS relies on RPCs for best selectivity & performance**

Goal is to study different algorithms/approaches for L0 Muon triggers in case of reduced RPC performance or coverage for new RPC chambers



**Also exploring the possibility of new algorithms targeting exotic signatures for example from long-lived particles**

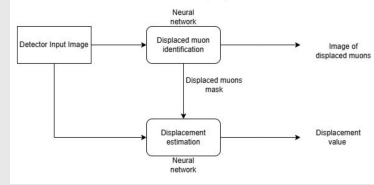
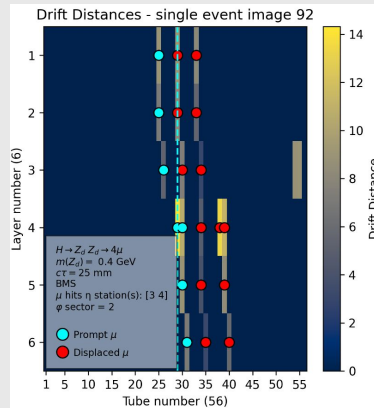


Exploring use of novel ML techniques

# NGT activities: Machine Learning algorithms

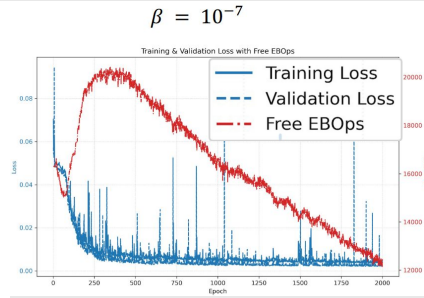
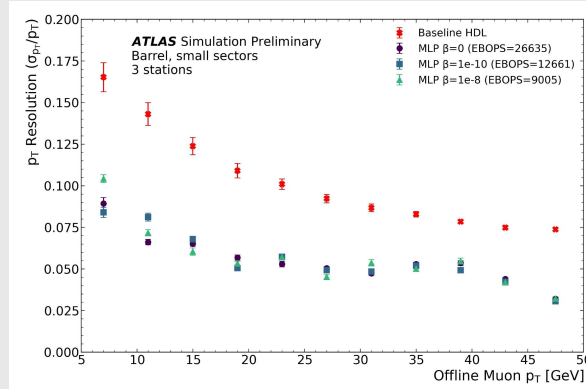
## Displaced muon identification

- Trigger limitations for analyses targeting long-lived exotic signatures
  - muon pair fall in the same RPC pad (single muon trigger item) or non-pointing
- Studying properties of signatures and exploring dedicated algorithms
  - Initial focus on very collimated cases - low dark photon mass
- Developing CNN & RNN algorithms to identify muon hits & distinguish from backgrounds
- M. thesis A. Kakos & E. Larié
- Also exploring GNN & transformer architectures - more challenging to implement



## Momentum estimation

- Using a NN improve the momentum estimation or make it more robust given the inhomogeneous B-field in the muons
- Using a simple model to test inference of NN models in accelerator cards using HLS4ML
- Pipeline developed HP scan → training → conversion → FW



[AtlasPublic/L0MuonTriggerPublicResults](https://atlaspublic.l0muontriggerpublicresults)

\* Summary:

Latency (cycles)		Latency (absolute)		Interval	
min	max	min	max	min	max
8	8	40.000 ns	40.000 ns	1	1

Vitis Implementation

# Summary and Outlook

- The MDTTP pre-production is ongoing
  - Pre-production of SM is ongoing and pre-production of CM v3 is starting
  - Firmware actively progressing
- Basic tests and tests stands at the several institutes and CERN being development
  - Hardware design has been validated
  - Interfaces have been validated
  - Slice tests for MDT and TDAQ chains are being developed and exercised with increasing realism
- The tests have pushed forward the development of software required for the forthcoming commissioning and operations.
- Next Generation Trigger project is focused on R&D including using ML methods towards possible future developments beyond the baseline
  - First implementation of a pipeline from simulation to hardware test
  - Implemented several ML algorithms including for (displaced) muon identification and pT estimation
  - New algorithms still under development and simulation.