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U.S. DEPARTMENT OF ENERGY
Office of Science

A High-Bandwidth, High-Framerate Integrated Ionizing Particle Detection System

IEEE Real Time Conference, Elba, Italy 05/26/2026

Carl Grace, on behalf of the Advanced Accelerator Diagnostics Collaboration

Lawrence Berkeley National Laboratory

Advanced Accelerator Diagnostics Collaboration

- Three University of California campuses and three US National Labs
  - UC Santa Cruz (Santa Cruz Institute for Particle Physics), UC Davis, UC Santa Barbara
  - Lawrence Berkeley National Lab, Los Alamos National Lab, SLAC National Accelerator Lab

- Originally funded by the University of California, Office of the President. Current funding from the the US Department of Energy

- Developing diagnostic systems for XFEL, synchrotron, and proton beams and performing basic diamond sensor R&D (transport properties, radiation tolerance). Focus of this talk is on beam position monitors for future XFELs.

UC SANTA BARBARA

Los Alamos NATIONAL LABORATORY

SLAC NATIONAL ACCELERATOR LABORATORY

UCDAVIS

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SCIPP SANTA CRUZ INSTITUTE FOR PARTICLE PHYSICS UC SANTA CRUZ

Per-pulse XFEL beam diagnostics in the sub-ns regime

Capturing 100-300 ps X-ray pulses

THE CHALLENGE

Next-gen XFELs

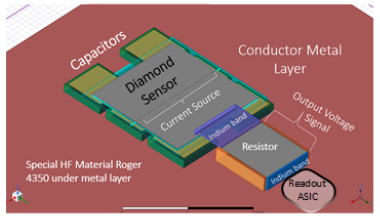
- 10^6 pulses/s
- 100-300 ps spacing
- Multi-pulse trains

Current 50 MHz electronics too slow and cannot resolve individual pulses

Remote digitizers smear signals

OUR APPROACH

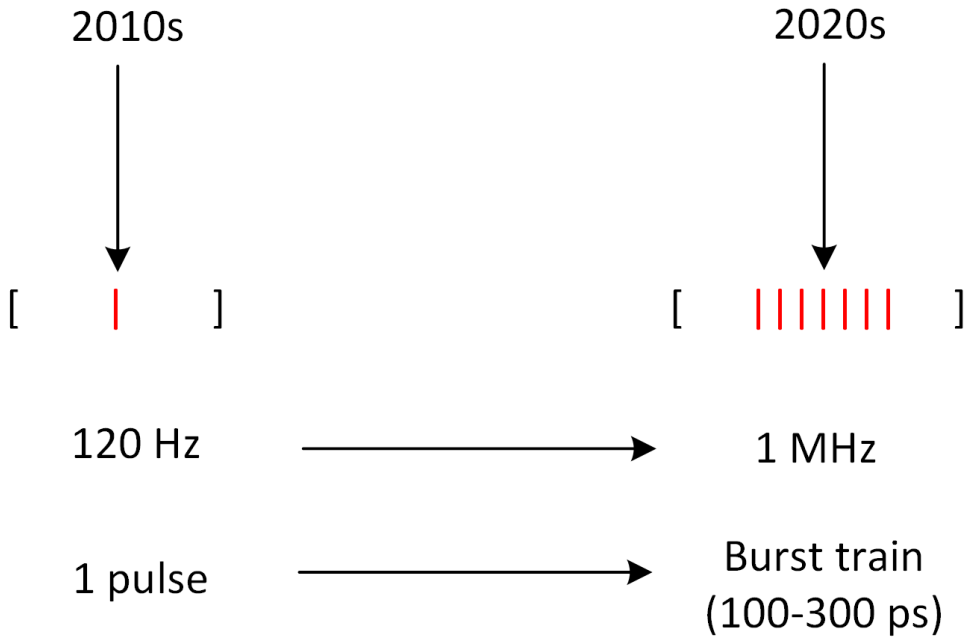
Move digitization TO the detector



- 36 GS/s
- < 250 fs Jitter
- Minimal cables
- Diamond + ASIC integration

Need: position, intensity, timing (<ps), waveform

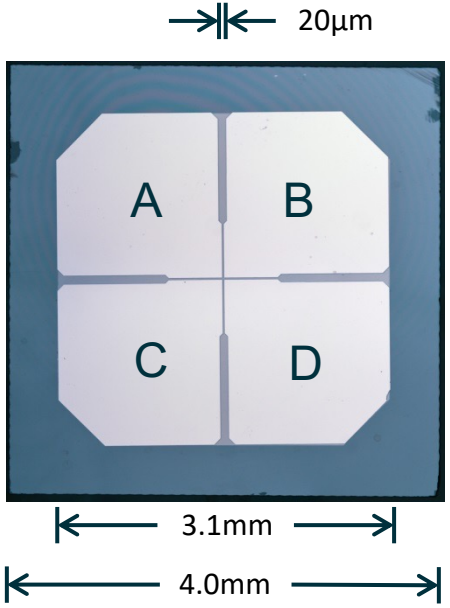
Evolution



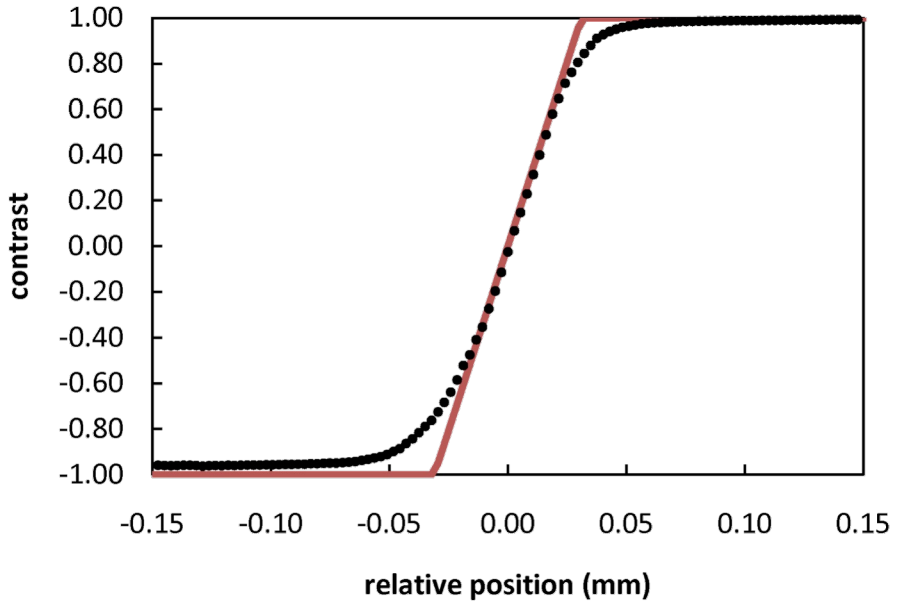
Tarun Prakash, IEEE NSS, 2025

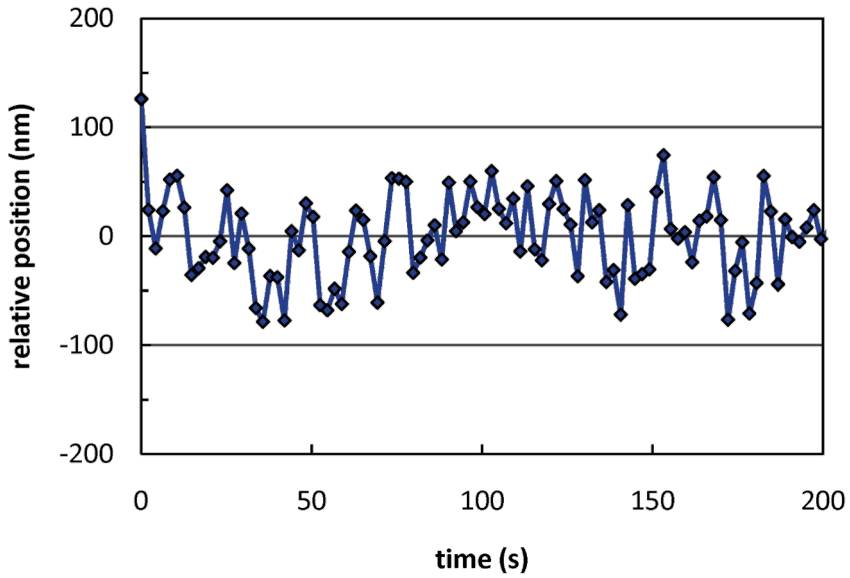
Beam Position Monitors

30-50 µm thick
Metallization: 25 nm Pt



$$X = G_x \frac{(I_B + I_D) - (I_A + I_C)}{I_A + I_B + I_C + I_D}$$

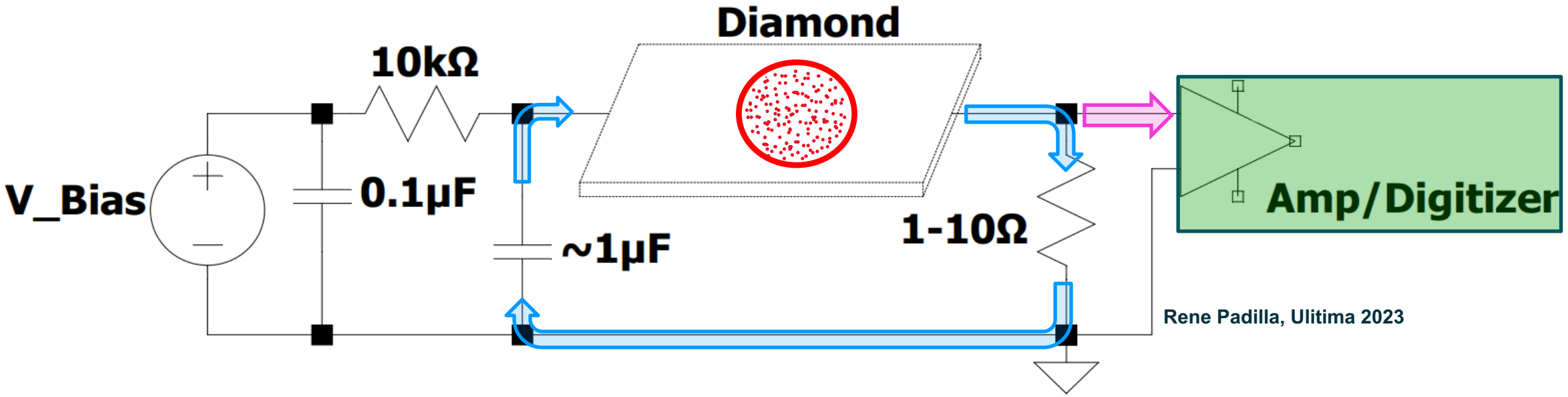




Diamond Sensors

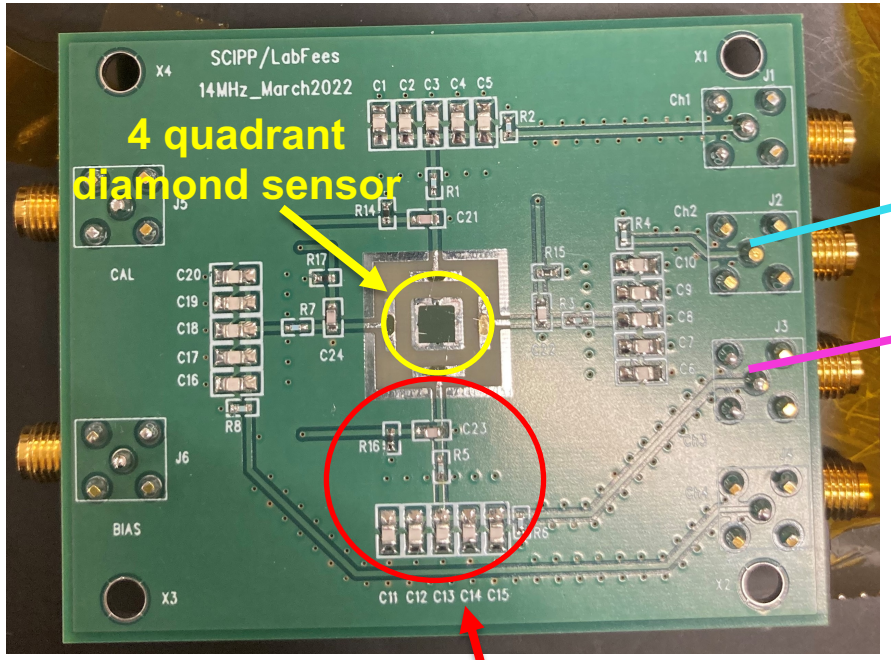
- Low X-ray Absorption (can be used in beam path)
- High Thermal Conductivity
- Radiation Hardness
- Large, indirect bandgap 5.5 eV → 13.3 eV/eh-pair (~4X silicon)
- High mobility (~2X e^- and 4X holes compared to Si)
- Fabricated at LANL

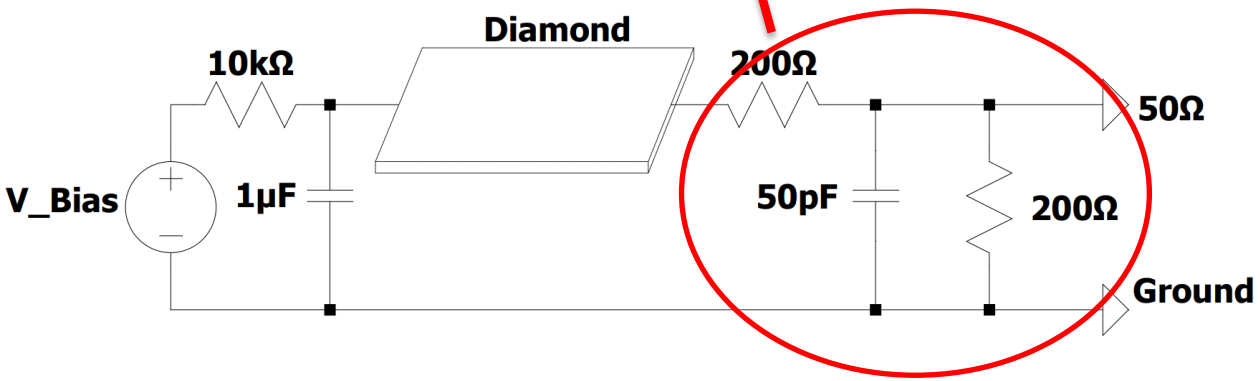
Fast Diamond Sensor System Concept



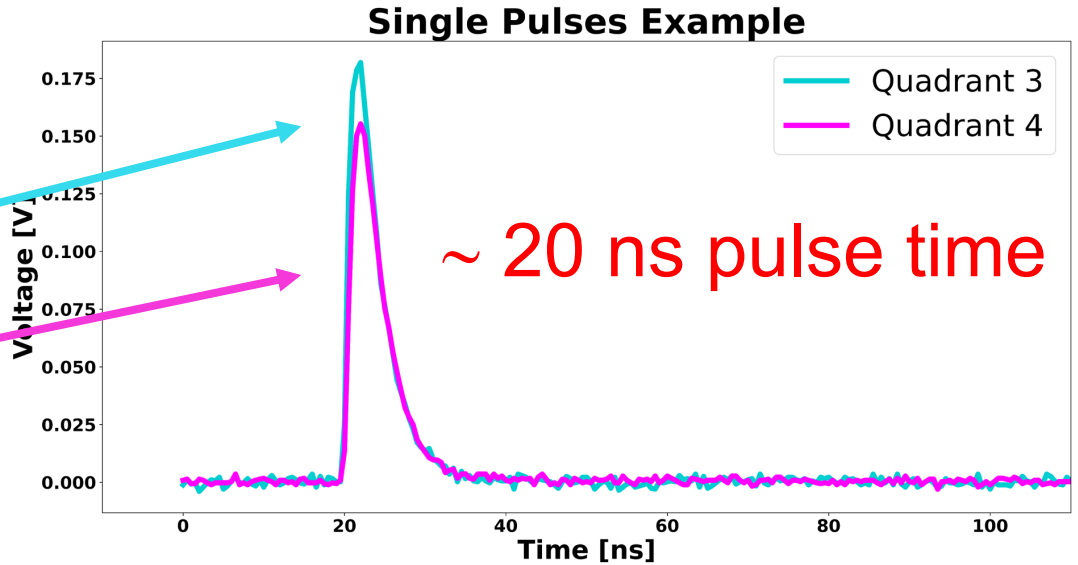
- **Charge Collection (LANL, SLAC)**
  - Diamond fast and efficient up to ~10^{16} charges/cm^3
- **Signal Path (UCSC, UCSB)**
  - How fast the signal can return to ground without ringing?
- **Signal processing / amplification / buffering / digitization (LBNL and UC Davis)**
  - High speed electronics development
- **Interfacing of signal path with signal processing features (LBNL)**
  - RF Engineering

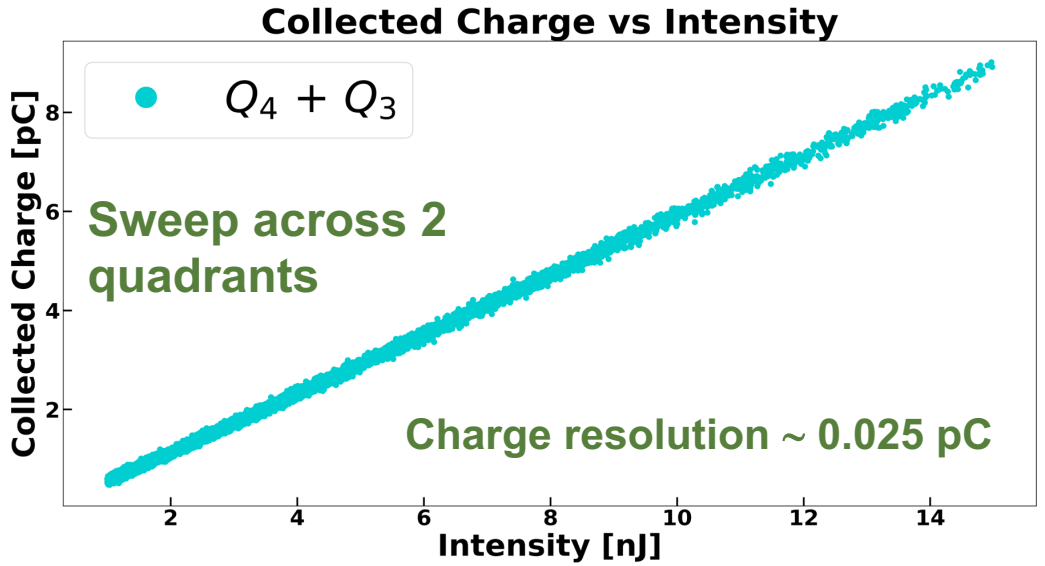
50 MHz Position-Sensitive Diagnostic (proof of concept)



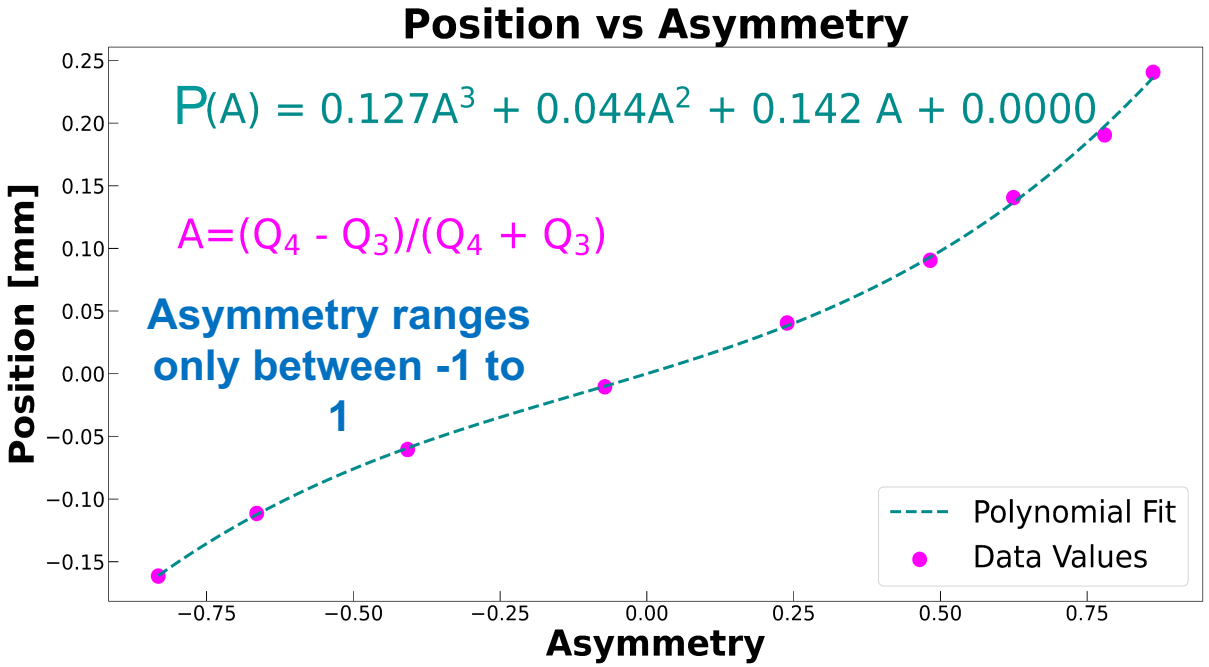


~ 10 ns shaping network





50 MHz Position-Sensitive Diagnostic (proof of concept)



$$\sigma_p = \frac{dP}{dA}\sigma_A$$

→ Position Resolution

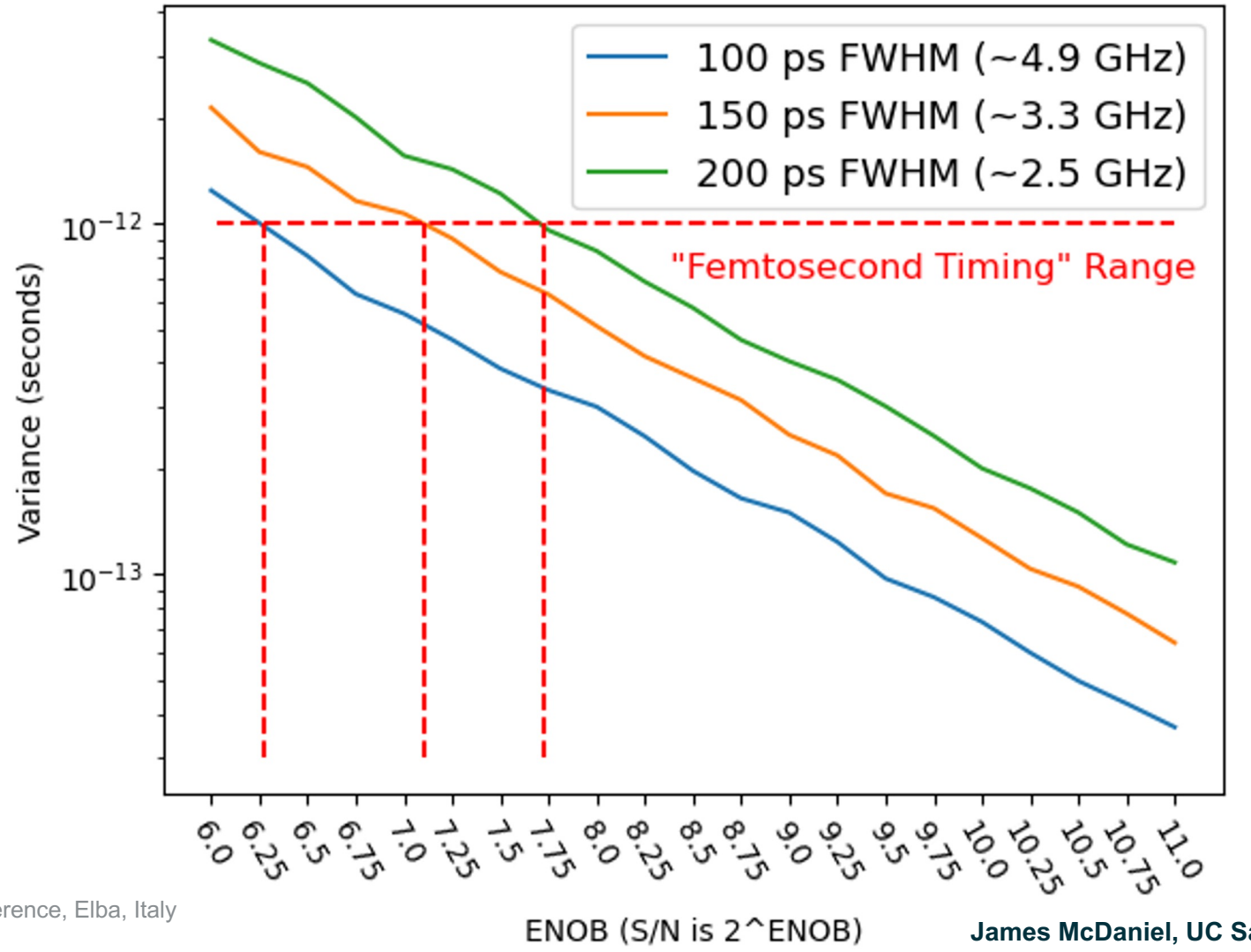
$$\sigma_A = \frac{\sigma_Q}{Q}\sqrt{1 + A^2}$$

For 4 nJ pulse ~ σ_Q of 0.025 pC yields to 2 μm centroid position resolution (pulse-by-pulse)

ASIC needed to extend speed by 20X +

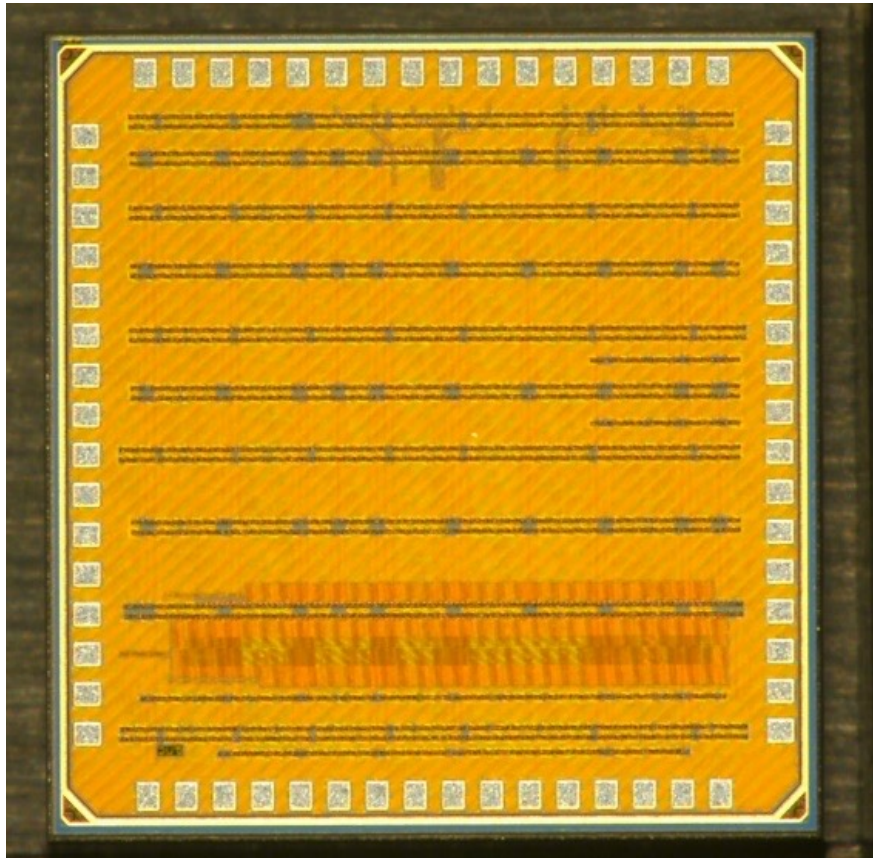
ASIC Specification

Timing Accuracy vs ENOB and analog BW (sampling at ~40 GS/s)



James McDaniel, UC Santa Cruz 2023

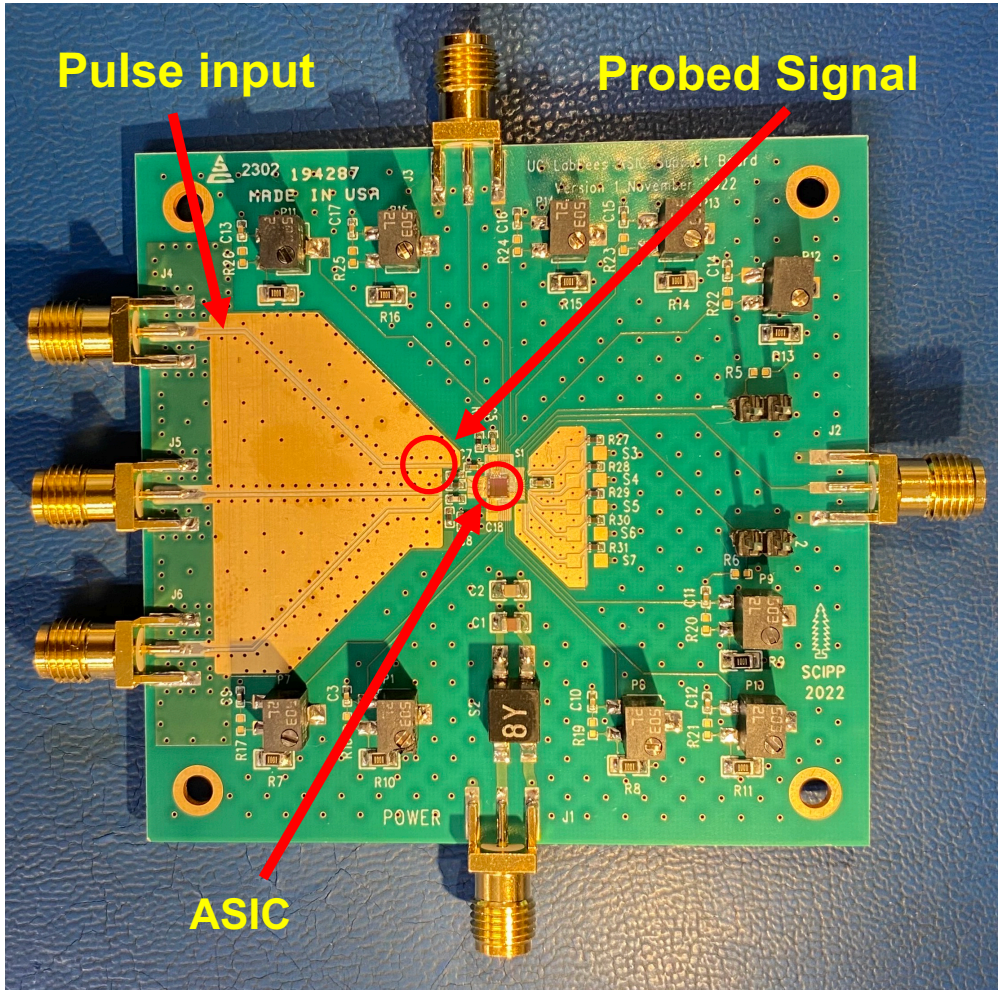
First ASIC – FPS-0 (was LABFEES)

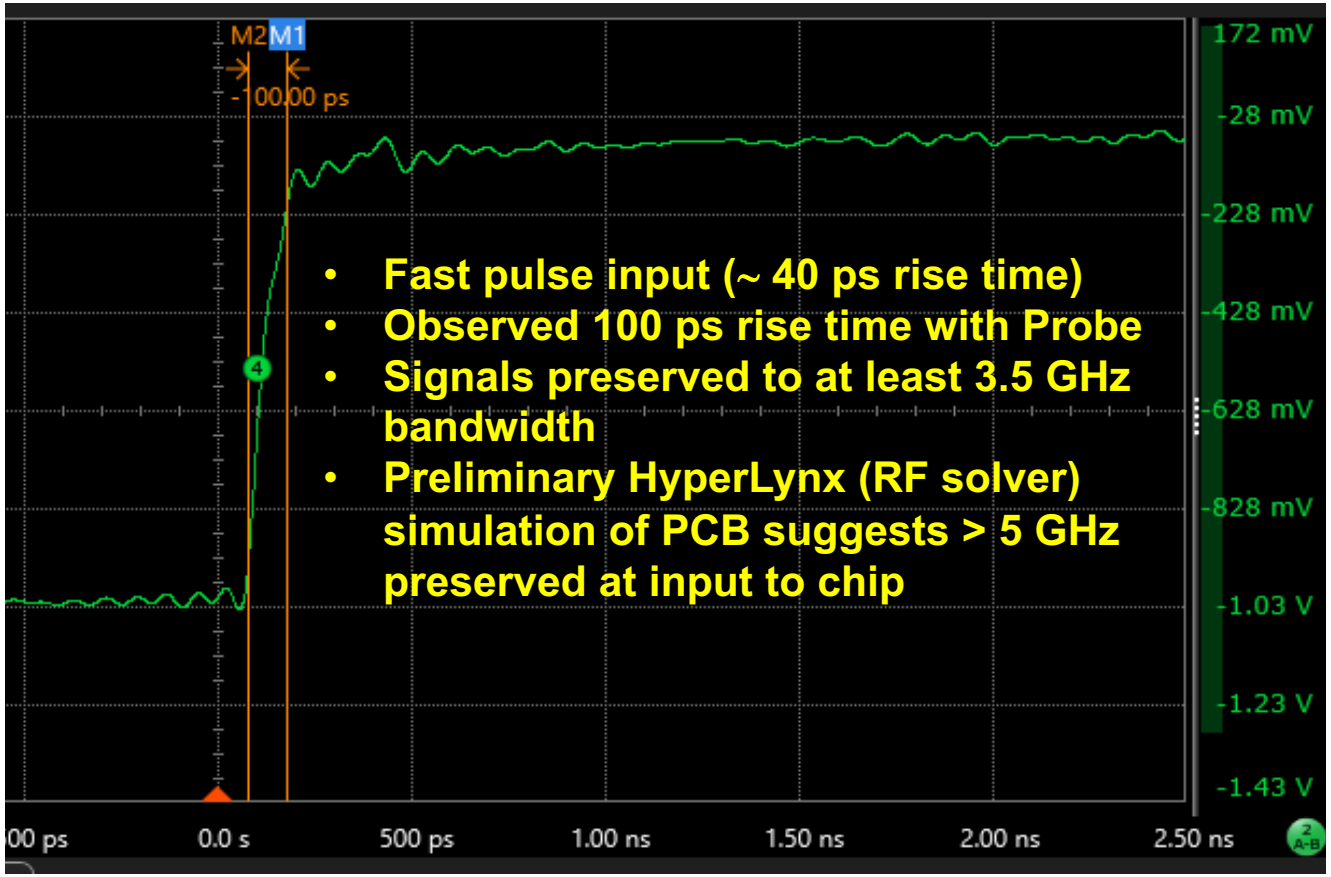


First ASIC submitted 04/2022

- Intended to explore front end architectures
- Designed for 11 GHz bandwidth
- 3 transimpedance (current mode input) amplifiers
- 3 voltage sensitive inputs
- Included ring oscillator and internal bias network
- Measured BW of 3.5 GHz. Limitation was use of active inductors in the front end to reduce silicon area
- Implemented in 65nm CMOS

First ASIC (FPS-0) performance

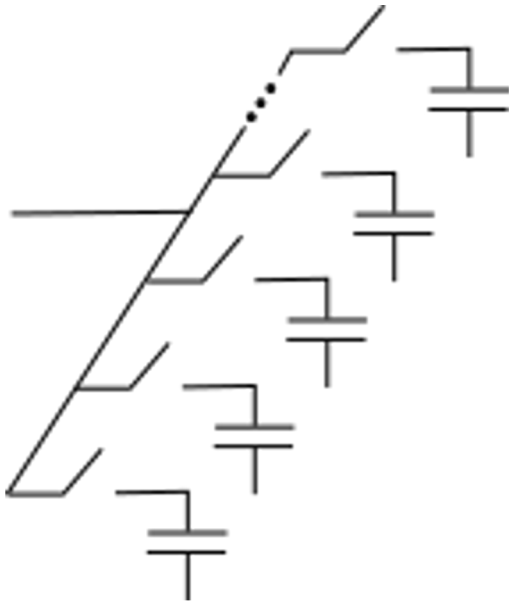




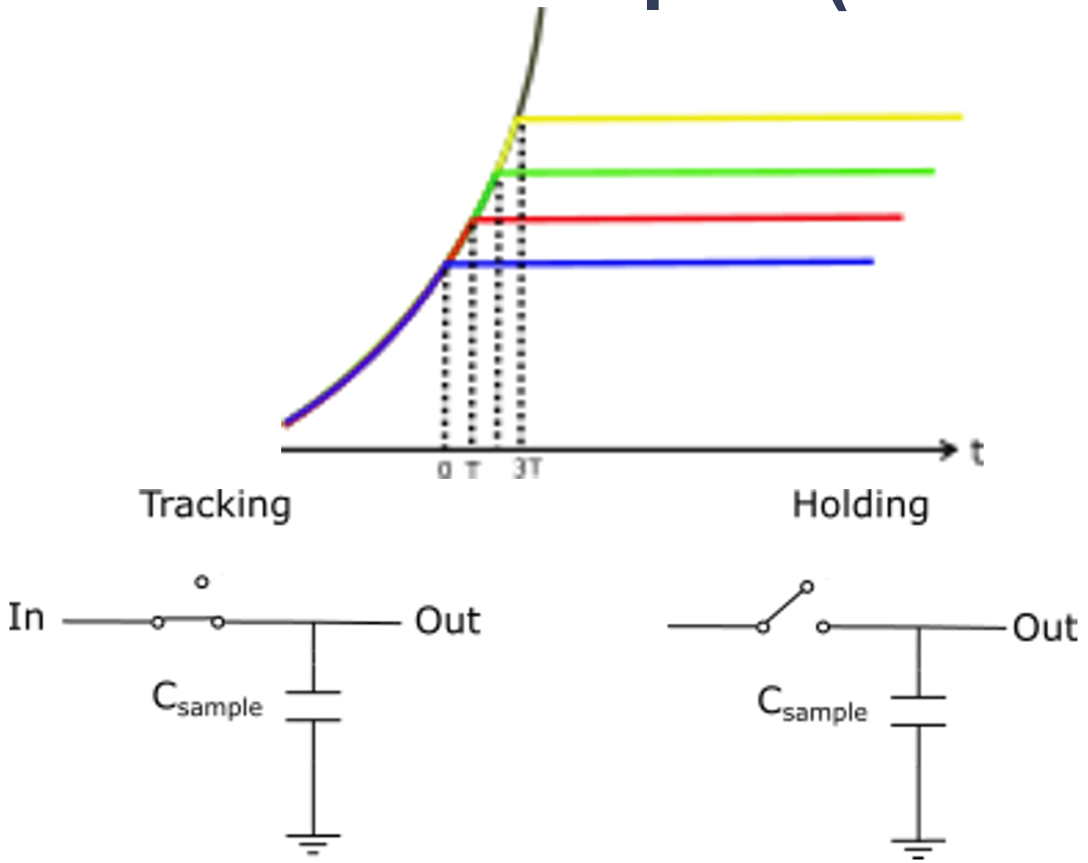
Rene Padilla, Ulitima 2023

Second ASIC – FastPulse Precision Sampler (FPS-1)

Input pulse



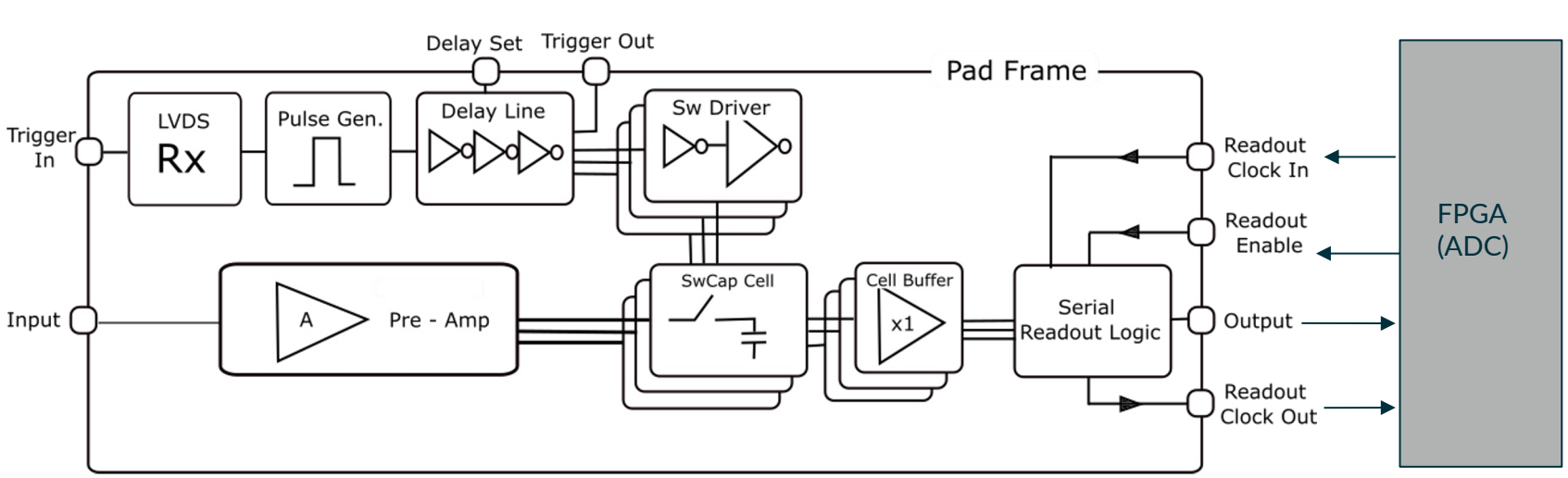
Switched-Capacitor array

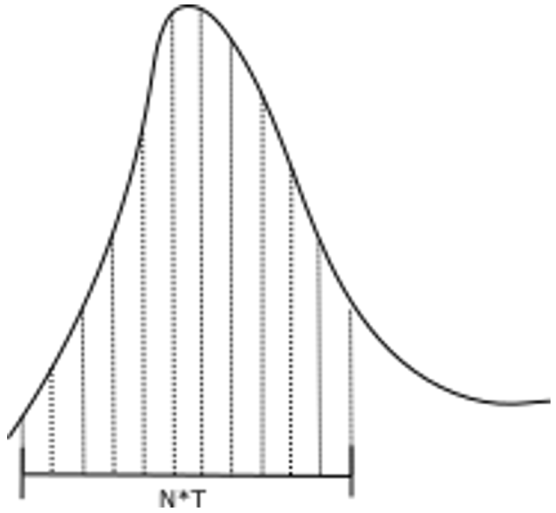


Conrad Rowling, UC Davis MS Thesis

- Concept: use array of capacitors to store fast pulse in “analog memory” and digitize slowly
- Useful because sampling is a faster process than quantization

Second ASIC – FastPulse Precision Sampler (FPS-1)



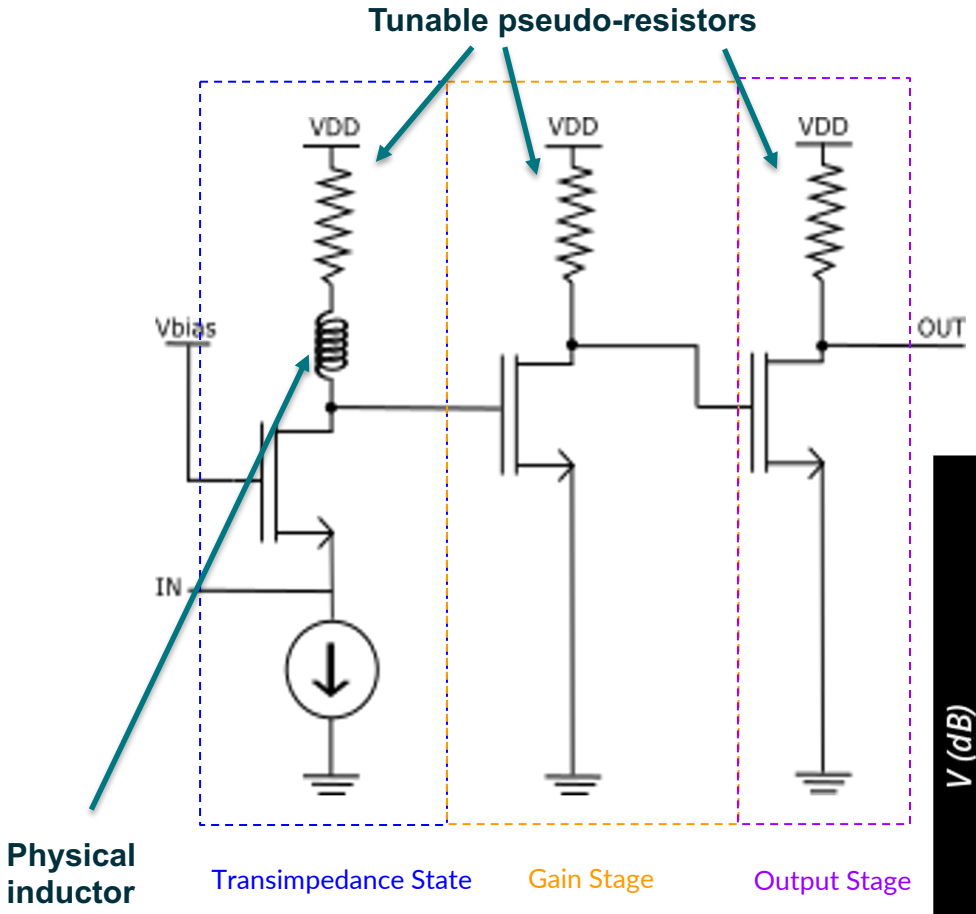


Second ASIC submitted 03/2023

Specification	Value	Unit
Sample Rate	50	Gs/s
Capture Window	1	ns
Readout Rate	500	MHz
Resolution	10	bits

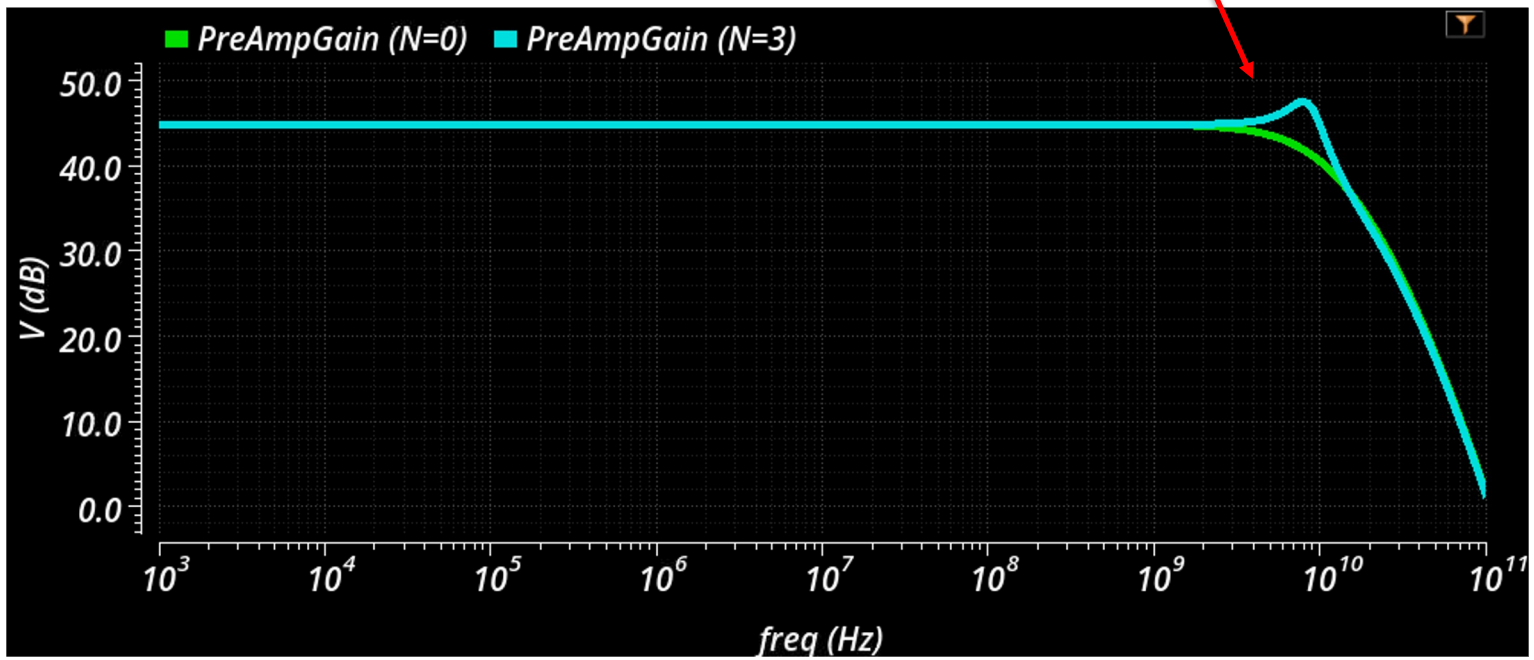
- Four-channel waveform digitizer with analog output
- Externally-triggered sampling
- Improved current-mode input amplifier
- Implemented in 65 nm CMOS

Second ASIC - FastPulse Precision Sampler (FPS-1)

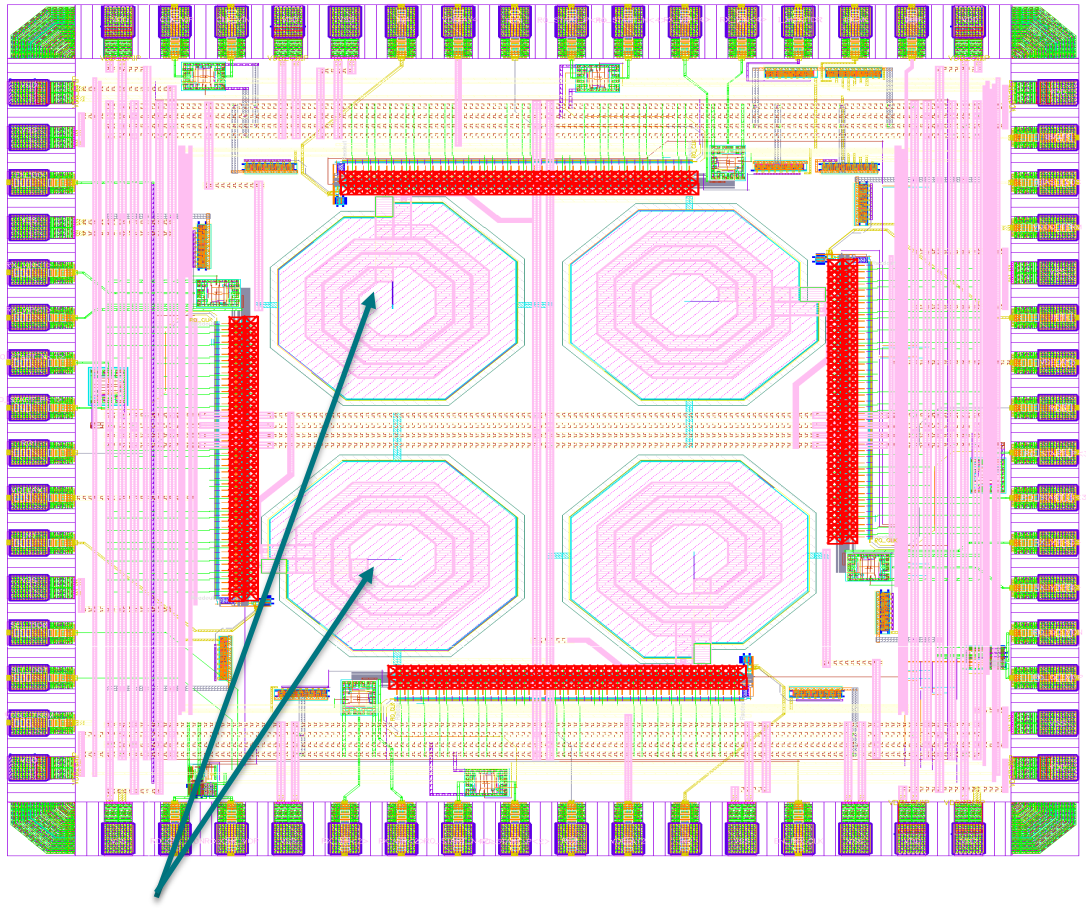


Key changes to address UCFEES ASIC shortcomings:

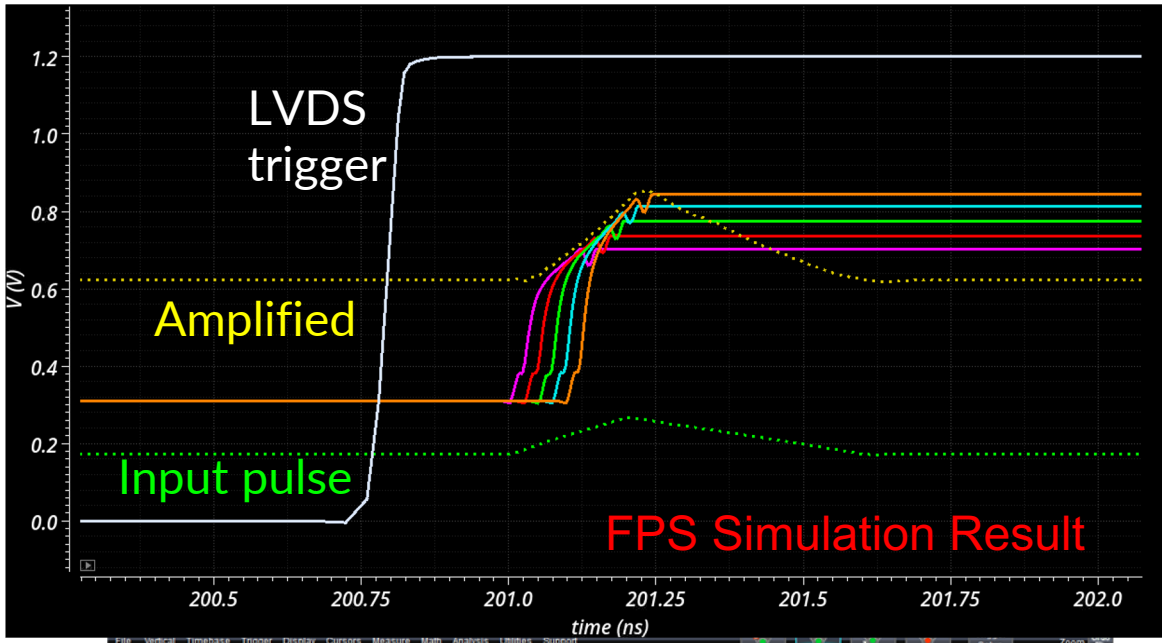
- Common-gate input with inductive peaking ← key
- Multi-stage, open-loop design
- Dedicated low-gain output stage

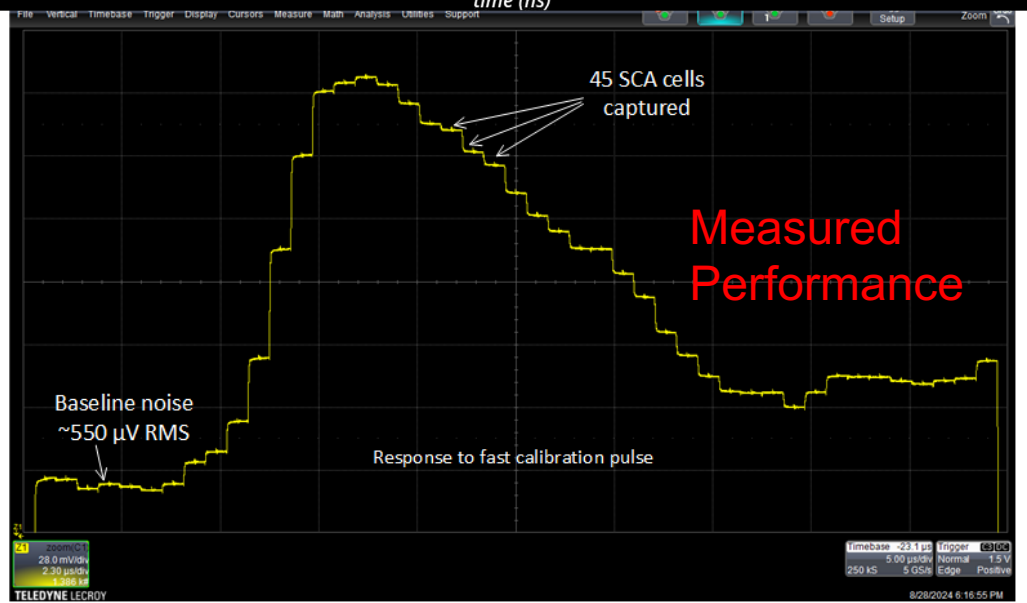


Second ASIC - FastPulse Precision Sampler (FPS-1)

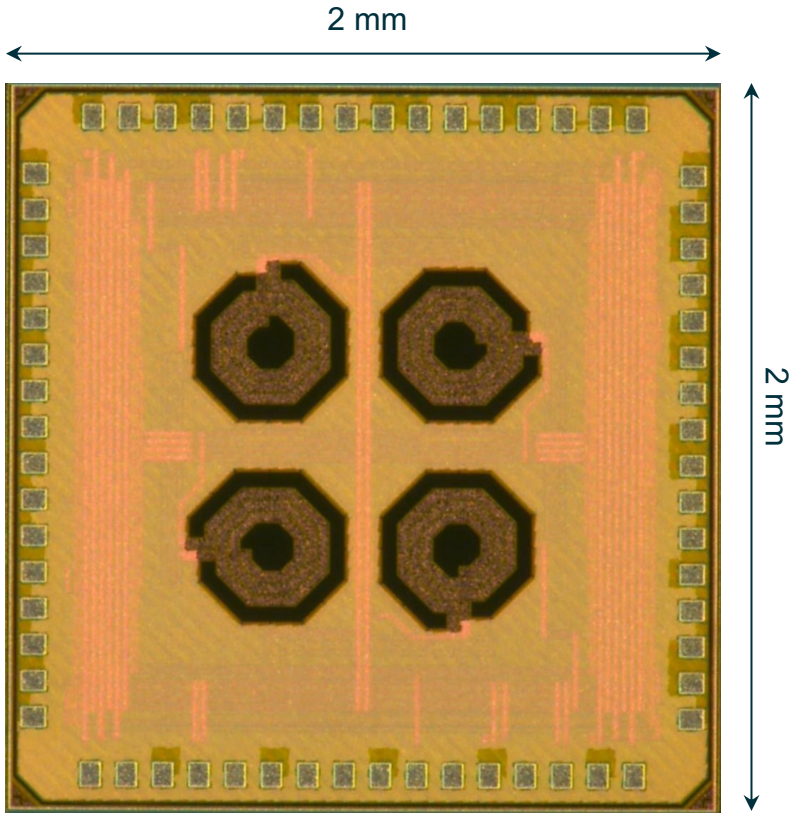


Inductors for gain peaking

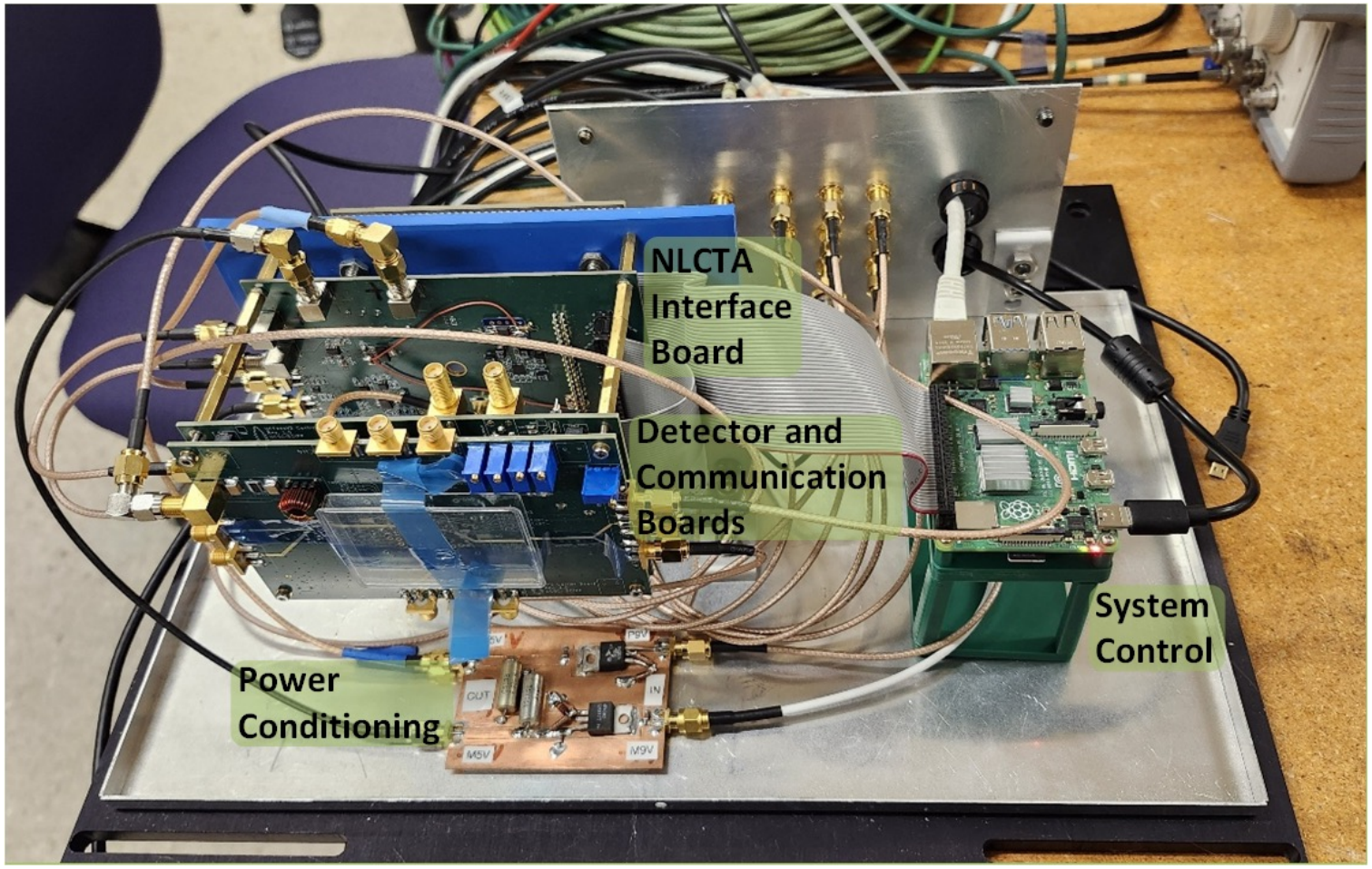




System Test at NLCTA at SLAC

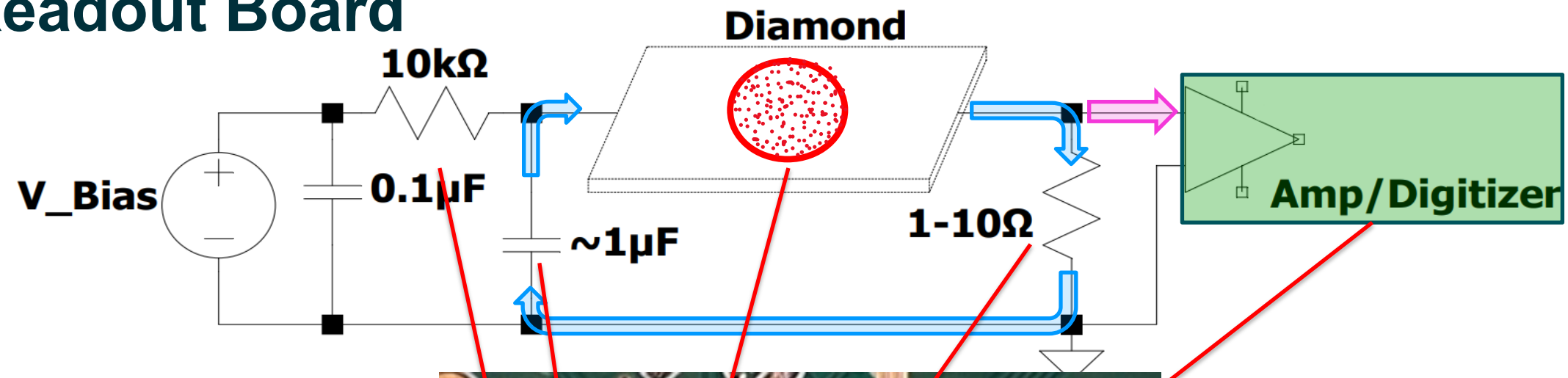


FPS-1 – 65 nm CMOS

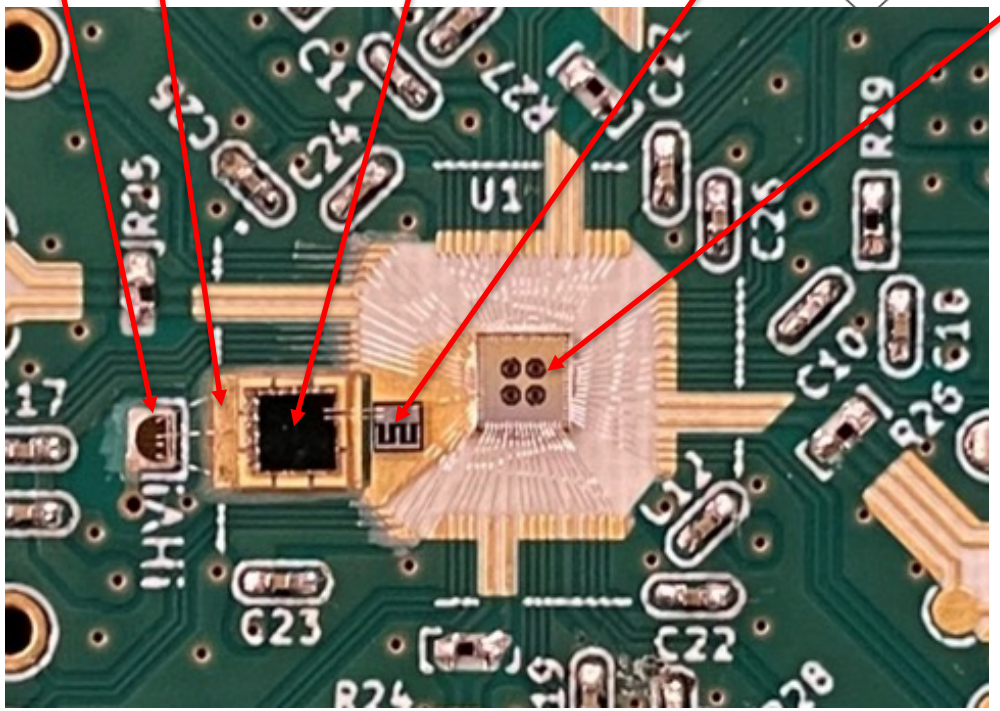


NLCTA = Next Generation Linear Collider Test Accelerator

Readout Board



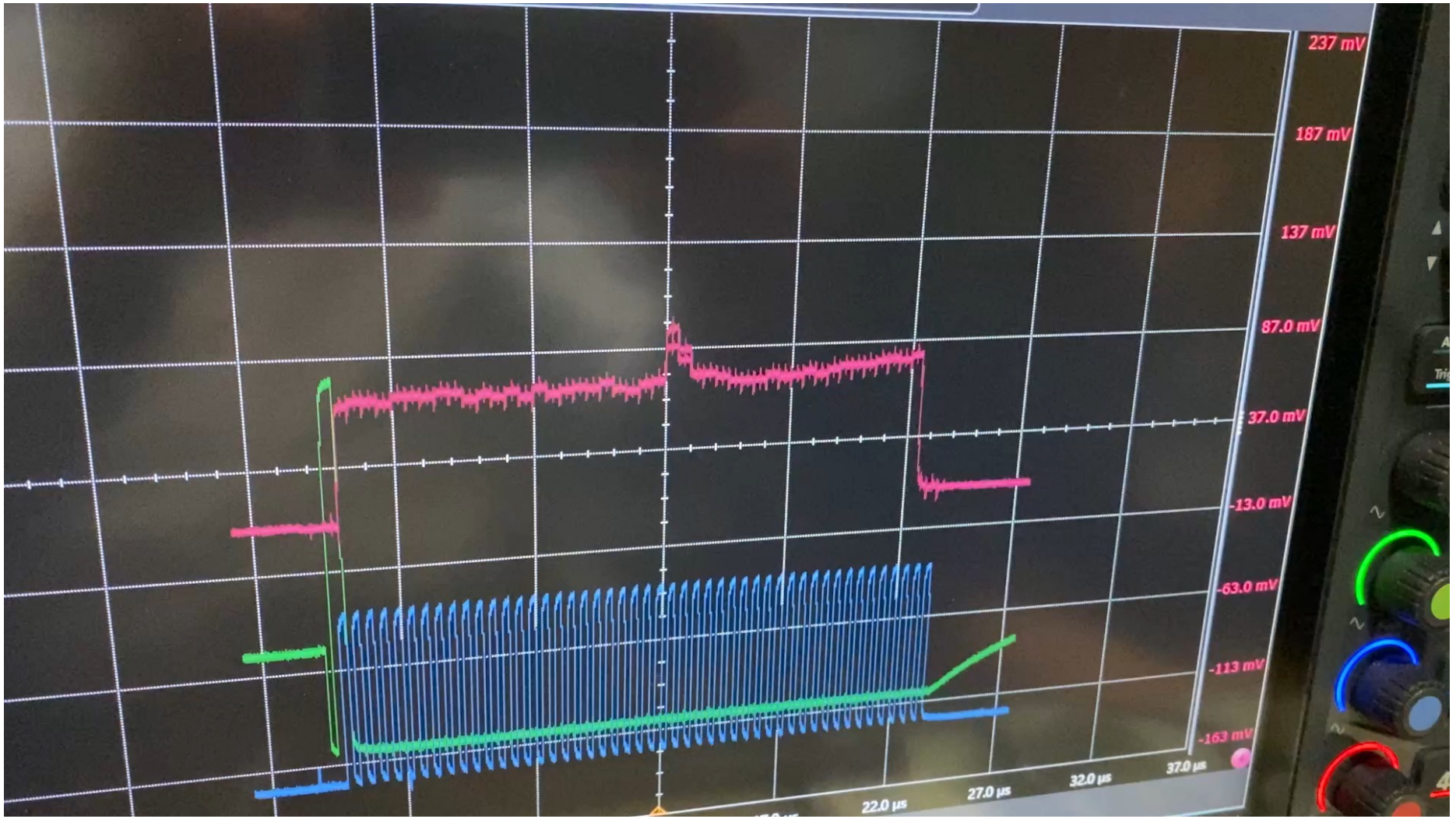
Zoom in on readout board



July 16, 2025: Beam delivered to the system

Search for beam with slowest sampling rate (~18 GS/s)

Capture window ~2.5 ns



Courtesy: B. A. Schumm, UCSC/SCIPP

July 16, 2025: Beam delivered to the system

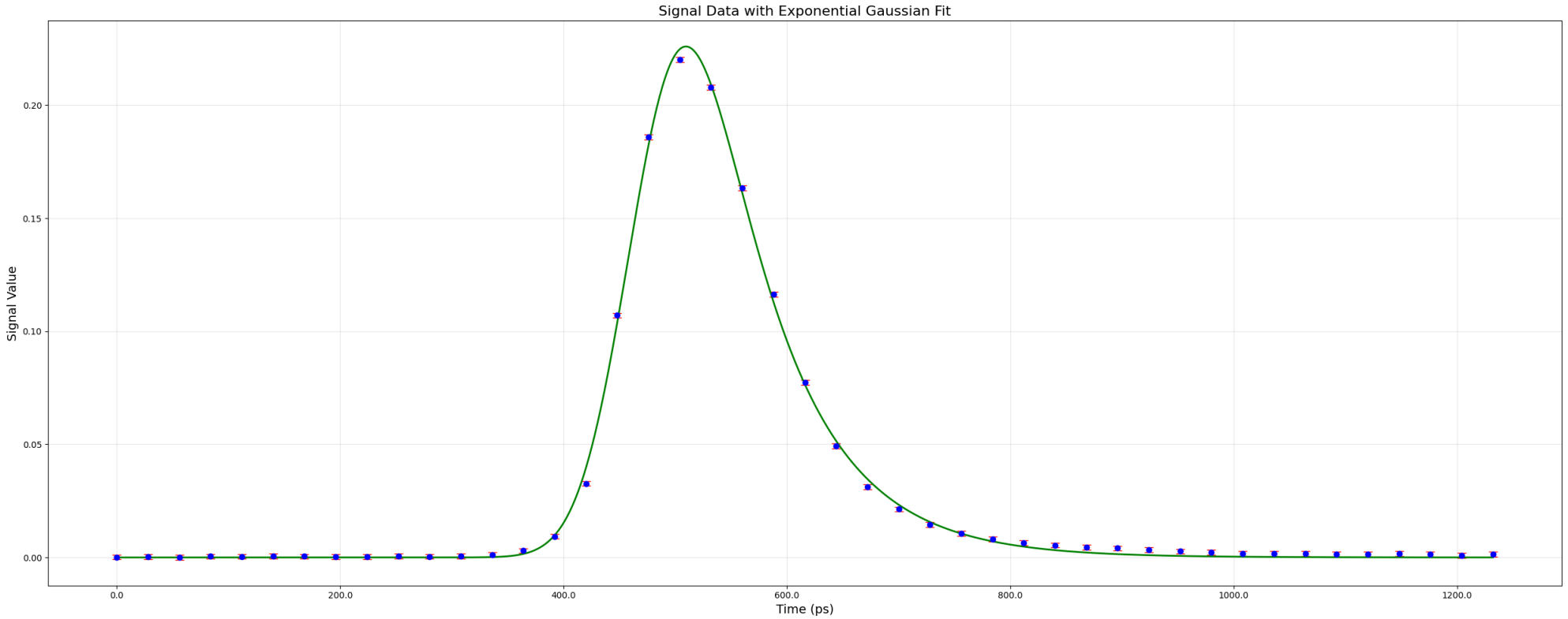
With beam found, switch to fastest sampling rate (~36 GS/s)

Capture window ~1.25 ns

Read out SCA at 2 MHz (500 ns per capacitor)

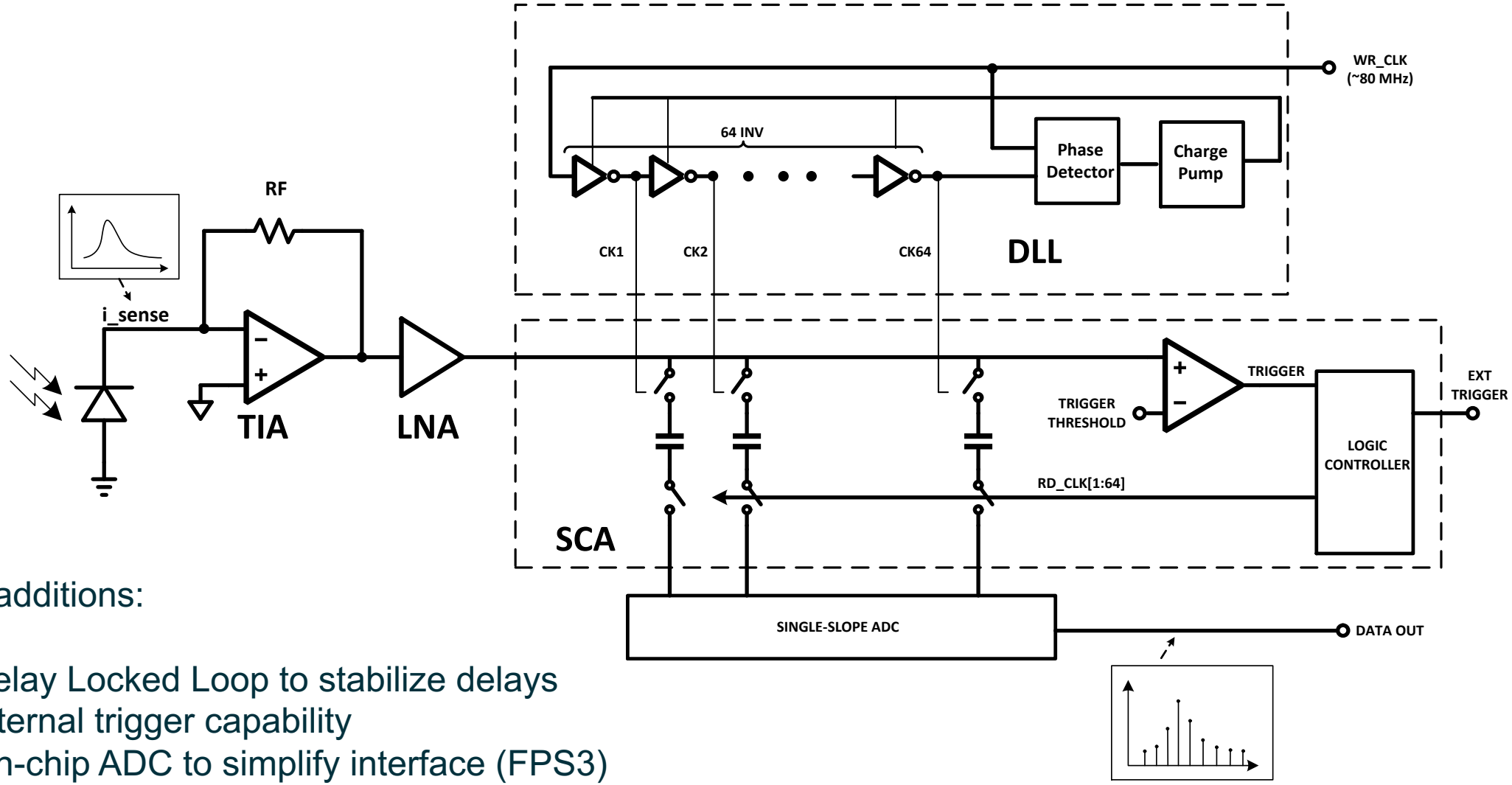
Courtesy: B. A. Schumm, UCSC/SCIPP

Measured beam pulse after averaging and fit



Cleanup: subtract pedestal, remove clock spikes, average ~1000 points → one value per cap
Align: use Δt calibration to map cells to time; reconstruct on 28 ps grid (~1.25 ns window)
Fit: Exponentially modified Gaussian fit to the samples; example pulse near top of linear range

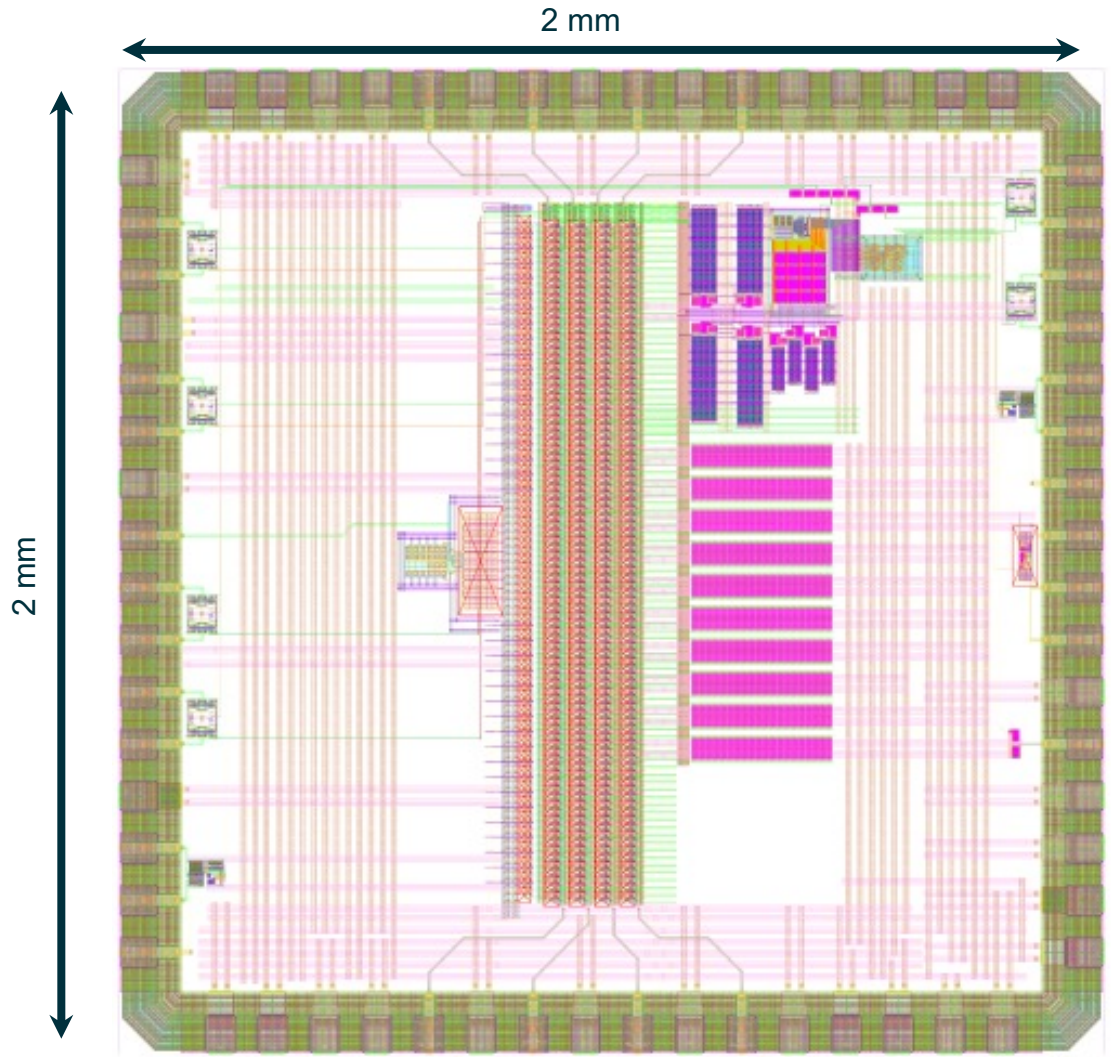
Third / Fourth ASIC (FPS2 / FPS3)



Key additions:

- Delay Locked Loop to stabilize delays
- Internal trigger capability
- On-chip ADC to simplify interface (FPS3)

FPS2 fabricated; characterization underway



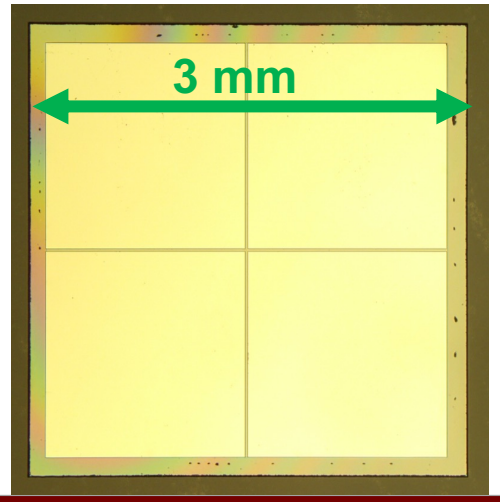
- Co-designed with compact signal path load (Spice level for now)
- Preamp change: regulated common gate amplifier for predictable 8+ GHz BW
- DLL from 1 GHz ref; low-jitter multiphase sampling; replica path for pulse conditioning
- 90 cells → 2.25 ns window at 25 ps spacing
- Improved routing/buffers to cut crosstalk;
- ADC will be added for FPS3

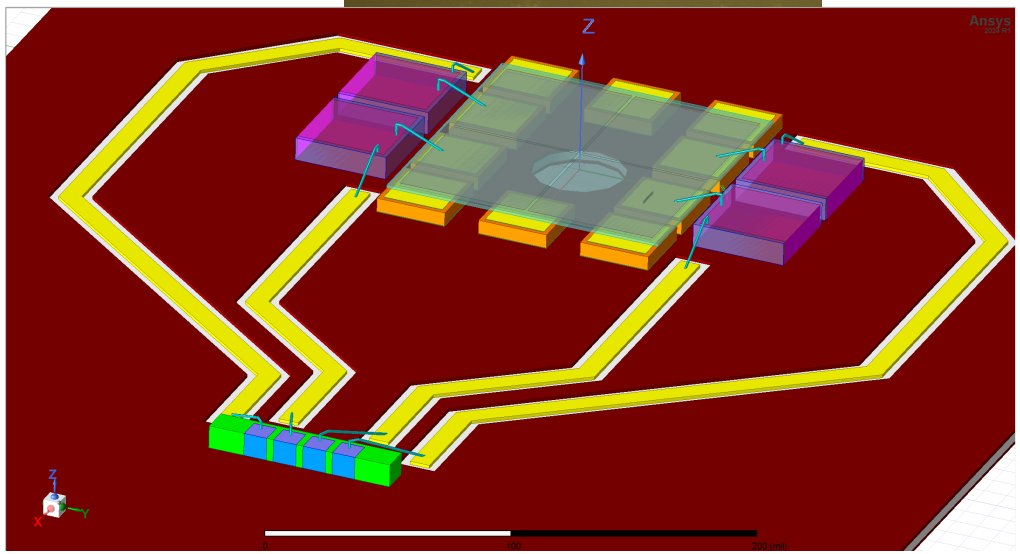
Comparison of FPS ASICs

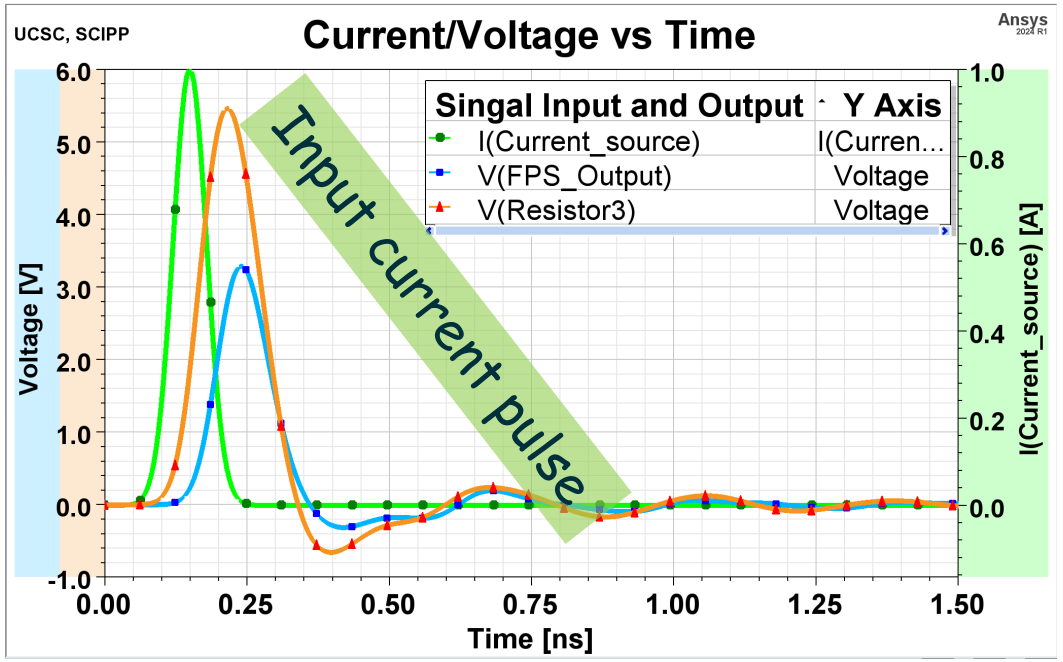
ASIC	BW [GHz]	Max Sampling Rate [GS/s]	Memory locations	Noise [μV-rms]	Resolution (ENOB)	Process [nm]	Fab Date
UCFEES (FPS-0)	3.5	N/A	N/A	750	N/A	65	2022
FPS-1	5	36	45	550	~ 8	65	2023
FPS-2	8	50	90	TBD	~ 9	65	2025 (under test)
FPS-3	TBD	TBD	TBD	TBD	10 (goal)	65	2028 (expected)

Future: Multi-GHz Position Sensing System

Diamond Sensor (LANL)







HFSS Simulation
10 Ohm back-contact sense resistor
50Ω traces on Rogers Material
FPS is 50Ω resistive load

Conclusion

- Developing high-speed diagnostics for next generation accelerators. End-goal is ease of use as well as performance
- Successfully demonstrated in-situ beam position monitoring
- Multi-GHz (5 – 10+ GHz) analog BW, 50+ GS/s, 10b+ readout generally useful
- Have made progress on diamond sensor, readout ASIC, and signal path

Thank You

This work was supported in part by the U.S. Department of Energy under Contract No. DE-AC02-05CH11231