A Low-Latency Distributed Machine-Protection System for the PIP-II Linear Accelerator

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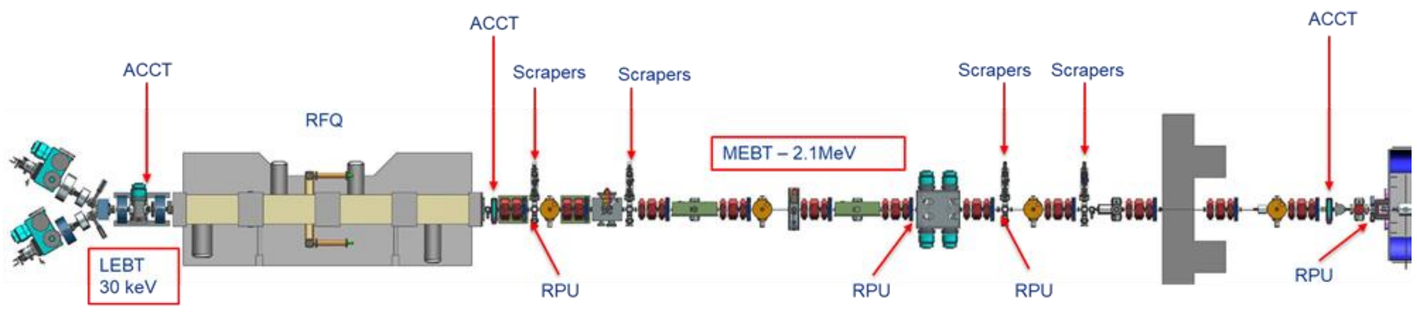
Protecting a 1 MW Superconducting Linac

PIP-II is an upgrade to the Fermilab accelerator complex that will deliver an intense high-energy neutrino beam to DUNE. It features an 800 MeV H^- superconducting linac with a Warm Front-End (WFE) and a 300-meter transfer line to the Booster. The WFE generates a 30 keV H^- beam, sets initial beam parameters, accelerates it to 2.1 MeV with an RFQ for downstream compatibility, and produces the required bunch pattern. A primary goal of PIP-II is to provide over 1 MW of reliable proton beam power to the target while supporting multiuser operation of the Fermilab complex.

The machine protection scheme is designed to protect the machine from instantaneous and long-term beam induced damage.



A view of the Low Energy Beam Transport (LEBT) section, showing two ion sources and the DCCTs and Toroid used to measure the beam current and chopper operation.

Distributed Digitization Nodes

Beam-sensing devices; AC Current Transformers (ACCTs), Ring Pickups (RPUs), and scrapers are distributed along the linac. Analog signals from each device are conditioned and digitized at locally distributed digitization nodes.

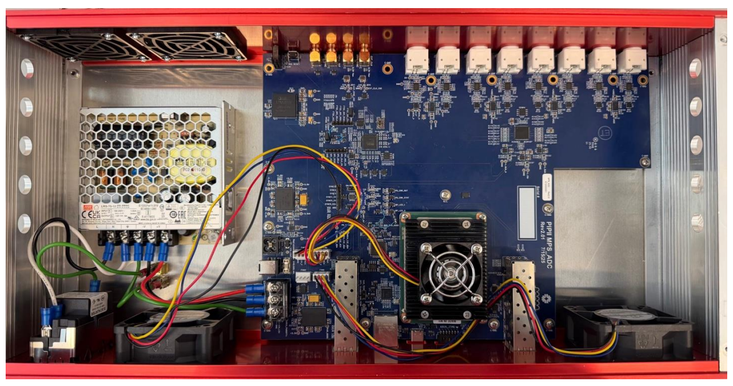
Each remote node streams 2 GB/s of ADC 16-bit samples (8 channels × 16 bits × 125 MHz) over two 10 Gb/s fiberoptic lanes to the central processor. The central processor applies per-channel calibrations, low-pass filtering, and the Differential Beam Current Monitor (DBCM) algorithm across all channels simultaneously.

The DBCM algorithm monitors the beam current at multiple sites across the linac and from insertable devices such as scrapers to detect instantaneous and long-term beam loss, and to monitor the action of control devices such as the low-energy beam chopper.

A 1-second circular post-mortem buffer in the 4 GB DDR on each node allows full-rate waveform capture. The buffer is readable over the GigE management interface without interrupting the protection data path for both monitoring and post-fault analysis.

During link initialization, the round-trip delay is measured and used to phase-align the 125 MHz digitization clock and SYSREF across all nodes. All data is synchronized and aligned at the central node.

Component Selection



An internal view of the digitization system

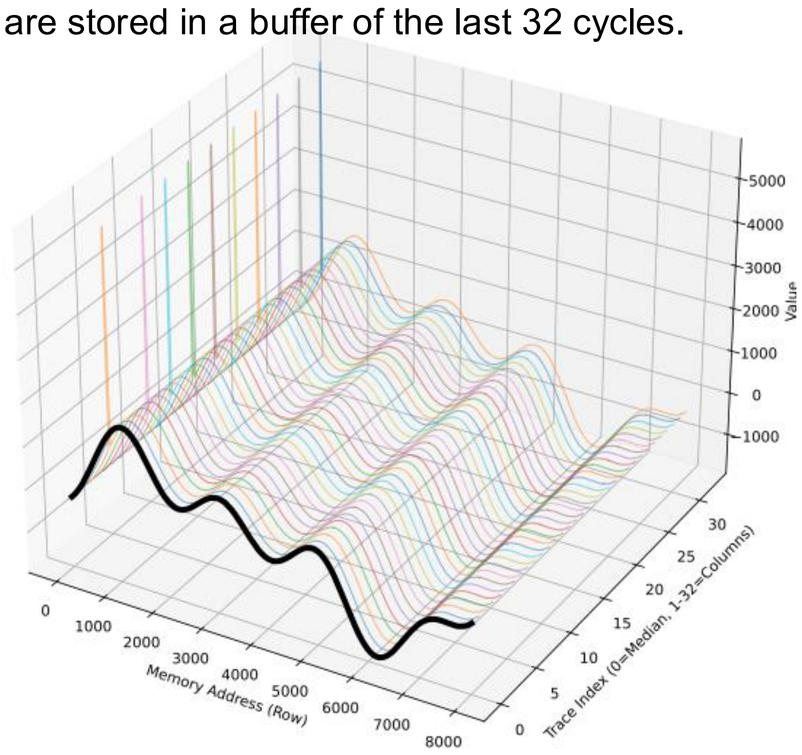
ADC TI ADS52J65 — 8-channel, 16-bit, 125 MSPS. Selected for its JESD204B Subclass 1 interface, which provides deterministic latency and simplifies multi-board PCB layout compared to parallel LVDS alternatives.

SoM AMD Kria K26 — Integrates a quad-core Cortex-A53 APU with UltraScale+ FPGA fabric, 4 GB DDR RAM, and GTH transceivers. Samples are routed through a scatter-gather DMA controller into a circular DDR buffer for monitoring and fault diagnosis.

Sync 8A34002 Synchronizer — Generates and distributes the system-wide 125 MHz clock reference and SYSREF pulses. Remote nodes recover the reference clock from the GTH serial link and phase-align digitization across all nodes during initialization.

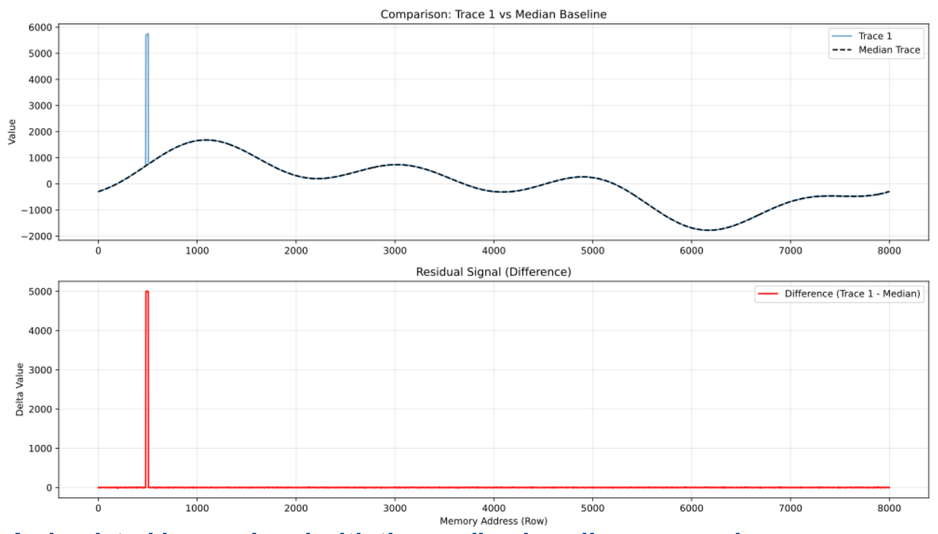
Online digital filtering

The raw digitized data may contain induced noise from both high frequency sources and low-frequency, harmonics of 60 Hz from AC powered equipment. To remove low-frequency baseline noise, we have developed multiple template subtraction algorithms. One algorithm uses a digital phased-locked loop to precisely synchronize to the 60 Hz AC phase and then downsample the data to 8000 points per phase, which are stored in a buffer of the last 32 cycles.



32 simulated 60 Hz cycles, with the 20 Hz beam signal and the median.

In the FPGA, the median for each point of the stored cycles is pre-calculated and used to interpolate the baseline shift to subtract from raw data as it arrives. This algorithm induces only three cycles of latency and runs easily at 125 MHz.



A simulated beam signal with the median baseline removed.

Status and Outlook

- The remote digitization nodes meet all primary design requirements.
- JESD204B Subclass 1 and GTH clock recovery together provide the deterministic, phase-aligned sampling needed to support the < 10 µs end-to-end latency budget.
- Hardware architecture validated; 2 GB/s data path and 1 s post-mortem buffer confirmed on K26 platform.
- Machine learning–based anomaly detection within FPGA fabric is planned to enhance loss sensitivity beyond threshold-based triggers