

# Tapped Delay Lines Time-to-Digital Converter Design and Performance in Versal Architecture

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## 1. INTRODUCTION

Tapped delay lines (TDLs) in FPGAs provide a flexible solution for precise timing measurements with reduced cost and shorter design time than application-specific circuits.

The main driver for higher resolution and precision is the FPGAs' fabrication process [1]. As the transistors get smaller, the average delay between each tap of the TDL also decreases, which leads to smaller bins and decreases the quantization error.

The Versal architecture (AMD) uses a 7 nm fabrication process, compared to a 16 nm process for AMD's previous architecture. This work aims at evaluating this architecture for TDL design.

## 2. OPTIMIZATIONS

The configurable logic block (CLB) was changed significantly compared to the previous architecture. Notably, the carry propagation circuit has only 4 outputs compared to 16 in the UltraScale+ architecture. However, these outputs are connected to the look-up-tables (LUTs) allowing for a secondary propagation path.

Even with these changes, optimizations found in previous architectures [2] all apply to the Versal architecture.

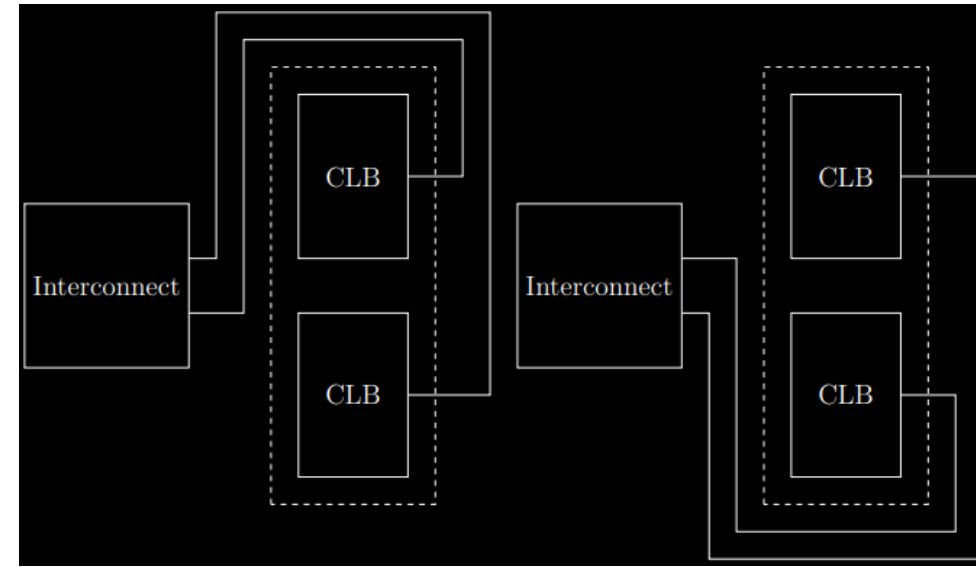


Fig. 1. Device representation of the 4 CLB column pattern. 1 CLB per column is shown.

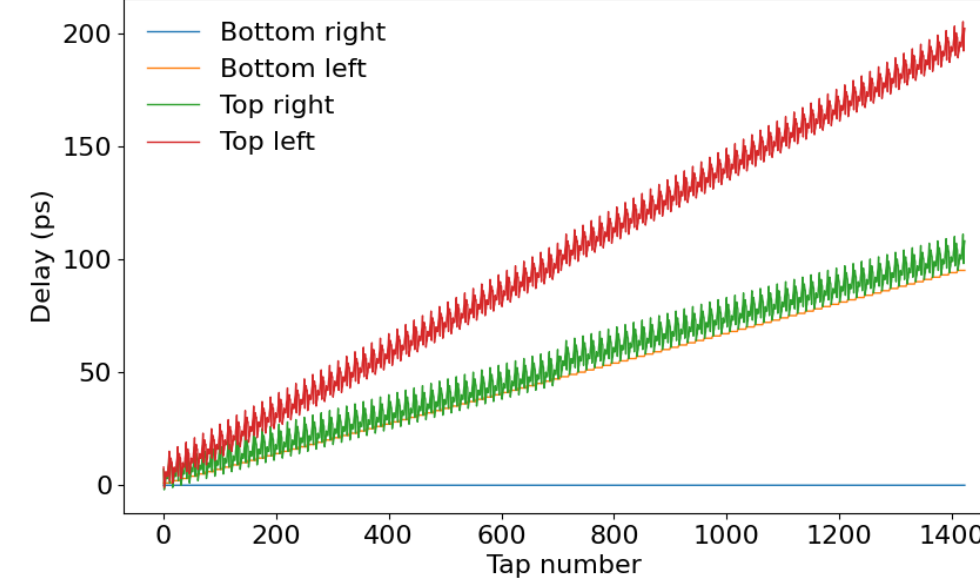


Fig. 2. Delay difference for each CLB column compared to the column with lowest delay.

In addition, the CLB columns are laid out in a repeating pattern containing four columns (see Fig. 1). The propagation delays depend on which column the TDL is implemented in (Fig. 2).

The TDLs were all placed in the column with the lowest propagation delays.

## 3. TAPPED DELAY LINE DESIGNS

### Only Lookahead8 outputs

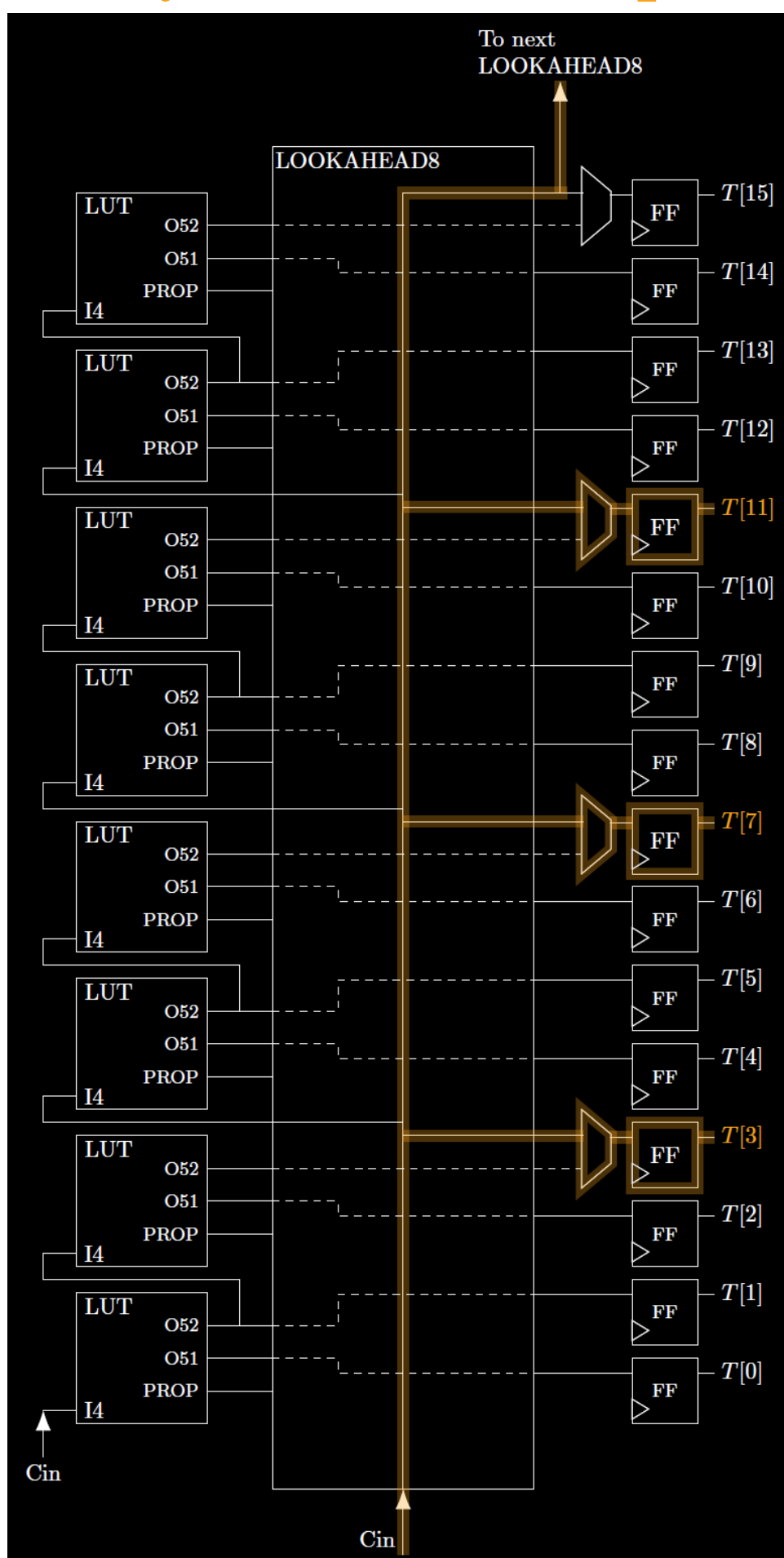


Fig. 3. In this design, the signal propagates only in the carry propagation circuit and its outputs are connected. Note that the top flip-flop cannot be used when forwarding the carry output to next CLB.

### Only LUT outputs

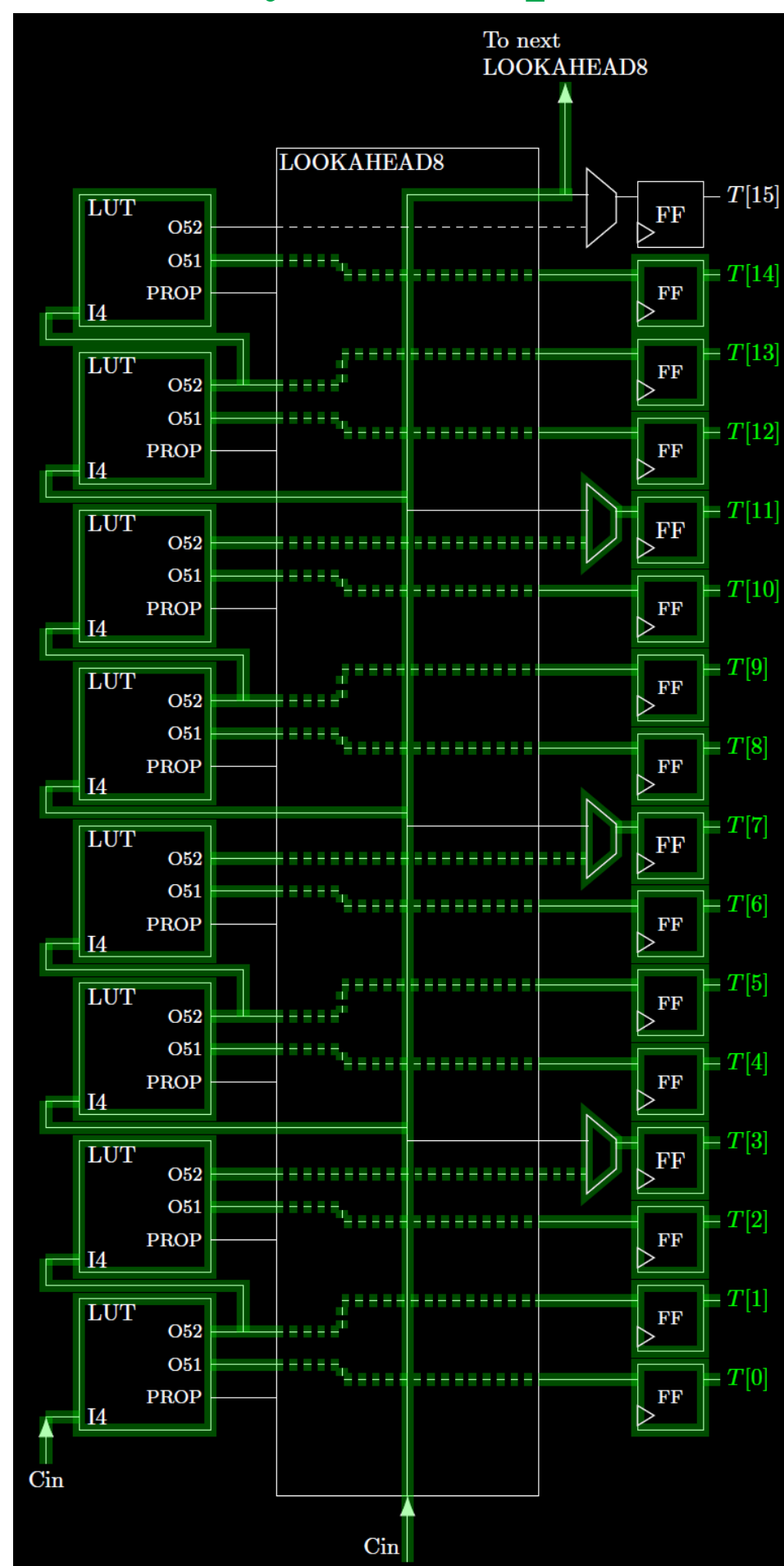


Fig. 4. In this design, the signal propagates through both the LUT and the carry propagation circuit, but only the LUT outputs are connected.

### Hybrid

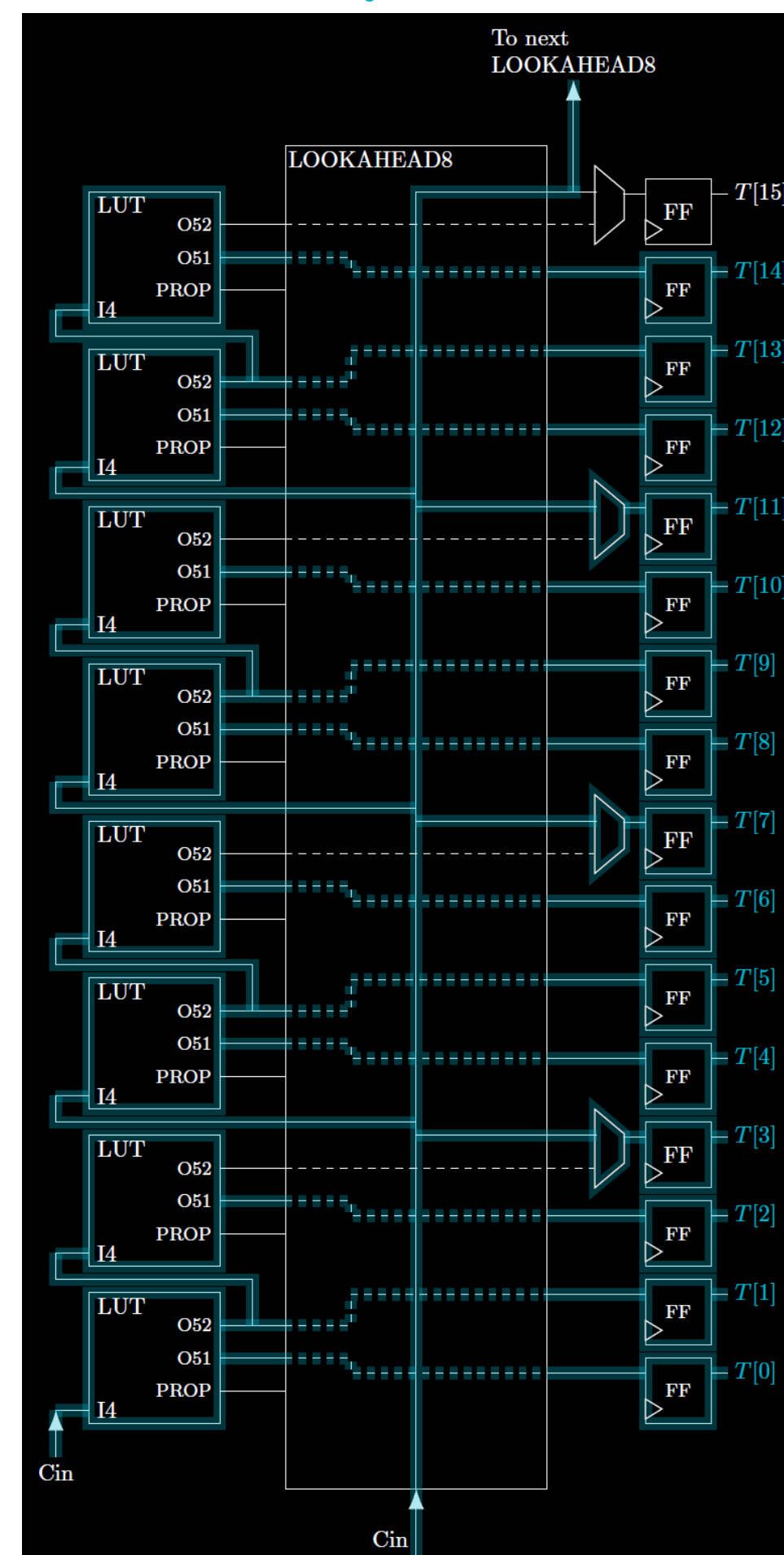


Fig. 5. In this design, the signal propagates through both the LUT and the carry propagation circuit and a mix of outputs are connected.

## 4. METHODOLOGY

Two TDLs were implemented for all 3 designs, targeting a Versal xcvm1802-2 SoC. Each TDL is made of 95 CLBs contained in a single clock region.

The delays  $D$  to each tap and the clock skew  $S$  for each flip-flop were extracted from AMD's toolchain. Taps were ordered based on their bin start time ( $D-S$ ) and bin widths  $W$  computed using:

$$W[n] = \Delta D[n] - \Delta S[n].$$

From these bin widths, a code density using a 700 MHz clock was generated. Allowing to compute the number of used bins ( $N$ ) and the resolution (LSB).

Then, the quantization error  $\sigma_q$  was computed using:

$$\sigma_q = \sqrt{\frac{1}{12 \times N \times LSB} \sum_{n=0}^{N-1} W[n]^3}.$$

The bin widths were used to obtain a conversion from time to code then from code to digitized time for each TDL. Two of these simulated TDLs were used to digitize 5 million pairs of events with a time difference uniformly distributed in a 5 ns range. In addition, a coarse measurement was simulated using a 700 MHz clock with 1.25 ps cycle-to-cycle jitter.

The precision of each design was then computed by taking the standard deviation of the error between the digitized time difference and the expected time difference.

## 5. SIMULATED PERFORMANCE

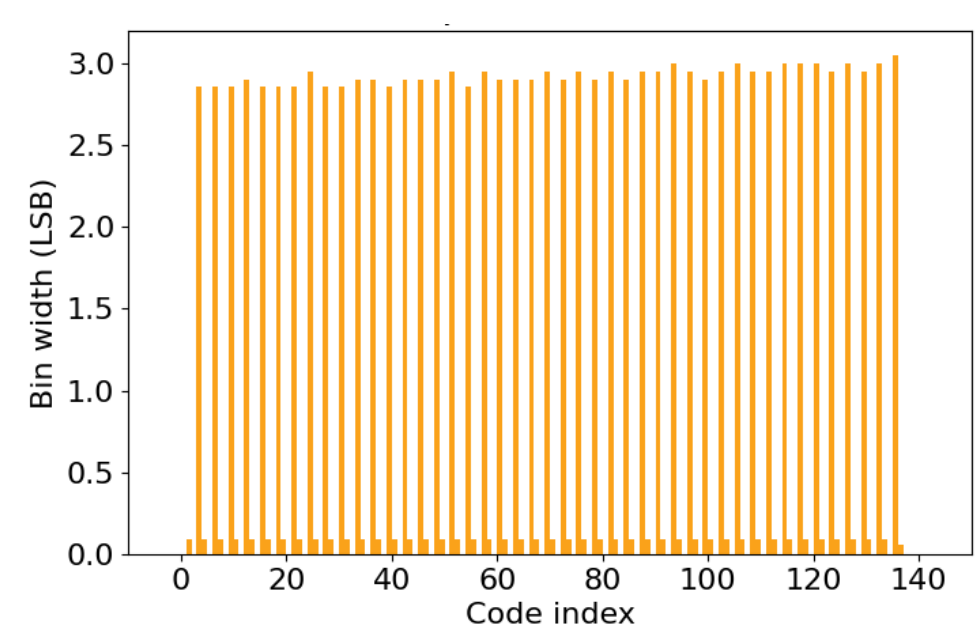


Fig. 6. Code density for the only lookahead design.

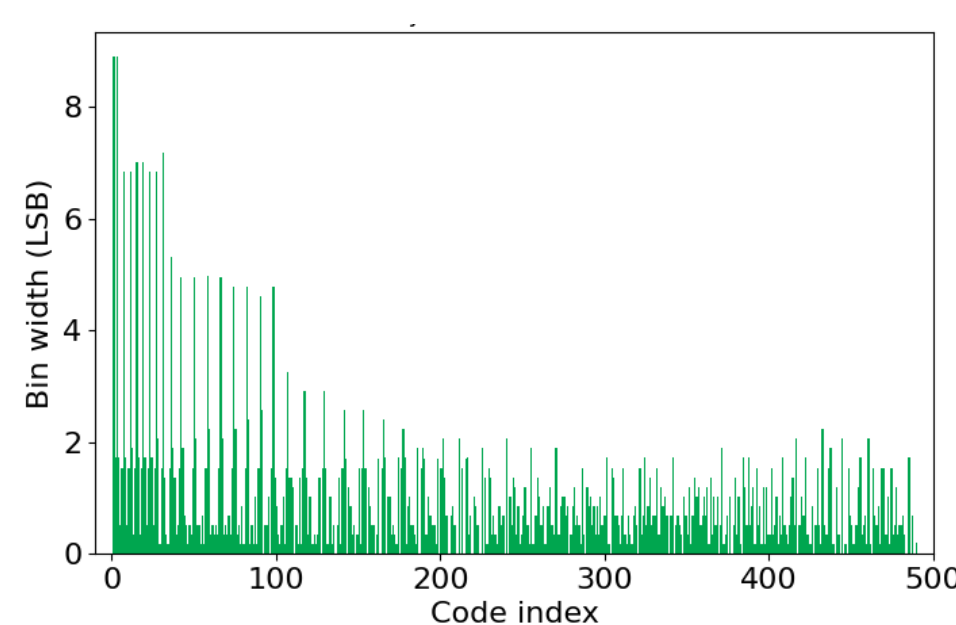


Fig. 7. Code density for the only LUT design.

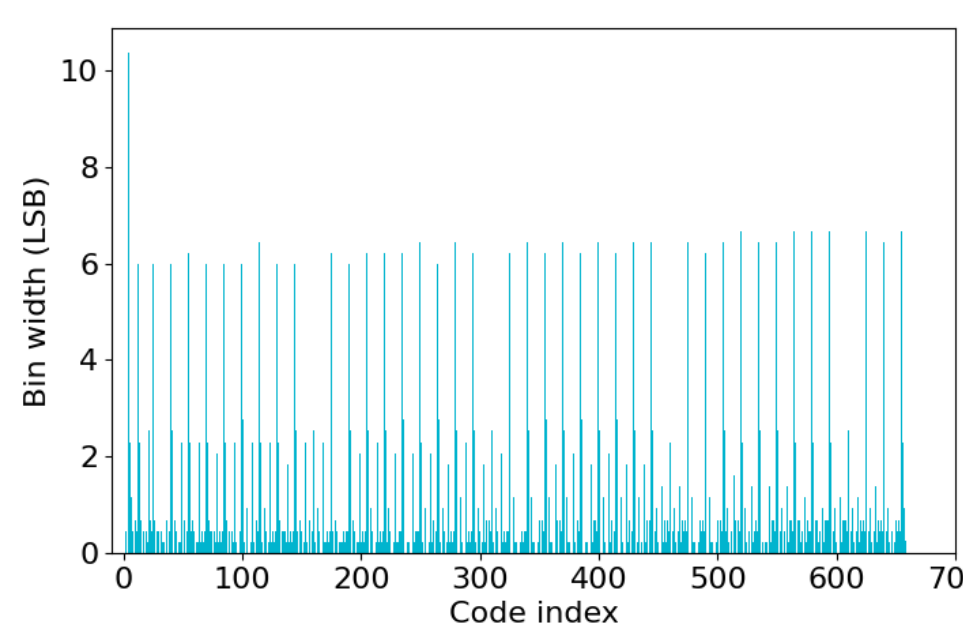


Fig. 8. Code density for the hybrid design.

	Reference UltraScale+	Only Lookahead	Only LUT	Hybrid
Resolution (ps)	1.8	10.5	2.9	2.9
Q error (ps)	1.3	8.7	2.9	2.9
Precision (ps)	2.7	12.5	4.5	4.5

The design using only the lookahead outputs features the best uniformity, but the lower number of taps significantly reduces achievable resolution and precision.

The other two designs have the same resolution, quantization error and precision even if they feature widely different pattern of bin sizes. In all cases, the reference UltraScale+ performs better.

## 6. CONCLUSIONS

- Three different designs of TDL implemented for the Versal architecture were evaluated in simulations.
- The changes to CLB design counteracts the improvements in fabrication process, thus the Versal architecture does not achieve the same performance as previous architectures.
- As long as all possible flip-flops are used, there is no impact of changing which outputs of the delay line are used.

## References

- [1] H. Xia et al., "A Review of Advancements and Trends in Time-to-Digital Converters Based on FPGA" IEEE T. Instrum. Meas. Vol. 73, June 2024.
- [2] Rossignol et al., "Simulating and Optimizing Tapped Delay Lines for Time-to-digital Converters in FPGA using a Precision Model based on Circuit Characteristics" SSRN 2025.