A Timing-Oriented Pixel Detector ASIC With Delay-Chain-Based Outputs for Three-Dimensional Particle Track Reconstruction

Chunlai Dong[a], Dong Wang[a,*], Hui Wang[a], Ni Fang[a], Shiqiang Zhou[a], Ran Chen[a]
[a]PLAC, Key Laboratory of Quark and Lepton Physics (MOE), Central China Normal University, Wuhan, Hubei 430079, China
* Corresponding author: dongwang@ccnu.edu.cn

Abstract

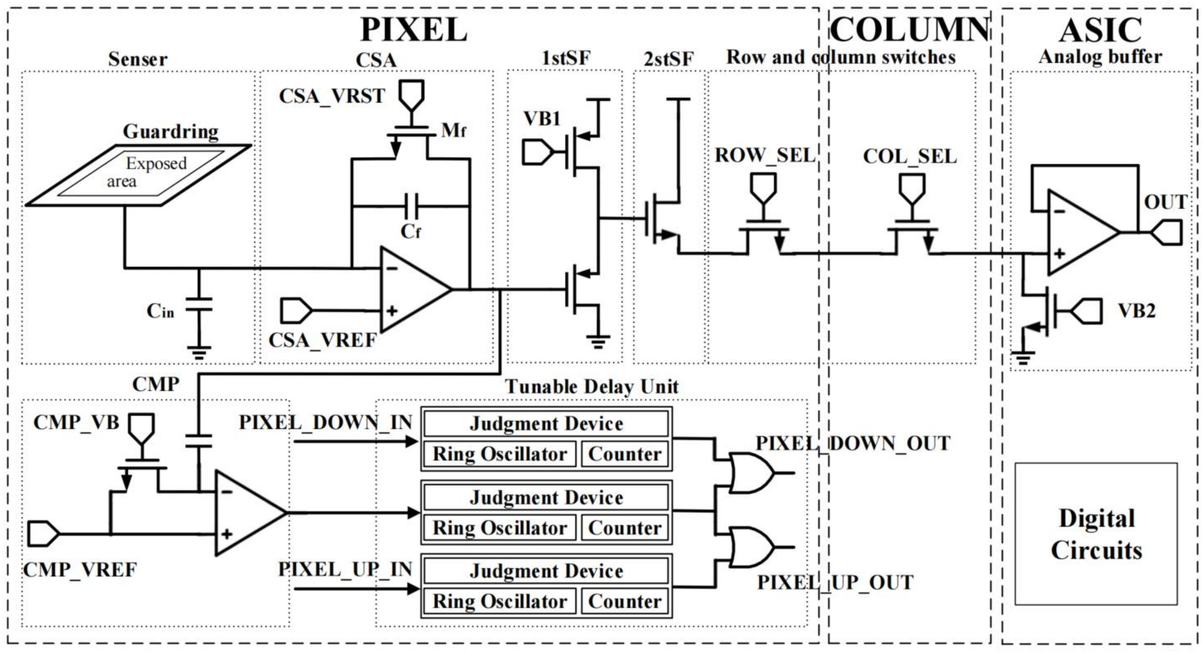
With the growing demand for real-time particle detection and precise event reconstruction, pixel detector readout chips with accurate timing capability for time-resolved particle tracking have become increasingly important. This work presents an energy- and timing-oriented pixel detector ASIC for three-dimensional particle track reconstruction.The chip is fabricated in a GSMC 130 nm CMOS process and implements a 10 × 10 pixel array, occupying a total chip area of 1 mm × 1.5 mm, with each pixel measuring 90 μm × 50 μm. Two on-chip delay chains form the basis of the time measurement scheme, in which three selectable delay stages provide nominal delays of 812 ps, 7.18 ns, and 14.36 ns, respectively, achieving an intrinsic timing resolution of 278.4 ps. Each pixel integrates an analog front-end circuit composed of a low-noise charge-sensitive amplifier, a comparator, and a tunable delay module. The analog front-end achieves an equivalent noise charge of 13.9 e^- and a charge-to-voltage conversion gain of 30.5 μV/e^-. A digital readout circuit implements row–column rolling-shutter scanning across the pixel array. Energy information is digitized by an external ADC, while timing information from on-chip tapped delay-chain outputs is processed in an FPGA to extract time-of-arrival values. The FPGA-processed data are transferred to a host computer for three-dimensional particle track reconstruction. Simulation results based on the proposed architecture demonstrate the feasibility of time-resolved three-dimensional particle tracking.

Pixel Overall Architecture

Pixel level
- Charge-sensitive amplifier (CSA)
- Comparator (CMP)
- Tunable delay unit (TDU)
- Two cascaded source followers (1stSF and 2ndSF)
- Row selection switch

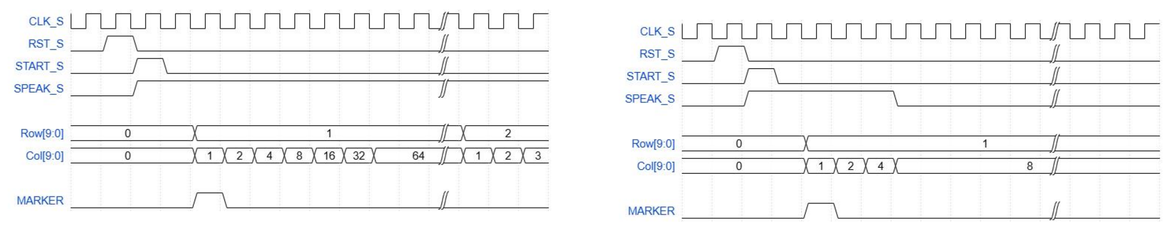
Column level
- Column selection switch

ASIC level
- Analog output buffer
- Digital circuit



Digital Readout Circuit

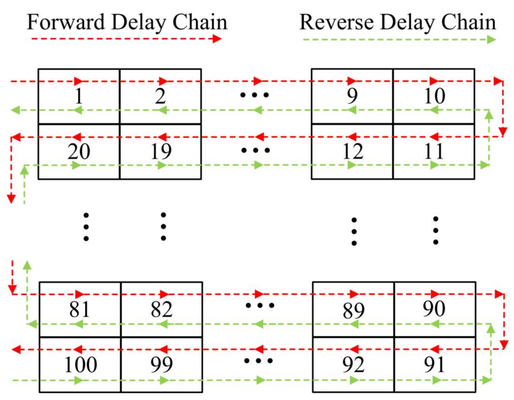
- Implements global control and scan sequencing for the pixel array, coordinating addressing and synchronization with the analog front-end.
- Includes one clock input (CLK_S), three control inputs (RST_S, START_S, SPEAK_S), one marker output (MARKER_A), and two 10-bit row/column addressing outputs.
- Supports a 1–40 MHz clock frequency range, enabling flexible trade-offs between readout speed and power consumption.
- Provides asynchronous reset assertion with synchronous release for stable operation.
- Supports both rolling-shutter full-array scanning and single-pixel addressing modes.
- Row/column outputs are level-shifted from 1.2 V digital logic to 3.3 V pixel-array operation.
- Compact L-shaped layout with an area of approximately 84,582 μm².

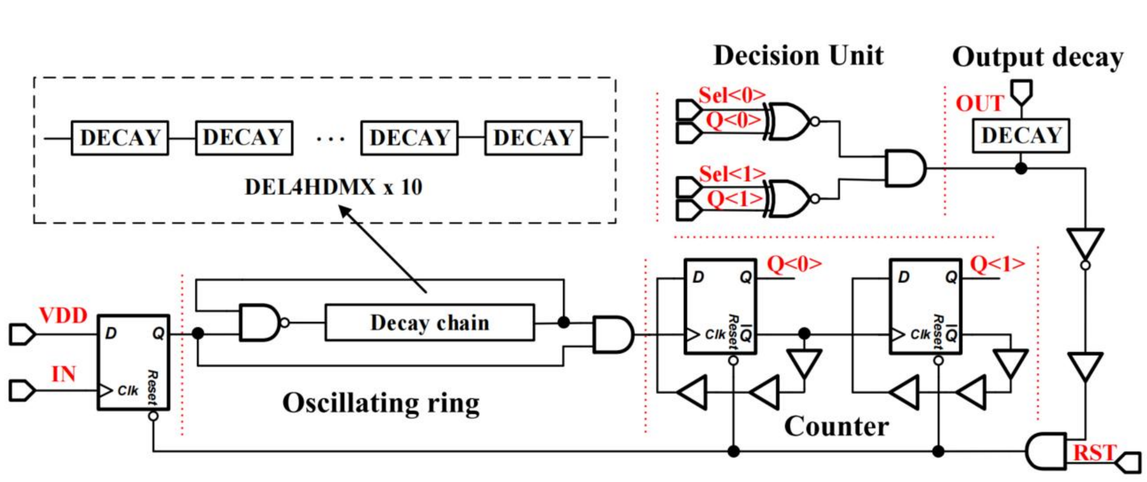


Delay Chain Circuit Design

Design of controllable delay chain circuit structure
- Oscillating ring
- Counter
- Decision unit
- Output delay circuit

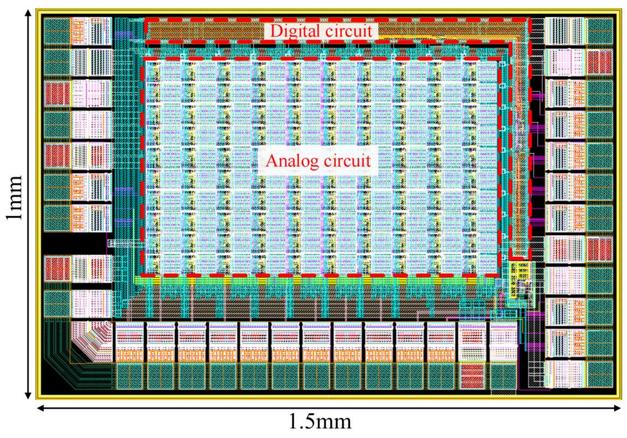
In the design, strategies involving bidirectional paths (down and up)
- 10×10 pixel array



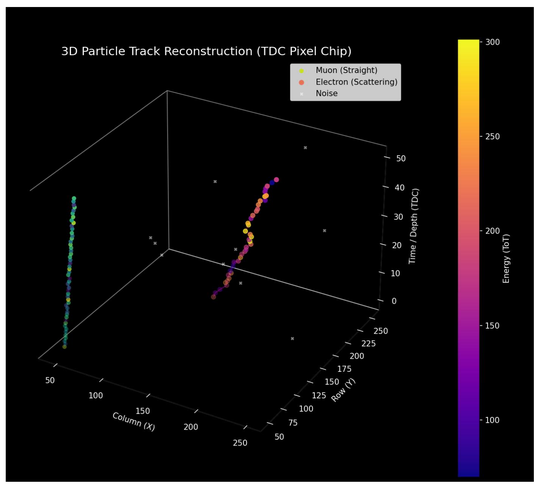


Test Analysis and Results

Chip Layout Summary
- GSMC 130 nm CMOS technology
- Die size: 1 mm × 1.5 mm
- Pixel array: 10 × 10
- Pixel size: 90 μm × 50 μm



Achieved 3D particle track reconstruction using on-chip timing outputs
- Distinguished straight tracks and scattering tracks
- Enabled noise discrimination through spatiotemporal correlation
- Integrated position + timing + energy information for event reconstruction
- Demonstrated feasibility of the proposed TDC pixel architecture



Conclusion

This work presents a timing-oriented pixel detector ASIC for simultaneous energy measurement and 3D particle track reconstruction. Fabricated in GSMC 130 nm CMOS, the chip integrates a 10 × 10 pixel array within an area of 1 mm × 1.5 mm, with each pixel measuring 90 μm × 50 μm. A dual delay-chain architecture with bidirectional signal propagation is proposed for hit localization and precise time extraction, achieving selectable delays of 812 ps, 7.18 ns, and 14.36 ns with an intrinsic timing resolution of 278.4 ps. The analog front-end achieves an equivalent noise charge of 13.9 e^- and a charge gain of 30.5 μV/e^-. Combined with digital rolling-shutter readout and FPGA-based backend processing, the proposed system demonstrates the feasibility of time-resolved 3D particle trajectory reconstruction.

Reference

[1]M. Mager, “ALPIDE, the monolithic active pixel sensor for the ALICI TS upgrade,” Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom.Detect. Assoc. Equip., vol. 824, pp. 434–438, Jul. 2016.

[2]M. Minuti et al., “XPOL-III: A new-generation VLSI CMOS ASIC for high-throughput X-ray polarimetry,” Nucl. Instrum. Methods Phys. Res.A, Accel. Spectrom. Detect. Assoc. Equip., vol. 1046, Jan. 2023, Art. no.167674.

[3]M. Passaseo, E. Petrolo, and S. Veneziano, “A TDC integrated circuit for drift chamber readout,” Nucl. Instrum. Methods Phys. Res. A, Accel.Spectrom. Detect. Assoc. Equip., vol. 367, nos. 1–3, pp. 418–421, Dec.1995.