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Precision analysis and development of timing measurement ASICs for strip LGAD readout

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Introduction

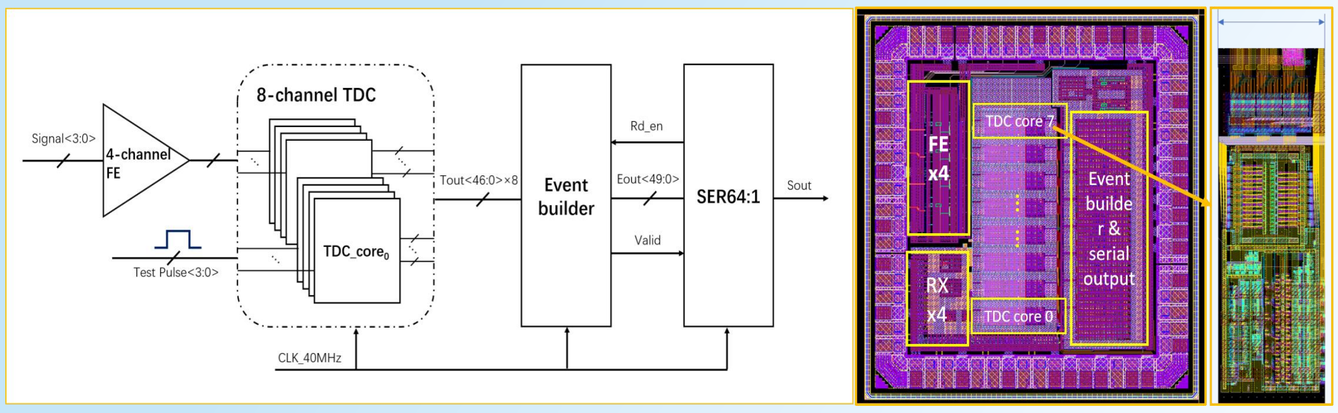

Fig.1. The block diagram of LATRIC1

- LATRIC is a readout chip designed for the Outer Tracker (OTK) of the reference detector on the Circular Electron Positron Collider (CEPC).
- LATRIC1 is an eight-channel version of LATRIC, with channels 0–3 having no preamplifier and channels 4–7 having preamplifiers.
- Channels 0, 1, 4, and 5 use the same TDC core as LATRIC0, while channels 2, 3, 6, and 7 use TDC cores optimized based on test results from LATRIC0.

Circuit Design & Test Setup

- **Timing block**
  - *The TDC core (Fig. 2) comprises three parts: an event-driven ring oscillator with quantization logic, a timing controller, and an encoder, supporting simultaneous TOA, TOT, and CAL measurements.*
  - *The ring oscillator uses 15 NANDs. Each delay cell can provide an average delay of 30 ps. Only the first stage has an enable signal (RO_key) to start the oscillating.*
  - *SR latches are used to capture time information upon event occurrence.*
  - *The optimized TDC core features improvements in the quantization logic, increased device dimensions, and an optimized layout to reduce nonlinearity caused by process variations.*

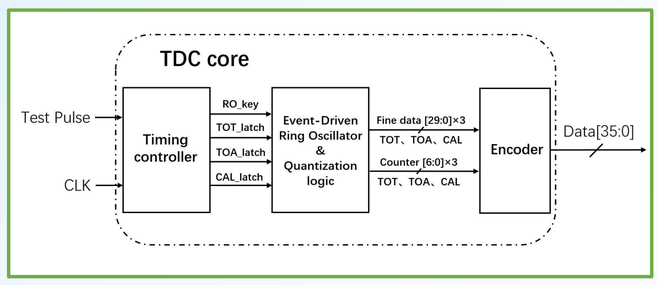

Fig.2. TDC core

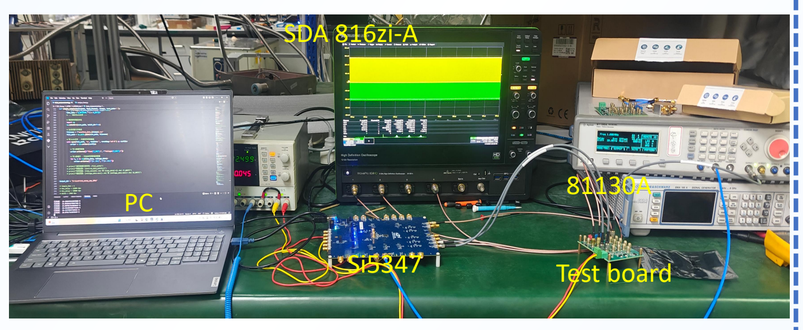

Fig.3. Test setup

- **The test setup**
  - *The Si5347 clock board generates a 40 MHz clock for both serialization and TOA measurement.*
  - *For the TDC core measurement, the Si5347 supplies a 5 MHz clock to trigger a pulse/pattern generator (81130A).*
  - *The pulse width and the delay with the synchronized clock are adjustable for TOT and TOA transfer curve scanning, respectively.*

Measurement and Analysis （TOA)

- **Jitter VS bin-size**
  - *During the test of LATRIC0, multiple TOA measurements of a pulse signal resulted in three types of distributions, as shown in Fig. 4.*
  - *When σ_{Delay} is significantly smaller than the bin size, the distributions resemble cases A and B; when σ_{Delay} is significantly larger than the bin size, the distribution resembles case C.*
  - *σ_{Delay} includes the jitter from the signal source (15 ps) and the jitter introduced by the time measurement circuit.*

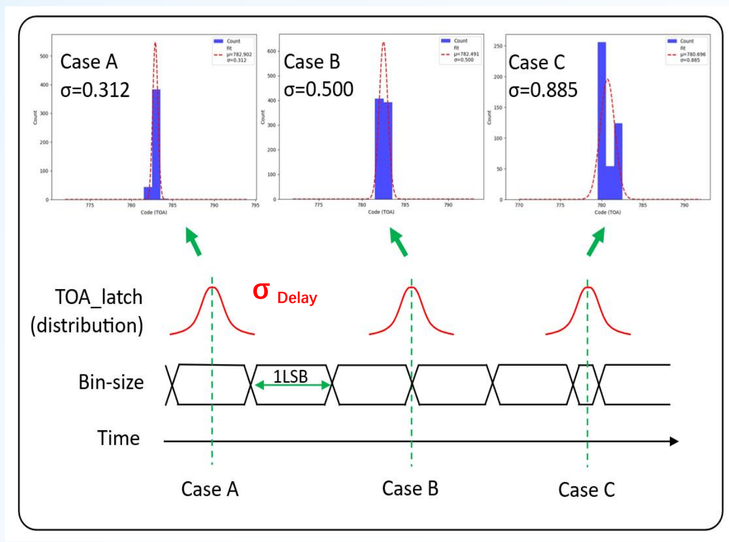

Fig.4. Three distribution patterns observed in LATRIC0 testing

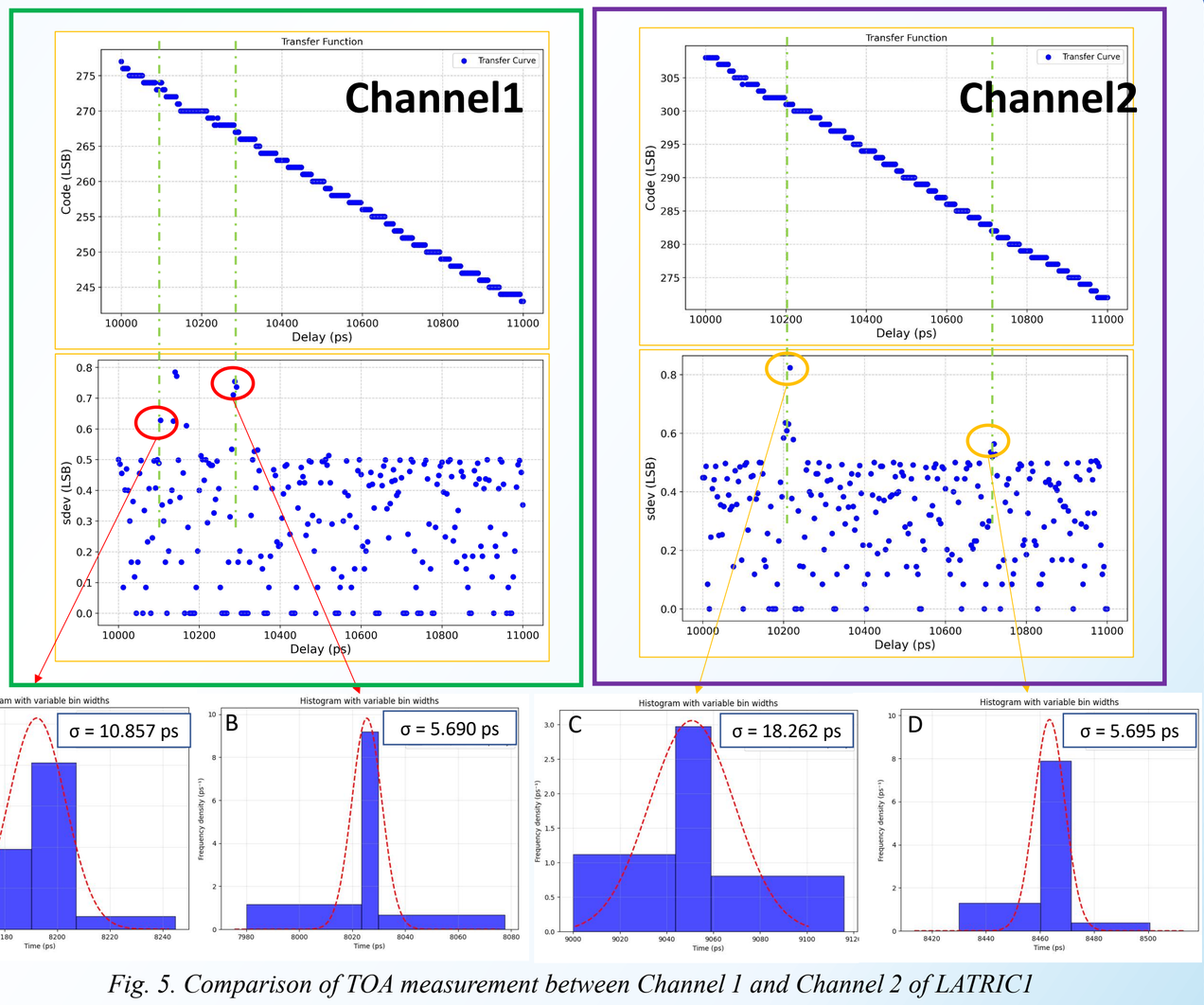

Fig. 5. Comparison of TOA measurement between Channel 1 and Channel 2 of LATRIC1

- **Precision analysis**
  - *During LATRIC1 testing, the signal source jitter is 5.7 ps. The worst-case distribution sdev of the TDC cores (Channel 1 and Channel 2) is 0.823 LSB, which is better than σ = 0.885 LSB of LATRIC0 Case C.*
  - *Channel 1 has an average LSB of 29.8 ps, and Channel 2 has 27.8 ps. The difference between the maximum and minimum bin-size is 60 ps for Channel 1 and 46 ps for Channel 2, as shown in Fig.6.*
  - *Compared with Fig.5.B and 5.D, the increase in the sdev caused by small bin sizes is alleviated.*
  - *Fig.5.A and 5.C indicate that for some code, the jitter introduced by the circuit is larger, pointing to directions for circuit optimization.*

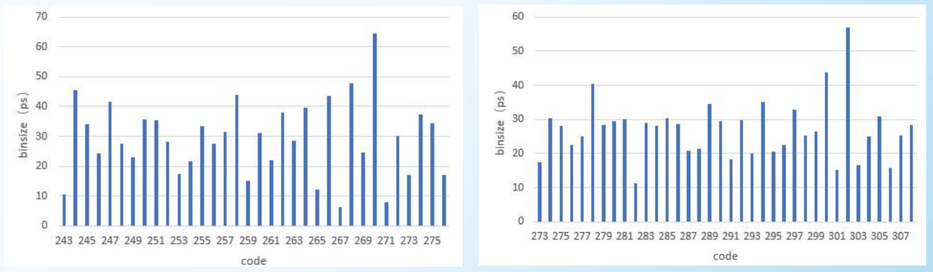

Fig. 6. Bin size vs. code for Channel 1 and Channel 2 of LATRIC1

Conclusion and outlook

This paper presents the design and precision analysis of LATRIC1. To suppress nonlinearity caused by process variations, the TDC core is improved with optimized quantization logic, increased device dimensions, and an enhanced layout. The optimized TDC core achieves an average LSB of 27.8 ps, and the nonlinearity issue is alleviated. However, significant circuit-induced jitter is still observed for certain code words, pointing to directions for further circuit optimization.