Operations and Performance of the ATLAS Tile Calorimeter Phase-II Upgrade Demonstrator in Run 3

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***Abstract*—The ATLAS Tile Calorimeter (TileCal) will undergo a major replacement of its on-detector and off-detector electronics for operation at the High-Luminosity Large Hadron Collider (HL-LHC). The upgraded system will provide fully digital calorimeter data for every bunch crossing to the new ATLAS Trigger and Data Acquisition architecture while improving bandwidth, radiation tolerance, timing distribution and operational flexibility. As part of this program, a Demonstrator module equipped with Phase-II electronics was installed in ATLAS and operated during Run 3 while maintaining compatibility with the present trigger, readout and detector control infrastructure.**

The Demonstrator provided a unique system-level validation of the upgraded detector readout and trigger architecture under real detector conditions. The module includes upgraded 3-in-1 cards, MainBoards, DaughterBoards, high voltage distribution and dedicated off-detector electronics. During Run 3, the Demonstrator was initially operated through the Tile Pre-Processor Demonstrator while maintaining the legacy readout path required for backward compatibility. In 2024–2025, the system was migrated to the Compact Processing Module and Carrier boards, and FELIX was integrated for clock, trigger, and configuration distribution as a step toward the final Phase-II architecture. This work presents the Demonstrator electronics and readout architecture, its evolution during Run 3, and the operational performance evaluated using calibration and detector data. Results from Charge Injection, Laser, Cesium, timing and detector monitoring demonstrate stable operation of the upgraded electronics and provide direct validation of the technologies, operational procedures and readout concepts required for the final TileCal Phase-II system.

***Index Terms*—ATLAS Tile Calorimeter (TileCal), Data Acquisition (DAQ) systems, Field-Programmable Gate Array (FPGA), High Energy Physics (HEP), High-Speed Electronics.**

I. Introduction

THE Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS experiment [1] [2], covering the pseudorapidity region $|\eta| < 1.7$. TileCal is a sampling calorimeter based on steel absorber plates and plastic scintillating tiles as active material, and contributes to the reconstruction of jets, hadronically decaying tau leptons and missing transverse energy.

As shown in Fig. 1, TileCal is organized in three cylindrical sections along the beam axis: one central Long Barrel and two Extended Barrels, subdivided into four readout partitions (LBA, LBC, EBA and EBC). The detector is composed of 256 wedge-shaped modules distributed azimuthally, each integrating the photomultiplier tubes (PMTs) and detector readout electronics in the outermost region of the module. The scintillation light produced in the active material is collected and transmitted to the PMTs through wavelength-shifting fibers. The complete detector readout is performed using approximately 10,000 PMT channels, which also provide information to the calorimeter trigger system.

The High-Luminosity Large Hadron Collider (HL-LHC), expected to operate from 2030 to 2041, will significantly increase the instantaneous luminosity and the number of simultaneous interactions per bunch crossing. These conditions impose stronger requirements on the detector readout and trigger input bandwidths, radiation tolerance, and long-term operational stability. The TileCal Phase-II Upgrade therefore replaces the present on-detector and off-detector electronics with a new readout architecture [3]. In the upgraded system, the PMT signals are digitized on the detector and transmitted continuously to off-detector electronics at the accelerator bunch-crossing frequency. The off-detector electronics then buffer the digitized samples, reconstruct calibrated cell quantities, distribute timing and configuration information, and interface with the ATLAS Trigger and Data Acquisition (TDAQ) systems.

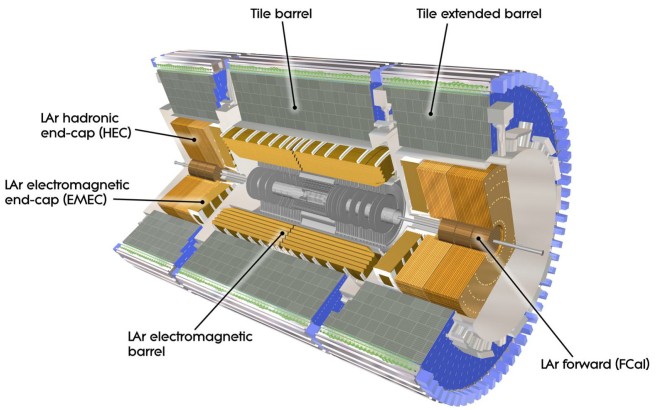

Fig. 1: ATLAS calorimeters. TileCal is composed of one central Long Barrel and two Extended Barrels [1].

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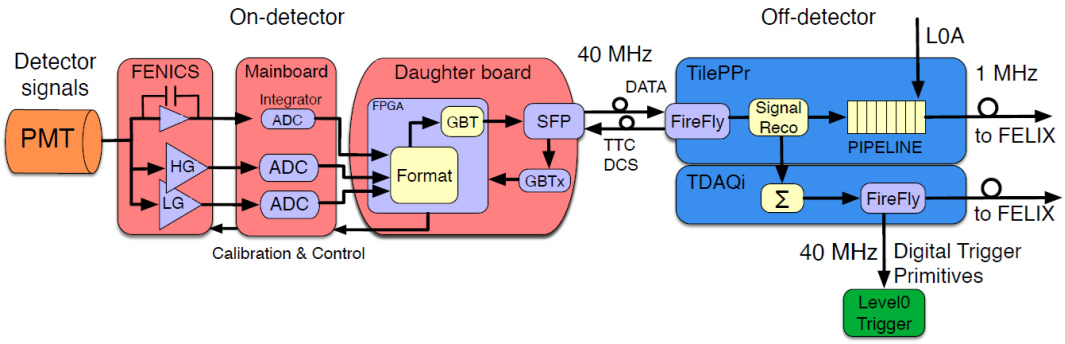


Fig. 2: TileCal Phase-II readout architecture illustrating the final electronics chain [4].

II. TileCal Phase-II Trigger and Readout Architecture

The TileCal Phase-II Upgrade introduces a fully digital architecture in which detector data are digitized directly on the detector and transmitted continuously to off-detector electronics for processing, buffering and trigger generation. The final Phase-II readout architecture is summarized in Fig. 2. The upgrade deployment is planned to take place during the HL-LHC installation period between 2026 and 2030 and will replace the present detector readout and trigger interfaces with the final Phase-II electronics architecture.

The Demonstrator program was established to validate the upgraded electronics under realistic detector conditions before large-scale installation.

In the final HL-LHC system, the electronics connected to each PMT shapes and amplifies the analog signal in two gains. The signals are digitized in the on-detector electronics and transmitted through high-speed optical links to off-detector PreProcessor electronics located in the counting rooms. The off-detector electronics receive the digitized data for every bunch crossing and distribute the LHC clock and configuration commands to the detector. The digitized samples are buffered in pipeline memories and processed to reconstruct calibrated cell quantities for trigger processing, while selected events are transmitted after a trigger accept.

The upgraded on-detector electronics are organized in Minidrawers [3]. Each Minidrawer hosts the PMT blocks and the electronics required to read out up to twelve PMT channels. The final Phase-II system uses Front-End Board for the New Infrastructure with Calibration and signal Shaping (FENICS) cards [5], MainBoards [6], DaughterBoards [7], high-voltage distribution and low-voltage power distribution. The MainBoard digitizes the two gain outputs and controls the front-end electronics. The DaughterBoard receives the digitized samples, handles timing and control, and transmits detector data to the off-detector electronics using fixed-latency optical links.

The off-detector PreProcessor system is based on Advanced Telecommunications Computing Architecture (ATCA) technology. The final TileCal PreProcessor [8] blade is composed of Compact Processing Modules installed on an ATCA Carrier board. The Compact Processing Module performs high-speed data acquisition, clock and configuration distribution, data buffering and reconstruction. It receives detector data from the DaughterBoards through uplinks operating at 9.6 Gb/s and sends clock, timing and configuration commands through downlinks operating at 4.8 Gb/s. The same module stores the detector samples and reconstructed quantities in pipeline memories until the reception of a trigger accept.

The upgraded trigger and readout architecture also introduces interfaces to the Front-End Link eXchange (FELIX) [9] system and to the Trigger and Data Acquisition Interface (TDAQi) boards. FELIX provides the interface to the ATLAS readout system and distributes trigger, timing and control information throughout the detector electronics chain. The PreProcessor transmits triggered detector event fragments to FELIX at trigger acceptance rates of up to 1 MHz. The TDAQi boards, implemented as an ATCA Rear Transition Module (RTM) connected to the PreProcessor blade, receive the reconstructed and calibrated calorimeter cell energies continuously at the accelerator bunch-crossing frequency. These reconstructed detector quantities are used to generate trigger primitives for real-time trigger processing.

In the upgraded architecture, the trigger primitives generated by the TDAQi are transmitted to the first-level trigger system, including both calorimeter trigger processors (FEXes) and the muon trigger chain, and are also provided to the Global Trigger system [10].

This architecture allows the TileCal system to provide full-granularity digital information to the upgraded ATLAS trigger while preserving deterministic timing between the detector and the off-detector electronics and enabling trigger decisions to exploit reconstructed calorimeter information at every bunch crossing.

The final system will require the production, integration and commissioning of several thousand on-detector electronics boards and the complete replacement of the off-detector readout infrastructure.

The on-detector electronics include approximately 10,000 refurbished PMT blocks equipped with upgraded PMTs, Active Dividers and Front-End Boards (FEBs), read out through 896 MainBoards and DaughterBoards and powered by a new power distribution system. In addition, approximately 10% of the PMT blocks located in the most radiation-exposed detector regions will be replaced.

The off-detector system is based on the deployment of 32

PreProcessor ATCA blades together with 32 TDAQi RTMs and 256 High Voltage (HV) control and regulation boards providing individual monitoring and control of the PMT operating voltages.

A. Demonstrator Program

The complexity and scale of the TileCal Phase-II Upgrade motivated the development of the Demonstrator program as a staged validation strategy, allowing progressive qualification of the upgraded electronics and operational concepts under realistic detector conditions before large-scale installation during the HL-LHC shutdown period.

The Demonstrator module was assembled and qualified through several dedicated test beam campaigns and subsequently installed in the ATLAS detector during Long Shutdown 2 in 2019. The installed Demonstrator module is shown in Fig. 3.

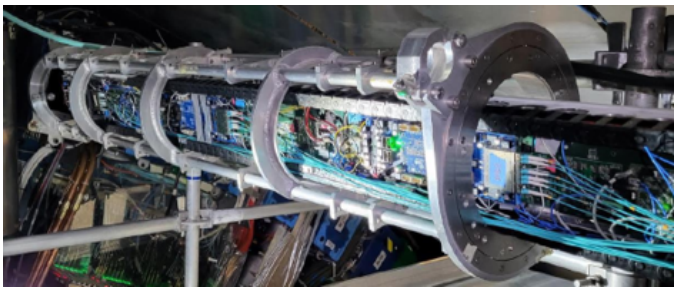


Fig. 3: Demonstrator module extracted during maintenance showing the Minidrawer mechanics and upgraded detector electronics [11].

During Run 3 (2022–2026), the Demonstrator was operated within the ATLAS detector using a hybrid architecture combining upgraded detector electronics with compatibility interfaces to the existing trigger and readout systems, enabling validation of the Phase-II detector electronics and strategy, while preserving compatibility with the current ATLAS TDAQ infrastructure.

III. Demonstrator Module Electronics and Evolution

As introduced in section II, the Demonstrator module was designed as a hybrid TileCal module to remain compatible with the existing ATLAS trigger and readout infrastructure. Therefore, the readout electronics chain is not identical to the final HL-LHC implementation at every stage. The most important difference between the Demonstrator and the Phase-II electronics is the use of upgraded 3-in-1 cards instead of the final FENICS cards, since the Demonstrator must continue to provide analog trigger signals to the current Level-1 calorimeter trigger.

A. Minidrawer Support

The upgraded TileCal readout electronics are organized in independent units called Minidrawers, where Long Barrel modules are composed of four Minidrawers, and Extended Barrel modules are composed of three Minidrawers. Each Minidrawer contains up to twelve PMT blocks together with one MainBoard, one DaughterBoard and the associated HV and Low Voltage (LV) distribution. This modular organization improves detector maintainability, fault tolerance through additional redundancy, and operational flexibility. An example of the mechanical and electronics layout of one Demonstrator Minidrawer is shown in Fig. 4.

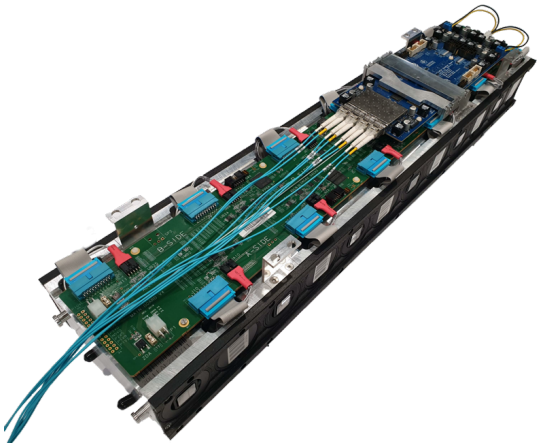


Fig. 4: Picture of one of the Minidrawers of the Tile Demonstrator [11].

B. High Voltage and Low Voltage Power Distribution

The Demonstrator and final Phase-II electronics also introduce a complete redesign of the detector power distribution system.

The HV architecture provides individual control, regulation and monitoring of the PMT operating voltage at channel level. Unlike the current HV system, the upgraded architecture moves HV regulation off-detector, making the active electronics more accessible for maintenance. The on-detector HV infrastructure is reduced to passive distribution of the regulated HV to the PMTs, thereby increasing system reliability by reducing the amount of active electronics installed inside the detector.

The LV Power Supply (LVPS) system has also been upgraded to support the increased functionality and power requirements of the upgraded electronics chain. The LVPS system distributes 10 V to separate sides of the on-detector electronics through independent power bricks in order to preserve the readout segmentation and improve operational robustness. Long Barrel modules are powered through eight LVPS bricks, while Extended Barrel modules employ six LVPS bricks. Since the Demonstrator is installed in the Long Barrel, its LVPS includes eight LVPS bricks, following the Long Barrel implementation for Phase-II.

The upgraded LVPS design was developed using strict qualification procedures for radiation tolerance, since part of the power distribution system is installed in some of the detector regions exposed to the highest radiation levels. Dedicated validation campaigns were therefore performed for the electronic components to ensure reliable long-term operation under HL-LHC conditions.

C. Photomultiplier block

The PMT block constitutes the fundamental readout unit in TileCal. Its function is to collect the optical signal produced in the scintillating tiles, convert it into an electrical signal and perform the first stage of analog processing before digitization.

Each PMT block integrates one optical beam expander, one Hamamatsu PMT, one Active Divider and one FEB.

The Demonstrator PMT blocks are equipped with Hamamatsu R11187 PMTs. This model was selected for the replacement of the PMTs in the most exposed regions of the detector to improve detector response stability and uniformity during the HL-LHC period. The Active Dividers apply stable dynode voltages, improving PMT linearity and gain stability during sustained current operation and large detector signals.

The final element of the PMT block is the FEB. The FEB receives the PMT output signal and performs the first stage of analog signal conditioning before digitization. While the final TileCal Phase-II architecture integrates FENICS within the PMT block, the Demonstrator employed the upgraded 3-in-1 card in order to preserve compatibility with the present Level-1 trigger system.

The upgraded 3-in-1 card functionality includes pulse shaping, bi-gain amplification with a gain ratio of 1:32, Charge Injection calibration and slow integrator readout. The two gain outputs are transmitted to the MainBoard for digitization. In parallel, the slow integrator path provides average PMT current measurements used for calibration and detector monitoring. The analog trigger outputs generated by the upgraded 3-in-1 are summed through the legacy trigger path and transmitted to the current Level-1 calorimeter trigger via electrical cables.

D. MainBoard

The MainBoard digitizes the signals from the twelve PMT blocks of one Minidrawer. For each PMT channel, the two gain outputs are digitized by 12-bit ADCs at 40 MS/s. The slow integrator signal is digitized using a 16-bit ADC. The MainBoard also hosts Field-Programmable Gate Array (FPGA) logic used to control and configure the FEBs.

The digitized samples are transferred from the MainBoard to the DaughterBoard through LVDS lines for every bunch crossing. This interface is the boundary between the local digitization performed in the Minidrawer and the high-speed optical readout implemented by the DaughterBoard.

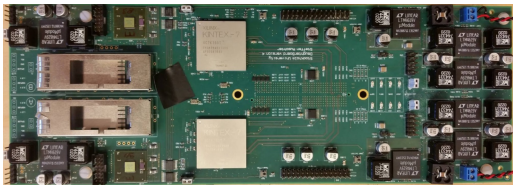
E. DaughterBoard

The DaughterBoard receives the digitized samples from the MainBoard, formats the data and transmits them to the off-detector electronics. It also receives timing, control and configuration commands from the off-detector system and distributes the recovered clock to the on-detector electronics for the digitization of the PMT signals.

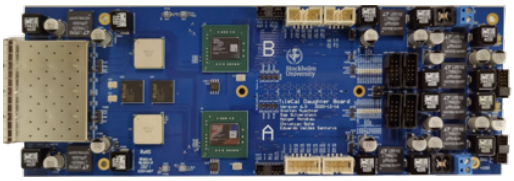
The initial Demonstrator implementation used DaughterBoard version 4 (DBv4). DBv4 was equipped with two Xilinx Kintex-7 FPGAs, two Gigabit Transceiver (GBTx) [12], [13] ASICs and quad small form-factor pluggable (QSFP) optical modules. The GBTx ASIC recovered the LHC clock with fixed and deterministic latency, which was then distributed for ADC sampling and used as reference for the FPGA high-speed transceivers.

During the evolution of the Demonstrator toward the final Phase-II system, the on-detector readout was updated to DaughterBoard version 6.1 (DBv6.1). DBv6.1 adopts the FPGA technology and device selection foreseen for the final system and is equipped with two Xilinx Kintex UltraScale XCKU035 FPGAs, two Microchip ProASIC3E devices, two GBTx ASICs and four small form-factor pluggable (SFP) optical modules. The evolution from DBv4 to DBv6.1 is illustrated in Fig. 5.

The Kintex UltraScale devices implement the detector data processing and communication functions, while the ProASIC3E devices provide detector control and supervision functions of the DaughterBoard. This represents a significant convergence with the final electronics solution. The optical interface also evolved from the QSFP-based connectivity used in earlier Demonstrator implementations toward the SFP-based solution adopted in the later system and foreseen for the final Phase-II architecture.



(a) DaughterBoard version 4 (DBv4).



(b) DaughterBoard version 6.1 (DBv6.1).

Fig. 5: Evolution of the Demonstrator DaughterBoard implementation. DBv4 (top) was used during the initial Demonstrator operation, while DBv6.1 (bottom) adopts the FPGA technology and optical connectivity foreseen for the final TileCal Phase-II detector electronics [3] [7].

The DaughterBoard transmits the detector data to the off-detector electronics through redundant high-speed uplinks operating at 9.6 Gb/s. The downlink from the off-detector electronics operates at 4.8 Gb/s and carries timing, control and configuration information. The use of fixed-latency GBT links is essential to maintain deterministic synchronization between the LHC clock, the digitization of PMT signals and the off-detector pipeline.

IV. Off-Detector Readout and Evolution During Run 3

The off-detector readout architecture evolved during Run 3 while keeping the legacy readout path required for detector operation. The legacy Read-Out Driver (ROD) remained part of the operational chain for backward compatibility. The changes

introduced during Run 3 concerned the upgraded readout, clock and configuration path, which evolved from the Tile PreProcessor Demonstrator toward the Compact Processing Module (CPM), Carrier and FELIX-based architecture without interrupting standard detector running.

A. Tile PreProcessor Demonstrator

The Tile PreProcessor Demonstrator was the original off-detector board used to operate the Demonstrator module. It controlled and read out the Demonstrator, propagated the LHC clock to the on-detector electronics and acted as a bridge between the upgraded electronics and the current ATLAS TDAQ, Trigger, Timing and Control (TTC) and readout systems.

The Tile PreProcessor Demonstrator was a double mid-size Advanced Mezzanine Card (AMC) [14] equipped with two FPGAs: a Xilinx Virtex-7 readout FPGA and a Xilinx Kintex-7 trigger FPGA; and four QSFP modules. The Tile PreProcessor Demonstrator board used during the initial Run 3 operation is shown in Fig. 6.

The readout FPGA interfaced with QSFP modules providing high-speed communication with the on-detector electronics through links operating at 4.8/9.6 Gb/s. Communication with the legacy ROD and with the detector control infrastructure was performed through a dedicated RTM connected through the Tile PreProcessor backplane ports. In this implementation, the RTM acted as a passive distribution interface and did not perform detector data processing. The TTC clock and commands were recovered independently through a dedicated optical receiver based on a photodiode, an Analog Devices ADN2814 device and dedicated firmware in the readout FPGA. The trigger FPGA was intended for the development of preprocessing algorithms for the HL-LHC but was not used for the standard operation of the Demonstrator.

This implementation allowed the Demonstrator to run in ATLAS while transmitting compatible event data to the legacy readout system. The system received digitized samples from the Demonstrator at the LHC frequency and transmitted triggered event fragments to the legacy ROD. The ROD interface therefore remained the operational compatibility path with the current TileCal DAQ.

B. Compact Processing Module

During the 2024–2025 maintenance period, the Demonstrator off-detector electronics was upgraded by replacing the Tile PreProcessor Demonstrator with a Compact Processing Module, Carrier, TileGbE switch, and integrating the CPM with the FELIX system. This change was a major step toward the final HL-LHC architecture.

The CPM, shown in Fig. 7, is the final off-detector processing element for the TileCal Phase-II system. It receives detector data from the DaughterBoards, distributes the LHC clock and configuration commands, stores detector samples in pipeline memories and provides interfaces to FELIX and the trigger/readout infrastructure. In the Demonstrator, the CPM provided an operational test of the final processing architecture while still preserving the legacy ROD path. Communication with the legacy ROD and with FELIX is performed

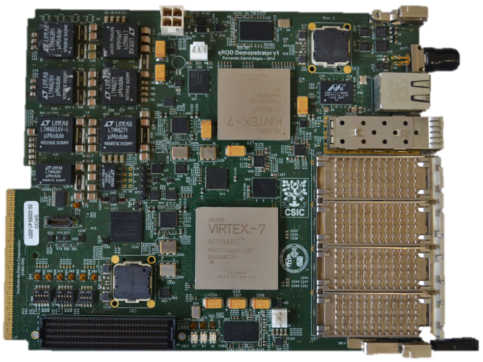


Fig. 6: Picture of the Tile PreProcessor Demonstrator used initially as off-detector electronics in the Demonstrator program [3].

through SFP optical interfaces located on the CPM front panel, while detector control and slow-control communication are implemented through the TileGbE switch installed on the ATCA Carrier and distributed internally through the Carrier backplane.

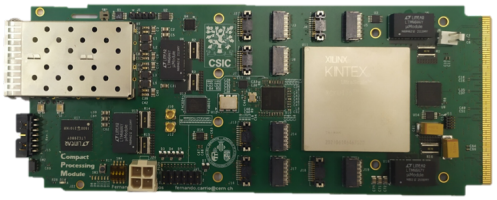


Fig. 7: Picture of the CPM installed on the ATLAS counting rooms implementing the final TileCal Phase-II off-detector architecture [15].

The 2024–2025 evolution also introduced reliance on FELIX for clock and configuration. The LHC clock is recovered from FELIX, and TTC commands including trigger acceptance and bunch configuration are distributed through the upgraded path. The improved readout path is capable of handling two gains, sixteen samples and 12-bit data, while the interface to the ROD is kept for backward compatibility.

V. Data Acquisition Architecture and Detector Operation

The Demonstrator data acquisition architecture starts at the PMT blocks, where the upgraded 3-in-1 card provides bi-gain readout together with a slow integrator path for detector calibration and monitoring. The detector signals are digitized for every bunch crossing in the MainBoard, while analog trigger compatibility is preserved through the legacy trigger path.

The DaughterBoard aggregates detector information, formats detector data using the CERN GBT communication protocol [16] and transmits detector data to the off-detector electronics through fixed-latency optical links operating at

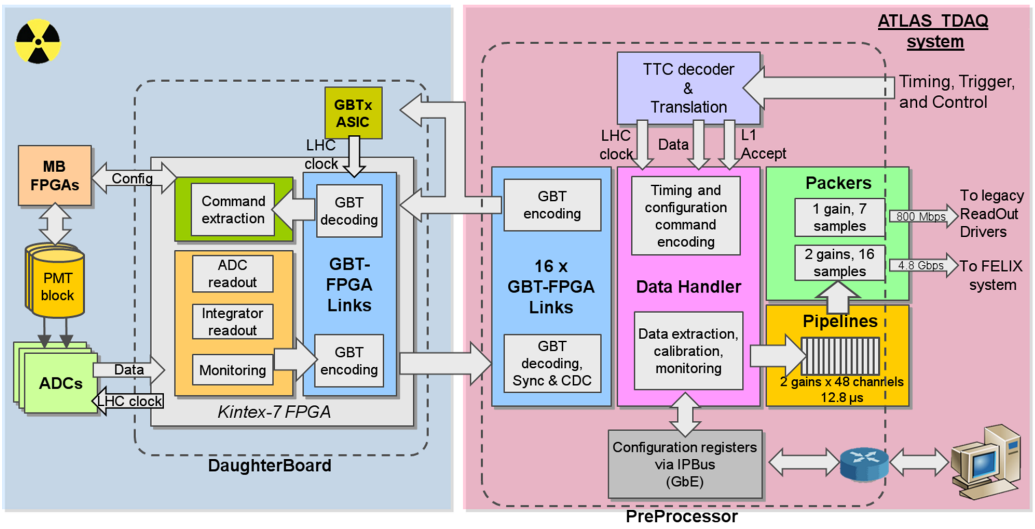


Fig. 8: Block diagram of the main firmware blocks of the Demonstrator data acquisition system, corresponding to the initial architecture with DBv4 as on-detector electronics and the Tile PreProcessor Demonstrator as off-detector processing [15].

9.6 Gb/s while receiving timing, trigger and configuration commands through 4.8 Gb/s downlinks.

Detector timing and synchronization are controlled from the off-detector electronics. In addition to event acquisition, the off-detector system supervises detector configuration, including gain configuration, front-end control, slow integrator readout, calibration execution and detector timing adjustments through clock phase configuration. The detector data are continuously received and stored in pipeline memories implemented as circular buffers until the reception of a trigger acceptance signal, after which the selected event data are transmitted to the subsequent stages of the readout chain. The pipeline memories provide a buffering depth of 12.8 μs, exceeding the minimum Phase-II requirement of 10 μs.

The off-detector electronics distribute the recovered LHC clock together with TTC commands including trigger accept signals, bunch crossing reset and event reset commands toward the on-detector electronics. The recovered clock is distributed by the DaughterBoard and used by the on-detector electronics for detector synchronization and ADC sampling. The main firmware blocks used in the Demonstrator data acquisition system are summarized in Fig. 8.

During the initial Run 3 operation, the detector uplinks used Cyclic Redundancy Check (CRC) to protect the transmitted data to the off-detector electronics. Starting in 2024–2025, together with the migration toward the CPM, the final Phase-II data formats were progressively introduced for the communication between the on-detector and off-detector electronics. The firmware for both DaughterBoard and CPM evolved from CRC-based protection toward the final uplink implementation based on Forward Error Correction (FEC), allowing both error detection and error recovery while adopting the bandwidth allocation and framing foreseen for Phase-II.

Although PMT signals are digitized with full 12-bit precision, detector samples are reduced to 10-bit precision before transmission to the legacy ROD in order to preserve compatibility with the ATLAS TDAQ data formats.

For standard physics and calibration operation, low-gain samples are truncated by discarding the two least significant bits. A dedicated truncation scheme is applied to high-gain samples to preserve compatibility with the effective gain ratio (1:64) of the current on-detector electronics while minimizing degradation of energy reconstruction performance. In this case, the least significant bit and the most significant bit of the original 12-bit sample are removed.

Depending on the operation mode, either one or both gains are transmitted to the legacy ROD. When single-gain samples are transmitted, gain selection is performed automatically in the readout FPGA implemented in the CPM. The high-gain channel is used whenever the detector signal remains within the effective dynamic range of the legacy readout, while the system automatically switches to the low-gain channel for larger signals.

Pedestal runs are the only operating mode where the least significant bits are preserved. This allows detailed noise characterization and direct comparison between legacy and upgraded detector operation.

This hybrid architecture allowed the upgraded digital readout to operate simultaneously with the analog trigger path and the legacy event-building system.

A. *Software integration and detector operation*

The software and operational infrastructure evolved together with the detector electronics and progressively transitioned from a Demonstrator-oriented environment toward the strategies foreseen for final Phase-II detector operation. The Demonstrator was integrated into the ATLAS TDAQ and DCS software frameworks through dedicated applications developed in C++ and Python responsible for detector control, configuration, monitoring and calibration.

These applications controlled the off-detector electronics according to the global detector states defined by ATLAS run control and implemented the detector configuration procedures

required by the upgraded electronics. In addition to standard timing and trigger commands distributed through the TTC system, dedicated configuration commands specific to the Phase-II detector electronics were implemented and transmitted through the detector downlinks. The operational software stack included detector configuration, front-end control, detector initialization, calibration execution and continuous detector monitoring.

Dedicated applications were developed to initialize detector links, supervise data quality, control calibration execution and read out slow integrator information. Continuous supervision of both on-detector and off-detector electronics was implemented with particular emphasis on high-speed link integrity, detector synchronization and firmware consistency across the detector electronics chain.

During Run 3, mechanisms were progressively introduced to supervise detector states, firmware versions and recovery procedures under abnormal detector conditions. Monitoring applications continuously generated warning and error conditions and integrated automated notification mechanisms through the TDAQ and DCS infrastructures, including email and SMS notifications, to allow rapid intervention by detector experts and reduce detector downtime.

To simplify detector maintenance and increase operational robustness of the on-detector electronics, a remote firmware programming strategy was introduced for the DaughterBoard FPGAs based on Golden and Operational firmware images [17]. The Golden image contains a minimal firmware implementation composed only of the optical communication links together with a Flash memory controller enabling remote firmware programming through the optical fibers. The Golden image partition is protected and cannot be overwritten, while the Operational images implement the complete detector functionality and can be remotely updated while preserving a safe recovery mechanism after unsuccessful updates.

The experience accumulated during Demonstrator operation therefore contributed not only to validating the upgraded detector electronics but also to establishing the operational procedures, firmware deployment model and software infrastructure required for final HL-LHC detector operation.

VI. Run 3 Performance

The Run 3 performance of the Demonstrator was evaluated using dedicated calibration campaigns together with detector data collected during standard ATLAS operation.

TileCal employs three complementary calibration systems to monitor different elements of the detector response and separate the contributions of the on-detector electronics, the PMTs, and the detector optics to the overall detector response. For the Demonstrator, these systems were essential to establish direct comparison with neighboring legacy modules and evaluate long-term detector behavior. These calibration systems are the Charge Injection System (CIS), the Laser system, and the Cesium system.

The performance results obtained from Charge Injection, Laser, Cesium, minimum-bias integrator measurements and timing studies demonstrate stable operation of the upgraded electronics under real detector conditions. Rather than evaluating isolated detector components, these complementary calibration and monitoring systems provide a combined assessment of the stability of the complete detector response chain.

Charge Injection measurements demonstrate stable electronics calibration and linearity over time [4]. Laser measurements provide continuous monitoring of PMT gain variations and optical response stability, while Cesium scans validate the long-term stability and equalization of the calorimeter response at detector level.

Minimum-bias integrator measurements extend this validation to collision conditions and provide direct monitoring of the detector response evolution during operation. Fig. 9 shows the comparison of the average detector response variation measured during 2024. The Demonstrator shows a consistently smaller response degradation compared to the neighboring legacy modules across all detector layers. The largest difference is observed in the innermost layer, where the average response variation reaches approximately -2% in the Demonstrator compared with about -7% in the neighboring legacy module. This behavior is attributed primarily to improved PMT stability in the upgraded detector chain, while the remaining response evolution is dominated by scintillator aging effects.

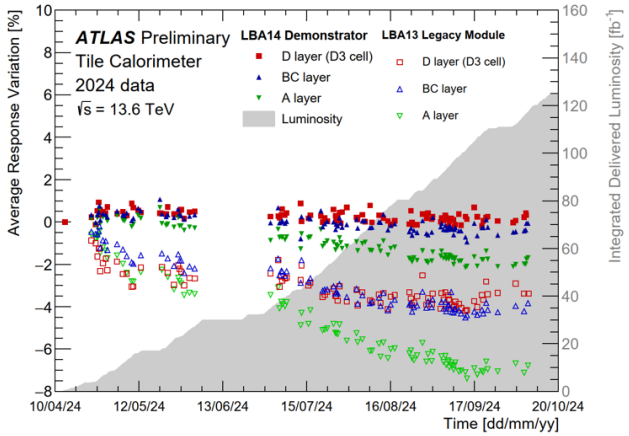


Fig. 9: Average relative response variation measured in individual TileCal layers in the Demonstrator and a neighboring legacy module as a function of time in 2024 [4].

Time calibration and long-term timing stability are important both to preserve the accuracy of the energy reconstruction and to enable precise time-of-flight measurements in dedicated physics analyses. The off-detector electronics distribute the detector clock through deterministic optical links and the recovered clock is used for ADC sampling and synchronization. Therefore, any instability in this chain can directly affect the energy reconstruction and timing.

Fig. 10 shows results of timing stability and resolution studies performed through Laser events acquired during empty bunch crossings with 2025 Run 3 data. The Demonstrator exhibits stable timing performance, with only a limited number of timing excursions at the level of approximately 1 ns observed since 2023. In comparison, a significantly larger

number of timing shifts were observed in individual legacy digitizers over the same operational period. The time resolution measured using laser events is comparable to, and in some regions slightly better than, the average performance obtained in neighboring legacy modules. These results validate the deterministic clock distribution and synchronization strategies implemented in the upgraded electronics.

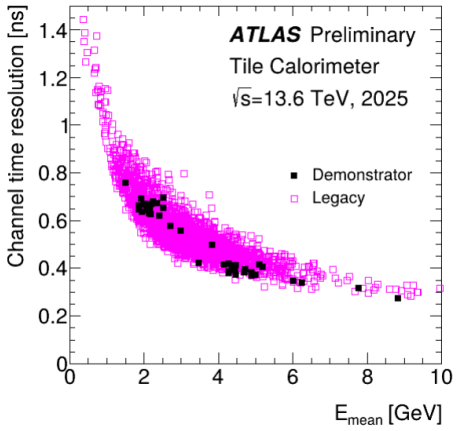


Fig. 10: Time resolution measured with 2025 laser data obtained during empty bunch crossings across all the modules of the Long Barrel A partition [4].

VII. Conclusions

The ATLAS Tile Calorimeter Phase-II Upgrade Demonstrator has operated successfully inside ATLAS during Run 3 as a hybrid detector module combining upgraded electronics with backward-compatible trigger and readout interfaces.

The Demonstrator provided a staged deployment strategy to validate the final Phase-II architecture under realistic detector conditions while preserving compatibility with standard detector operation.

During Run 3, the upgraded readout chain progressively evolved from an initial implementation based on the Tile PreProcessor Demonstrator toward the final CPM, Carrier and FELIX-based architecture. In parallel, the on-detector electronics evolved toward the final detector implementation through the introduction of updated DaughterBoard versions, final communication formats and operational concepts representative of the HL-LHC system.

The Demonstrator validated the complete detector readout chain, including upgraded PMT blocks, front-end signal processing, on-detector digitization, deterministic optical communication, clock and trigger distribution, pipeline buffering and off-detector processing.

Calibration and monitoring results obtained from Charge Injection, Laser, Cesium, minimum-bias integrator measurements and timing studies demonstrate stable operation of the upgraded detector electronics throughout Run 3.

The combined calibration measurements confirm compatibility with the established detector calibration strategy and indicate detector response stability comparable to legacy detector modules. In particular, minimum-bias integrator measurements show reduced response variation during collision operation, consistent with improved long-term stability of the upgraded detector chain.

Operational experience demonstrated that detector reliability does not depend only on hardware performance but also on firmware robustness, detector monitoring and recovery procedures. The integration of automated supervision mechanisms, firmware version control, remote programming capabilities and protected Golden firmware images established operational concepts directly applicable to final detector operation.

The Demonstrator therefore qualified not only the new detector electronics but also the associated operational procedures, firmware deployment model and software infrastructure required for HL-LHC operation.

Overall, the Demonstrator program significantly reduced the integration risk associated with the final TileCal Phase-II deployment and established the technical and operational foundations required for detector operation between 2030 and the end of the HL-LHC physics program.

References

[1] ATLAS Collaboration. The ATLAS Experiment at the CERN Large Hadron Collider. *Journal of Instrumentation*, 3:S08003, 2008. DOI: 10.1088/1748-0221/3/08/S08003.

[2] ATLAS Collaboration. Readiness of the ATLAS Tile Calorimeter for LHC collisions. *Eur. Phys. J.*, C70:1193–1236, 2010. DOI: 10.1140/epjc/s10052-010-1508-y.

[3] ATLAS Collaboration. Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter. Technical Report ATLAS-TDR-028, CERN, 2017.

[4] ATLAS Tile Collaboration. Approved Tile Calorimeter Plots. https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTile. Jun. 2026.

[5] D. Calvet. Upgrade of ATLAS Hadronic Tile Calorimeter for the High-Luminosity LHC. *Nucl. Instrum. Methods Phys. Res., A*, volume 1066, number 169614, 2024. DOI: 10.1016/j.nima.2024.169614.

[6] F. Tang, H. Akerstedt, K. Anderson et al. Design of Main Board for ATLAS TileCal Demonstrator. In *2014 19th IEEE-NPSS Real Time Conference*, pages 1–3, 2014. DOI: 10.1109/RTC.2014.7097541.

[7] E. Valdes Santurio, S. Silverstein, C. Bohm et al. A Revised Version of the ATLAS Tile Calorimeter Link Daughterboard for the HL-LHC. *IEEE Transactions on Nuclear Science*, 68(9):2414–2420, 2021. DOI: 10.1109/TNS.2021.3103408.

[8] F. Carrió and A. Valero. The PreProcessor module for the ATLAS Tile Calorimeter at the HL-LHC. *Nucl. Instrum. Methods Phys. Res., A*, 958:162487, 2020. DOI: 10.1016/j.nima.2019.162487.

[9] J. Anderson, A. Borga, H. Boterenbrood et al. FELIX: a High-Throughput Network Approach for Interfacing to Front End Electronics for ATLAS Upgrades. *J. Phys. Conf. Ser.*, 664(8):082050, 2015. DOI: 10.1088/1742-6596/664/8/082050.

[10] ATLAS Collaboration. Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System. Technical Report CERN-LHCC-2017-020. ATLAS-TDR-029, CERN, 2017.

[11] ATLAS Tile Collaboration. Public Material. https://atlas-tilesc-presenter.docs.cern.ch/material/. Jun. 2026.

[12] P. Leitao, S. Feger, D. Porret et al. Test bench development for the radiation hard GBTX ASIC. *Journal of Instrumentation*, 10(01):C01038–C01038, Jan. 2015. DOI: 10.1088/1748-0221/10/01/c01038.

[13] M. Barros Marin, S. Baron, S. S. Feger et al. The GBT-FPGA core: features and challenges. *Journal of Instrumentation*, 10(03):C03021–C03021, Mar. 2015. DOI: 10.1088/1748-0221/10/03/c03021.

[14] PICMG. *AdvancedTCA Short Form Specification*, Jan. 2003.

[15] F. Carrió. The Data Acquisition System for the ATLAS Phase-II Tile Calorimeter Demonstrator. *EPJ Web Conf.*, 253:01002, 2021. DOI: 10.1051/epjconf/202125301002.

[16] S. Baron, J. P. Cachemiche, F. Marin et al. Implementing the GBT Data Transmission Protocol in FPGAs. *Proceedings of TWEPP-09*, Sep. 2009. DOI: 10.5170/CERN-2009-006.631.

[17] Advanced Micro Devices, Inc. *UltraScale Architecture Configuration User Guide (UG570)*, v1.20.1 edition, March 2025.