Design and Results of a Radiation Test System for SEE and TID Assessment of the VLAST-P Calorimeter Electronics

— Evaluation of AD9266 and THS4524 —

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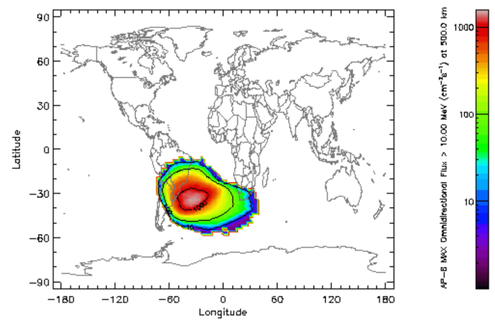
Introduction

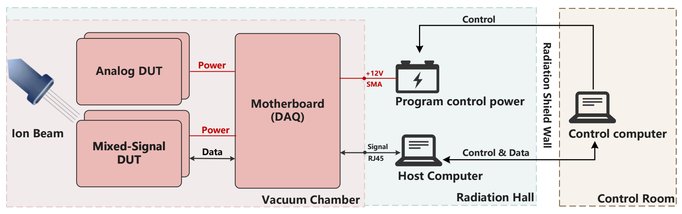
- The VLAST-P is a space detector designed to observe solar high-energy gamma rays and protons, operating in a low-Earth, Sun-synchronous orbit at ∼500 km altitude where it periodically encounters the South Atlantic Anomaly (SAA).
- Space radiation triggers single-event effects (SEE) and total ionizing dose (TID) risk: individual heavy ions cause transient logic upsets (SEU) or high-current locking states (SEL), while cumulative dose leads to progressive parametric and noise degradation.
- Ground-based heavy-ion irradiation tests are the standard methodology for validating electronics against these radiation risks. However, conventional test setups often lack scalability and adequate tools to characterize active event recovery, especially for SEL.
- To address this, an FPGA-based heavy-ion irradiation test system was developed. It adopts a radiation-decoupled modular architecture, enabling real-time SEE detection and quantitative evaluation of TID-induced performance degradation.



Electronics Design

Overall Design

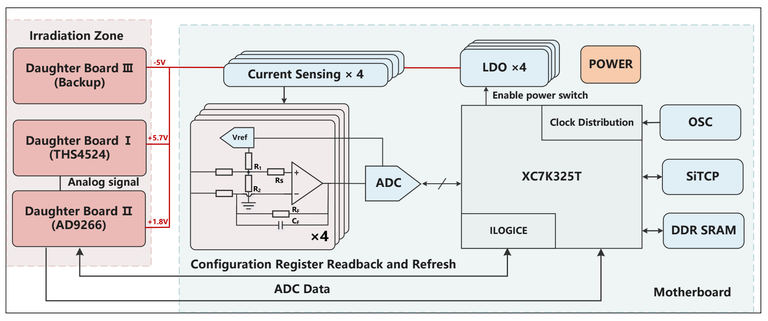
The system utilizes a **radiation-decoupled architecture** to ensure DAQ stability. The motherboard interfaces with DUT daughter boards via high-density cables with voltage-drop compensation, while the SiTCP protocol ensures robust data transmission.



Hardware Design

The hardware architecture is engineered for real-time SEL mitigation:

- **High-Fidelity Detection:** Shunt resistors, level shifters (aligning signals with the ADC linear range for enhanced precision), AD8032 amplifiers (gain of 20), and 12-bit TLV2548 ADCs accurately resolve microsecond-level transient current spikes.
- **Rapid Isolation:** FPGA-enabled LDOs and 20 Ω series resistors provide hardware redundancy, executing microsecond-level power shutdown to protect remote DUTs.



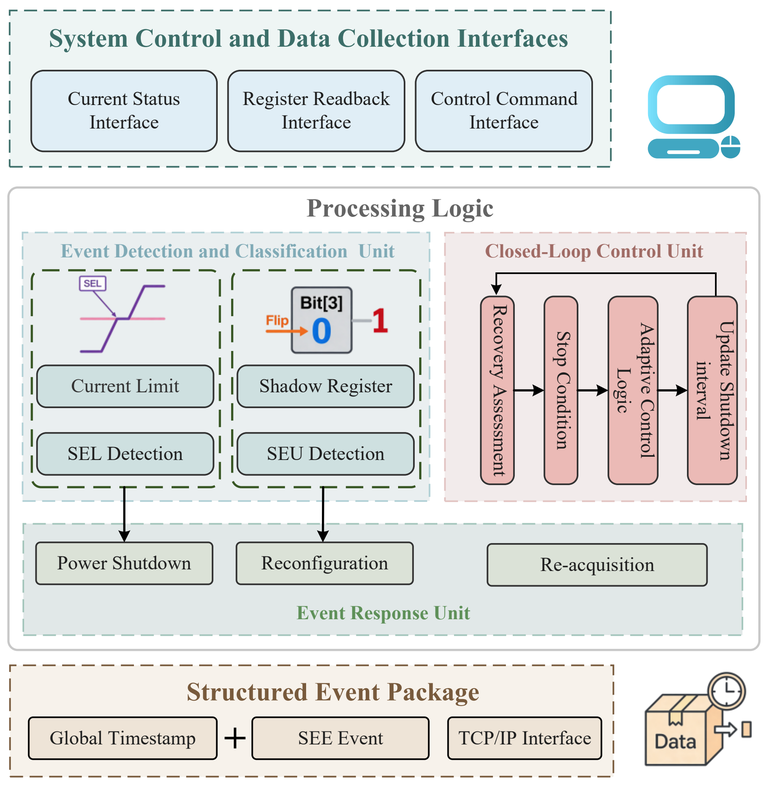
For SEU management, digital FPC interfaces enable continuous configuration register readback and state refresh. Separately, high-precision analog interfaces (SMA/LEMO) are integrated for comparative TID performance evaluation.

Logical Design

The FPGA-based logic implements a dual-layer self-recovery strategy:

- **SEL Mitigation:** Fast power-off sequence (50 μs) triggered upon over-current detection.
- **SEU Correction:** Real-time monitor captures register upsets and triggers immediate register refresh to restore state machine integrity without power cycling.
- **Closed-Loop Control:** Iterative adjustment of shutdown intervals based on real-time recovery success metrics.

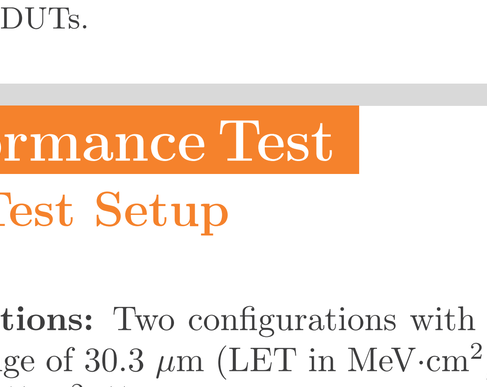
Coupled with global timestamps for nanosecond-level event correlation, this logic quantifies critical recovery times, while utilizing DDR3 memory to buffer continuous telemetry data for reliable SiTCP transmission to the host computer.



Performance Test

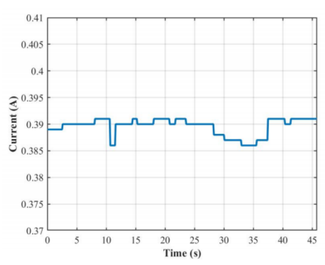
SEE Test Setup

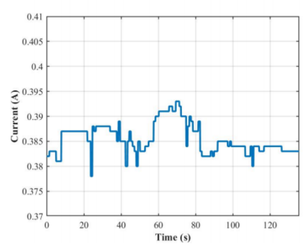
- **Conditions:** Two configurations with the same ion range of 30.3 μm (LET in MeV·cm^2/mg, flux in ions/(cm^2·s)):
  (1) **LET 15:** Cl ions (109 MeV), flux $\sim 4.54 \times 10^4$, fluence 1.70×10^6 ions/cm^2;
  (2) **LET 37:** Ge ions (205 MeV), flux $\sim 5.74 \times 10^4$, fluence 1×10^7 ions/cm^2.
- **Placement:** DUTs inside a vacuum chamber; DAQ motherboard safely shielded outside.



SEE Test Result

- **SEL Immunity:** No SEL occurred in either AD9266 or THS4524 under $LET = 15$ and 37 MeV · cm^2/mg with stable currents.
- **Current Monitored:** Operating currents under $LET = 37$ for AD9266 (left) and THS4524 (right) are shown below.





- **SEU Recovery:** A total of 45 SEUs were detected in the AD9266 under an LET of 37 MeV·cm^2/mg and successfully resolved via automatic register reconfiguration without manual intervention.

TID Test & Results

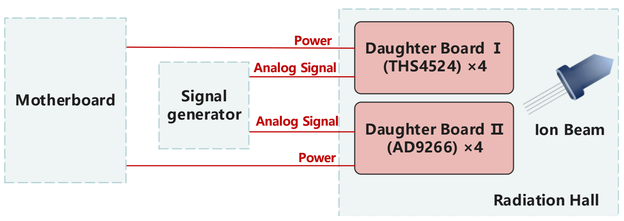
Conducted using a ^{60}Co facility, involving an initial 10 krad dose, an intermediate annealing process, and a subsequent 30 krad over-irradiation (dose rate: 5 krad/h, non-uniformity $< 10\%$).

THS4524

Parameter	Pre-rad	Post-rad	Over-rad
I_{CC}	4.17 mA	5.83 mA	4.5 mA
Noise Level	75.6 mV	94.7 mV	94.4 mV

AD9266

Parameter	Pre-rad	Post-rad	Over-rad
I_{CC}	52.62 mA	52.75 mA	50.50 mA
DNL	0.25 LSB	0.27 LSB	0.29 LSB
Timing Func.	Normal	Normal	Normal



Conclusion

- **System Architecture:** Radiation-decoupled DAQ with FPGA-based dual-layer self-recovery, ensuring safe and real-time DUT evaluation.
- **SEE Resilience:** Tested up to LET 37 MeV · cm^2/mg. Achieved zero SEL and autonomously resolved 45 SEUs without manual intervention.
- **TID Tolerance:** No functional failure was observed, while some parameters showed limited degradation and partial recovery after annealing/over-irradiation.

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