# Timing and Slow Control Backend for CMS Drift Tube On-Board Electronics

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***Abstract*—Commissioning of the detectors for the High-Luminosity Large Hadron Collider (HL-LHC), also referred to as the Phase-2 upgrade, is planned for the period 2026–2028 at CERN. In this framework, the readout and control electronics of the Drift Tube (DT) subdetector of the Compact Muon Solenoid (CMS) experiment have undergone a complete redesign. This upgrade is being carried out to cope with the expected increase in event rates and to ensure compatibility with the upcoming Trigger and Timing Control Distribution System (TCDS2). In parallel with this, a new back-end system for timing distribution and slow control has been developed. This system is based on a set of field-programmable gate array (FPGA)-based Advanced Telecommunications Computing Architecture (ATCA) boards onto which custom firmware has been deployed. Each board is connected to the server through a network interface and provides approximately one hundred high-speed optical links implementing the Low Power Gigabit Transceiver (LpGBT) protocol, used to distribute machine-synchronous timing signals and slow-control commands to the detector electronics. The VHSIC Hardware Description Language (VHDL) firmware integrates intellectual property (IP) cores, makes use of the SLAC Ultimate RTL (register-transfer level) Framework (SURF), and incorporates dedicated modules specifically designed to interface and manage custom on-detector electronics. In addition, a Python software library has been developed to configure, monitor, and control the boards through a dedicated Reliable User Datagram Protocol (RUDP) connection between the boards and the server. This contribution will describe the overall design of the system, detail the implementation at the firmware level, and present the results of the benchtop and field tests performed to date.**

***Index Terms*—CMS, Drift Tubes, HL-LHC, TCDS2, LpGBT, ATCA, Serenity, timing distribution, slow control, FPGA.**

## I. Introduction

The Phase-2 upgrade of the High-Luminosity Large Hadron Collider (HL-LHC) will expose the experiments at CERN to higher luminosity and increased event rates. These conditions impose more demanding requirements on the trigger, timing, and readout systems of the CMS [1] detector. In the muon system, the Drift Tube (DT) [2] electronics are being upgraded [3] to sustain the expected operating conditions and to interface with the new Trigger and Timing Control Distribution System, TCDS2 [4]. The DT detector provides precision muon measurements in the barrel region of CMS. The upgraded on-detector electronics are based on On-Board Drift Tube (OBDT) front-end boards, which perform time-to-digital conversion of the drift tube signals and transmit data

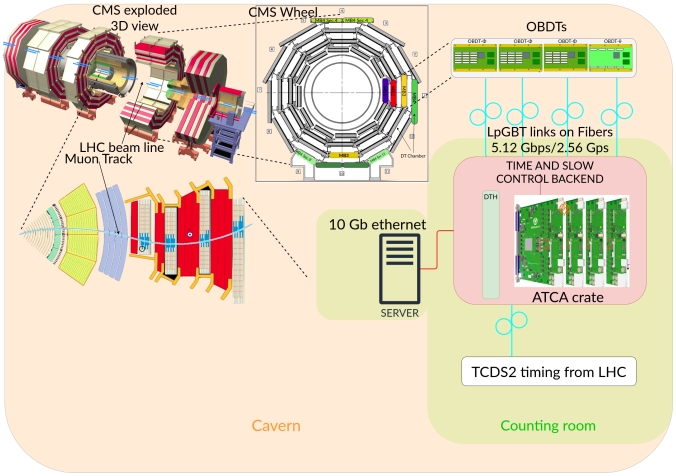


Fig. 1. Top-Left: three-dimensional view of the CMS Detector; Top-Center: a sectional representation of the wheel; Middle-Left: detail of the Drift Tube sub-detector detecting a muon track; Top-Right: arrangement of the OBDT boards; Bottom-Right: backend system installed in the counting room

to the back-end system through optical links [5], [6]. Each OBDT board integrates an LpGBT chip [7], which provides the optical-link interface and handles the reception of the machine-synchronous clock and timing/control information, and a Slow Control Adapter (SCA) chip [8], which provides monitoring, slow-control functions, and support for remote FPGA reconfiguration. In this context, a dedicated timing and slow-control backend has been developed. Its role is to distribute the LHC machine timing to the OBDT boards, provide deterministic synchronization, configure and monitor the front-end electronics, and support remote FPGA reconfiguration.

The design is intended for implementation on Serenity ATCA boards and has been validated so far on a provisional system based on commercial boards (HTG-940 platform) sharing the same FPGA family as the final hardware.

## II. System Architecture

The backend system is implemented using ten Serenity ATCA boards [9]. Each board provides timing and slow-control functionalities to approximately 90 OBDT front-end boards. Overall, the system distributes timing and control

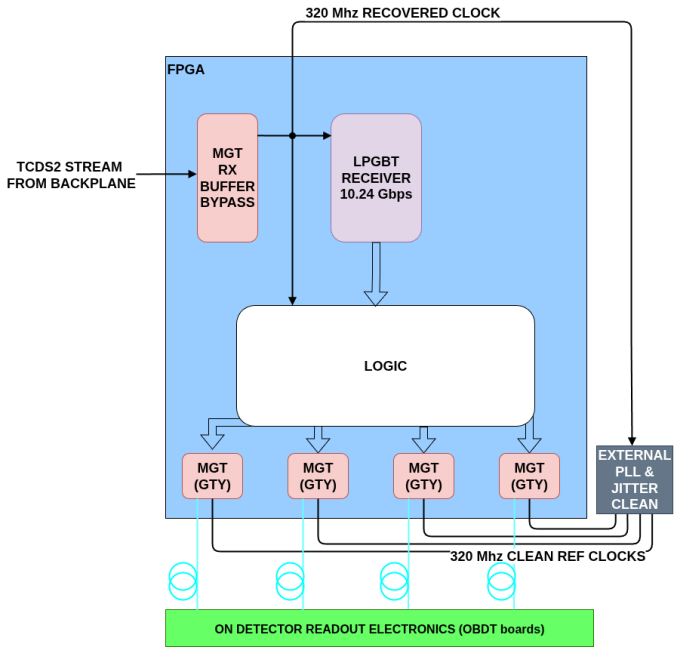


Fig. 2. Clock and synchronization distribution scheme inside the backend board

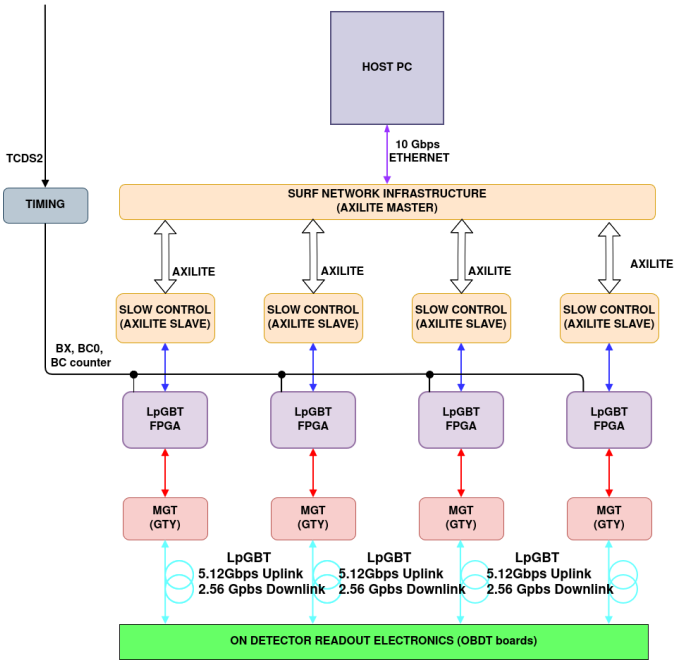


Fig. 3. Overview of backend channels and interfaces between timing, slow control, and firmware blocks.

signals to about 1000 OBDT boards in the CMS DT system. Fig. 1 illustrates the location of the backend with respect to the structural layout of the CMS detector.

The timing distribution originates from the Large Hadron Collider (LHC) machine timing system, which is transmitted via the TCDS2 protocol to the DAQ and Timing Hub (DTH) board, located in the same crate. The DTH board then provides the timing information to the Serenity boards through the crate backplane. The Serenity boards, in turn, distribute the 40.079 MHz bunch-crossing clock and the associated synchronization signals, including bunch-crossing-zero (BC0) markers, to the OBDT boards over point-to-point optical links.

Each optical link implements an optical interface based on the LpGBT protocol [10]. The downlink (backend to OBDT) runs at 2.56 Gbps and carries clock, control, and synchronization information from the backend to the front-end. The uplink (OBDT to backend) runs at 5.12 Gbps and carries monitoring and data information from the OBDT boards.

In addition to the timing distribution functionality, the backend provides slow-control capabilities for each OBDT board. These functionalities include board configuration; readout of supply voltages, currents, and temperatures; programmable threshold adjustment; status monitoring; and remote reconfiguration of the front-end FPGA. The control software is implemented in Python and is built upon the Rogue library [11], which employs a reliable User Datagram Protocol (UDP)–based transport layer to access firmware registers and data streams.

## III. Timing Requirements

The DT detector achieves a spatial resolution of approximately 200–250 $\mu$m in the $\phi$ coordinate and an intrinsic time resolution of approximately 2 ns [12]. To preserve this performance, the backend timing system must distribute a stable reference clock and synchronization information to the front-end boards.

The precision required for the absolute timing reference on the OBDT boards is on the order of 100 ps. This value is significantly smaller than both the intrinsic detector time resolution and the time-to-digital converter (TDC) quantization step of 779 ps, ensuring that the clock distribution contributes only negligibly to the overall timing uncertainty. Adopting a 100 ps target therefore provides comfortable margin while remaining achievable with commercially available timing components and clock-distribution techniques. For this reason, the firmware architecture minimizes variable latency sources and uses deterministic transceiver configurations (transmit buffer bypass) [13].

## IV. On Board Clock Scheme

The internal clock distribution of the board derives its reference from the TCDS2 stream received through the backplane, as summarized in Fig. 2. The clock is recovered by the clock and data recovery (CDR) circuitry of the multi-gigabit transceiver (MGT) receiver. The recovered clock is used to drive the FPGA fabric and is also routed to an external phase-locked loop (PLL) that acts as a jitter cleaner. The outputs of the jitter cleaner are then used as reference clocks for the MGTs connected to the OBDT boards.

## V. Firmware Design

The FPGA on the Serenity board is connected to an external host PC via a standard 10 Gbps Ethernet interface. The

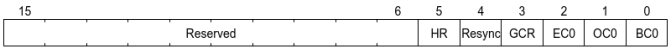


Fig. 4. Waveform diagram used in the firmware design.

TABLE I
TCDS2 TIMING FRAME FIELDS USED BY THE BACKEND FIRMWARE (SEE FIG. 4).

| Field | Meaning |
|---|---|
| BX[1] | Bunch-crossing identifier within the current orbit. |
| BC0 | Bunch-crossing-zero marker (asserted at $\mathrm{BX} = 0$). |
| OC0 | Orbit-counter reset / orbit-alignment marker. |
| EC0 | Event-counter reset / orbit-alignment marker. |
| GCR | Global counter reset |
| Resync | flush pipelines |
| Reserved | Unused bits; carried through for compatibility / future use. |

[1] BX does not have its own dedicated bit field, because the strobe signal in each valid frame already indicates when the bunch crossing is asserted.

firmware follows a CPU-less Ethernet architecture: reliable UDP (RUDP) packets are mapped to the Advanced eXtensible Interface (AXI) AXI-Lite and AXI-Stream busses, allowing an external control PC to access registers and data without embedding a processor in the FPGA. This approach simplifies firmware partitioning and scales over standard Ethernet infrastructure.

Deterministic timing is guaranteed by running the LpGBT interface entirely in a single 320.632 MHz clock domain—exactly eight times the 40.079 MHz LHC clock—and by driving the multigigabit transceivers in buffer-bypass mode. This architecture ensures fixed latency through resets and reconfiguration. Robust backend implementations of the LpGBT and Slow Control Adapter (SCA) control interfaces provide seamless, deterministic links to the corresponding LpGBT and SCA chips located on the OBDT front-end electronics.

The design is based on the SURF framework [14], using blocks for registers access and Ethernet communication. Custom logic implements timing distribution, optical-link management, slow control, and diagnostics required for DT operation.

## VI. TIMING DISTRIBUTION

In Fig. 3, the timing block is depicted as the segment of the firmware responsible for the distribution of timing information synchronously with the 320.632 MHz master clock. The TCDS2 fields used by the backend firmware are summarized in Table I. The information of the bunch crossing (BX) and the bunch crossing reset (BC0) (Fig. 5), extracted from each TCDS2 stream frame (see Fig. 4), is propagated to the downstream LpGBT FPGA blocks, which subsequently drive the multigigabit transceivers (MGTs) interfaced with the OBDTs. The event counter reset (EC0) and orbit counter reset (OC0) and others (GCR, Resync) signals are decoded by the backend firmware but are not distributed to the OBDTs, as they are not required by the front-end electronics.

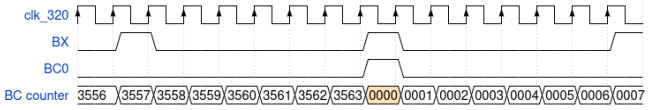


Fig. 5. Waveform diagram used in the firmware design.

## VII. PROTOTYPE HARDWARE

The final target platform is the Serenity S1 ATCA board, which provides the required optical connectivity and FPGA resources for the backend system [9]. Since Serenity hardware became available only recently as a single prototype, laboratory and development tests were initially performed with an HTG-940 evaluation platform [15], shown in Fig. 6.

The HTG-940 platform uses a Xilinx Virtex UltraScale+ FPGA, the same FPGA family as the Serenity board, and supports optical mezzanine cards. This makes it suitable for firmware development, optical-link validation, and early integration tests while preserving good architectural compatibility with the final backend.

## VIII. PRELIMINARY MEASUREMENTS

### A. Signal Integrity

Preliminary signal-integrity measurements were performed on the optical links, and a summary of the results is reported in Table II. The 2.56 Gbps downlink, evaluated using the link-monitoring circuitry implemented in the OBDT LpGBT chip showed an eye opening of approximately 80%. The 5.12 Gbps uplink, evaluated using the receiver diagnostics of the backend FPGA multigigabit transceivers and the Integrated Bit Error Ratio Test (IBERT) core, showed an eye opening of approximately 76%. During the test interval, no errors were observed up to a measured bit-error-rate limit of $10^{-6}$. Although this BER limit is less stringent than the values typically reported in dedicated link-qualification studies, it was intentionally chosen to allow rapid and continuous monitoring of link quality during system development and integration.

### B. Timing Performance

A synchronous event was distributed to three OBDT channels connected to the backend system and observed with an oscilloscope. The measurement used a horizontal time scale of 100 ps/div. The measured RMS channel-to-channel jitter was 5.95 ps. The observed channel-to-channel skew ranged from 200 ps to 420 ps.

TABLE II
PRELIMINARY TIMING AND SIGNAL-INTEGRITY MEASUREMENTS.

| Quantity | Value | Comment |
|---|---|---|
| Downlink rate | 2.56 Gbps | LpGBT downlink |
| Uplink rate | 5.12 Gbps | LpGBT uplink |
| Downlink eye opening | $\sim$80% | LpGBT-generated eye |
| Uplink eye opening | $\sim$76% | IBERT measurement |
| Uplink BER | $< 10^{-6}$ | Test interval result |
| Channel-to-channel jitter RMS | 5.95 ps | Three-channel test |
| Channel-to-channel skew | 200–420 ps | Three-channel test |

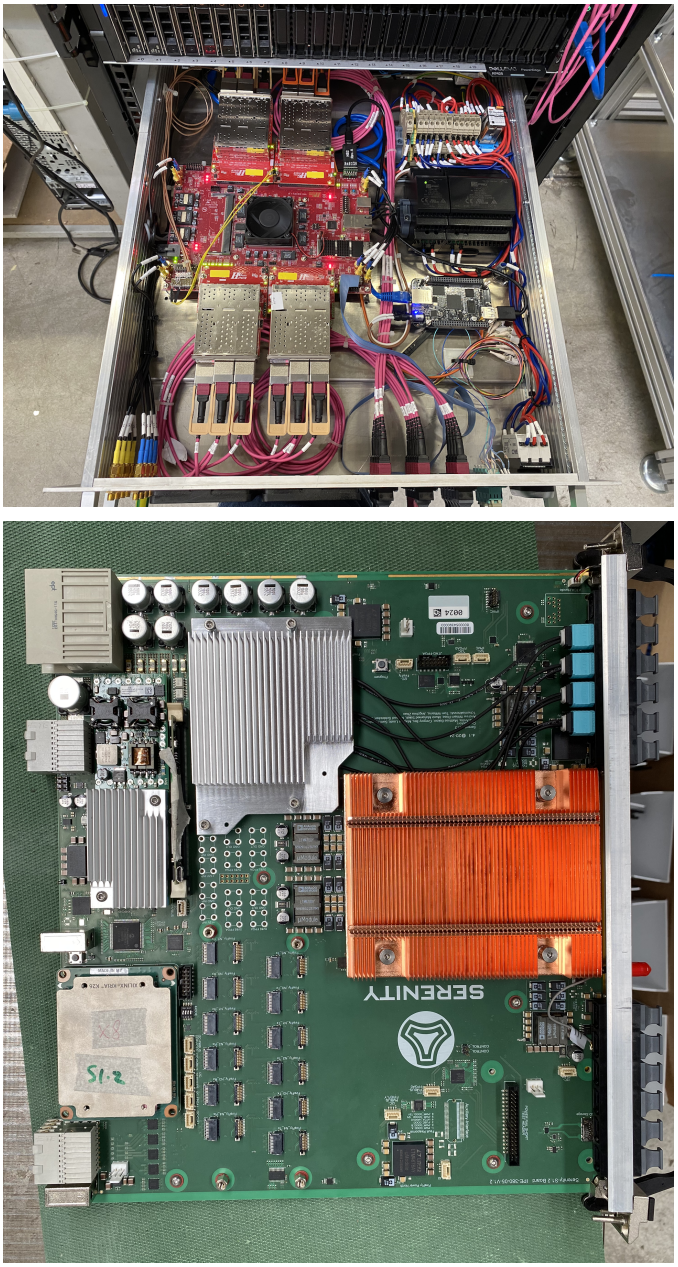


Fig. 6. Top: internal view of the prototype setup. Bottom: Serenity S1 ATCA board used as target hardware for the backend system.

These first measurements confirm the feasibility of the proposed timing distribution and optical-link architecture. Further tests will be required on the final Serenity hardware and in detector-integration conditions.

## IX. Conclusion and Outlook

A timing and slow-control backend for the CMS DT Phase-2 on-board electronics has been developed. The system distributes the LHC bunch-crossing clock and synchronization information from TCDS2 to the OBDT front-end boards and provides configuration, monitoring, and remote FPGA reconfiguration capabilities.

The firmware adopts a CPU-less Ethernet architecture, a deterministic LpGBT timing path, and buffer-bypass transceiver operation. Preliminary tests on an interim HTG-940 platform show good optical-link eye openings and sub-10 ps RMS channel-to-channel jitter in a synchronous timing test.

Future work will focus on continuing tests with the provisional setup, porting the HDL design to the Serenity hardware, and performing detector-integration tests by the end of 2026.

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