Timing and Slow Control backend for CMS Drift Tube On-Board electronics

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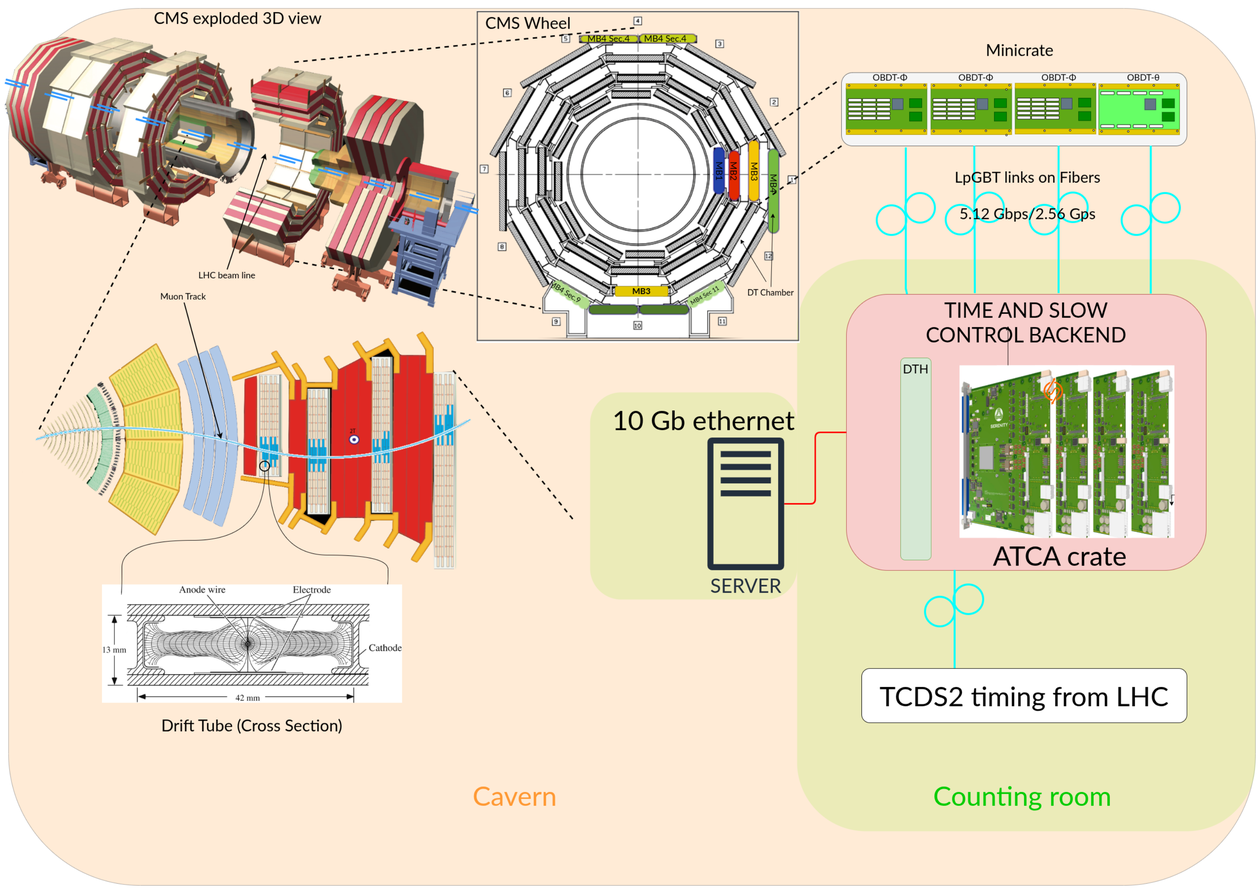
Introduction - System Context



In view of the Phase-2 upgrade of the High-Luminosity Large Hadron Collider (HL-LHC), the experiments at CERN will operate at significantly higher luminosity, leading to increased data rates and stricter timing requirements. To address these challenges, the CMS experiment is upgrading its detector systems and electronics, including a complete redesign of the Drift Tube (DT) muon subdetector electronics [1] to sustain higher trigger rates and interface with the new Trigger and Timing Control Distribution System (TCDS2) [2].

Within this framework, a new backend system for timing distribution and slow control has been developed. It is based on FPGA-equipped ATCA modules interfaced via high-speed optical links (5.12 Gbps uplink, 2.56 Gbps downlink) that implement the LpGBT protocol [3]. The system is implemented using ten Serenity boards [4], each providing timing and slow control to about 90 OBDT (On-Board drift tube) front-end boards, which receive precise 40.079 Mhz bunch crossing timing and synchronization signals (i.e. Bunch crossing zero) from the LHC through the TCDS2 system. These signals are first received by the DAQ and Timing Hub (DTH), which makes them available through the crate backplane to the Serenity boards, and are then distributed to approximately 850 OBDT front-end boards [5].

Beyond timing distribution, the system provides:

- comprehensive slow control functionality: configuration and monitoring of each OBDT board by acquiring key operational parameters, including voltages, currents, temperatures, and programmable thresholds;
- remote FPGA reconfiguration on the front-end boards.

Combined with SURF-based dedicated firmware [6] and Python control software using a reliable UDP protocol (Rogue) [7], the system ensures scalable, reliable, and efficient operation of DT readout electronics.

Timing System Requirements

The primary function of the readout system is to perform time-to-digital conversion of the signals generated by the Drift Tube detector cells. The detector attains a spatial resolution in the range of 200–250 μm in the ϕ direction, with an intrinsic time resolution of approximately 2 ns [8]. To preserve this performance, the readout system must operate with a commensurate temporal precision.

To achieve this level of accuracy, the timing and control system must distribute an absolute time reference to the OBDT front-end boards with precision on the order of 100 ps. Such timing accuracy is crucial to guarantee proper synchronization of the measurements and to fully exploit the intrinsic temporal resolution of the detector.

Firmware block diagram

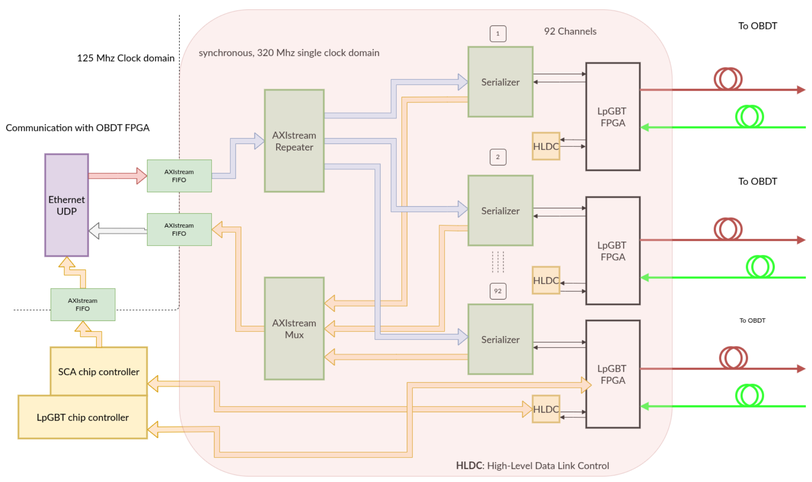


Figure 1. Firmware block diagram

- CPU-less Ethernet architecture with UDP (RUDP) mapped to AXI-Lite/AXI-Stream interfaces;
- LpGBT interface implemented in a single 320 MHz clock domain for deterministic latency;
- Multigigabit transceivers configured in buffer-bypass mode;
- Backend implementations of LpGBT and SCA chips for control.

Signal integrity

CMS Muon preliminary DT Phase-2 Upgrade

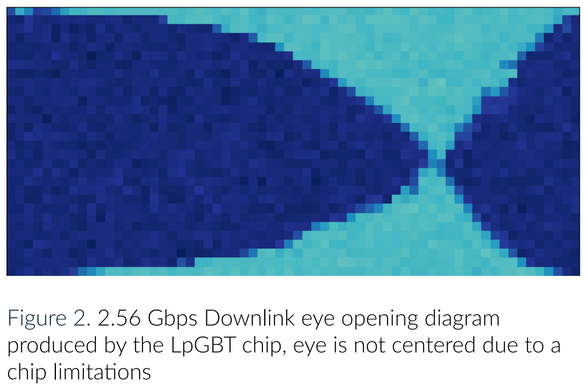


Figure 2. 2.56 Gbps Downlink eye opening diagram produced by the LpGBT chip, eye is not centered due to a chip limitations

CMS Muon preliminary DT Phase-2 Upgrade

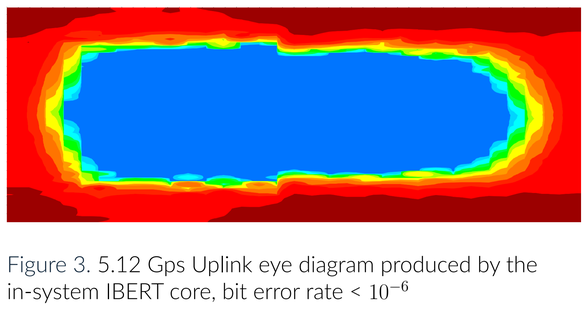


Figure 3. 5.12 Gps Uplink eye diagram produced by the in-system IBERT core, bit error rate < 10^{-6}

The downlink eye opening is approximately 80%, while the uplink eye opening is about 76%.

Hardware pictures

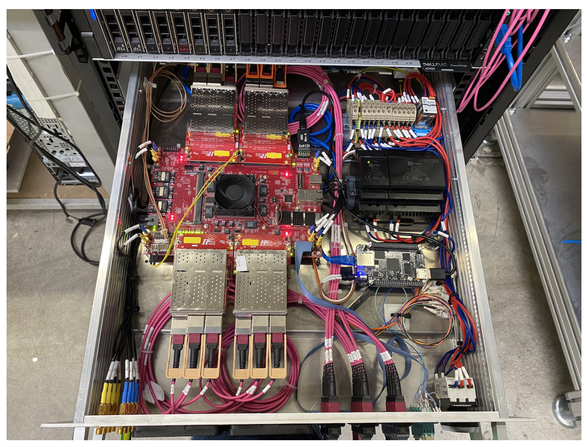


Figure 4. Provisional system based on a HTG 940 board

Since the Serenity board has only recently become available as a single prototype, development, laboratory, and field tests have been carried out using an interim hardware platform (HTG-940) [9]. This platform uses the same FPGA (Virtex Ultrascale+) as the final system and is equipped with optical mezzanine cards, ensuring good architectural compatibility.

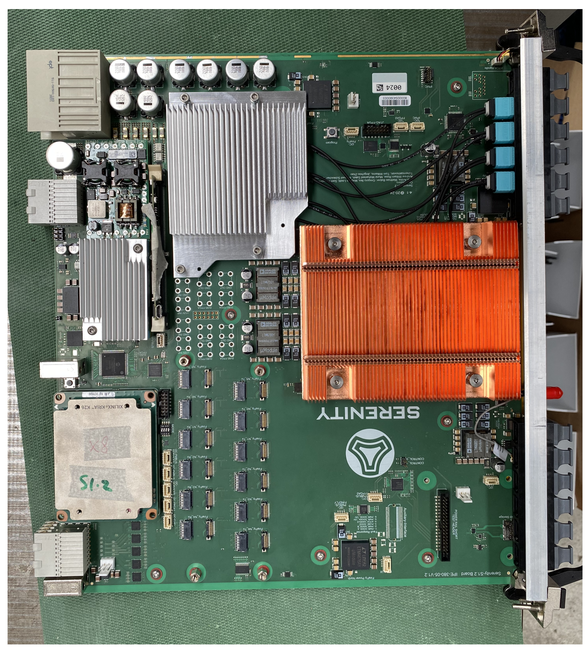


Figure 5. The Serenity board, S1 version

Timing Performance

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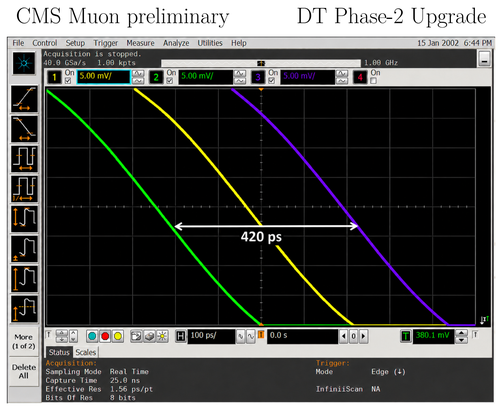

Trace	Channel
	Test Pulse falling edge, channel A
	Test Pulse falling edge, channel B
	Test Pulse falling edge, channel C

Timing Performance	Min [ps]	Max [ps]
Channel-to-channel jitter RMS	5.95	
Channel-to-channel skew	200	420

Figure 6. The oscilloscope screenshot shows signals from a synchronous event acquired on three OBDT channels connected to the backend system. The horizontal time scale is set to 100 ps/div.

Summary and Plans

- Continue test activities with the provisional system, in preparation for the installation of the on-board electronics;
- Port the HDL design to the Serenity hardware;
- Perform detector integration tests by the end of 2026.

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