Data Processing Firmware of the Upstream Tracker for LHCb Run 3

C. Abellan Beteta[1], F. Alessio[2], G. Bassi[3], I. Bezshyiko[1], C. Hadjivasiliou[4], G. Hijano Mendizabal[1], W. Krupa[5], F. Lazzari[3,6], G. Loustau de Linares[1], A. Mathad[1], M. Peco Regales[1], G. Punzi[3], M. Rudolph[5], M. Tobin[2,7], L. Villardita[1], G. Vouters[8]

[1] University of Zurich (CH), [2] CERN, [3] Università di Pisa (IT), [4] University of Maryland (US), [5] Syracuse University (US), [6] INFN Pisa (IT), [7] Institute Of High Energy Physics, Beijing (CN), [8] Centre National de la Recherche Scientifique (FR)

Abstract

LHCb, one of the four main experiments at CERN, was upgraded for Run 3 to enable fully software-based triggering and data acquisition. A key component of this upgrade is the Upstream Tracker (UT), a silicon microstrip detector installed in early 2023. The UT comprises 968 silicon sensors and 4192 SALT ASICs, which perform analog processing, digitization, common-mode subtraction, zero suppression, and data serialization. The resulting data streams are transmitted to the TELL40 back-end readout boards. Each TELL40 board can be viewed, in simplified terms, as a set of optical fibre receivers connected to a high-performance Intel Agilex 10 FPGA, responsible for data processing and transfer to a PCIe interface.

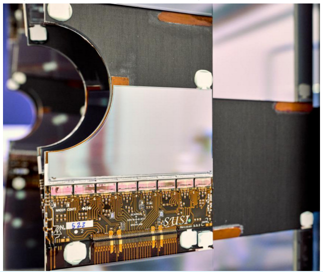
This contribution focuses on the TELL40 FPGA gateware developed for the UT readout. It describes the challenges posed by the UT electronics architecture, data formats, high data rates and zero deadtime. It presents the adopted mitigation strategies, which reduced system complexity at the cost of specific trade-offs. In addition to the core data acquisition functionality, several monitoring and control mechanisms were implemented within the Experiment Control System (ECS) and the Timing and Fast Control (TFC) system. The resulting architecture and the key design decisions are presented.

Finally, the development of a system with custom inputs and outputs required the application of dedicated design verification and debugging techniques, as well as the development of supporting software, which are also described.

The LHCb Upstream Tracker

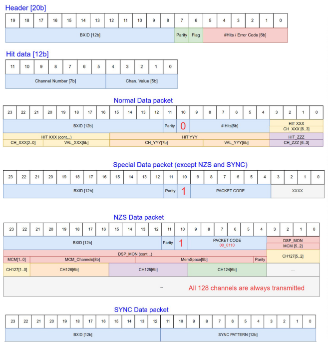
The Upstream Tracker (UT) is a silicon detector placed upstream of the LHCb dipole magnet and is composed of four planes of silicon microstrips. Four different silicon sensor designs are used to handle the varying occupancy over the detector acceptance. Dedicated front-end ASIC, named SALT chip, read out 128 channels at 40MHz. They provide 12b words composed of 7b for the strip and 5b for the read value. This data is serialized in 8b elinks working at 320Mbps. The UT features SALT ASICs with 3, 4 or 5 enabled elinks, depending on the occupancy of the region. This data is collected by GBT ASICs that send it through optical fibers to the counting room where our FPGAs process it.

Packet name	Header (12-bit) BXID 4 bits	Parity 1 bit	Flag 1 bit	Length 6 bit	Data n·12 bits	Comment
Idle	0000	1	1	'b11_0000	—	no enough data
BxVeto	*bxid_cnt[3:0]*	*	1	'b01_0001	—	BxVeto in TFCcmd
HeaderOnly	*bxid_cnt[3:0]*	*	1	'b01_0010	—	HeaderOnly in TFCcmd
BusyEvent	*bxid_cnt[3:0]*	*	1	'b01_0011	—	$nHits > 63$
BufferFull	*bxid_cnt[3:0]*	*	1	'b01_0100	—	no space in memory
BufferFullN	*bxid_cnt[3:0]*	*	1	'b01_0101	—	no space in memory
NZS	*bxid_cnt[3:0]*	*	1	'b00_0110	Values	NZS in TFCcmd
Normal	*bxid_cnt[3:0]*	*	0	*nHits*	Hits	Normal event
Sync	*bxid_cnt[11:0]*				*sync_pattern*	Synch in TFCcmd



GBT frame byte	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4 x 3-eports			24-bit			24-bit			24-bit			24-bit		
2 x 3-eports			24-bit					24-bit						
2 x 4-eports			32-bit					32-bit						
2 x 5-eports			40-bit					40-bit						

Requirements and Challenges



HIGH DATA RATES

- Data must be processed at the full 40 MHz LHC collision rate.
- Peak output bandwidths up to O(100) Gbps per TELL40.

UP TO 48 ASICs PER TELL40

- Each TELL40 board must receive, align and process data from up to 48 SALT ASICs.
- Multiple e-links per ASIC are aggregated through GBT links over optical fibres.

COMPLEX ASIC DATA FORMAT

- 12-bit words with intricate structure: headers, addresses, ADC data, time stamps, etc.
- Variable-length payloads depending on hit multiplicity.
- Error signaling with multiple error types.

NON-ZERO SUPPRESSED (NZS) PACKETS

- NZS packets contain non-zero-suppressed data and are always of a single, very large size.
- Efficient handling of NZS data is essential to control bandwidth and avoid buffer collapse.

ALIGNMENT TO 16-BIT WORDS

- ASIC data are in 12-bit words and must be aligned to 16-bit words for the internal processing and output interfaces.
- Alignment must be done efficiently while minimizing padding overhead and preserving data integrity.

BANDWIDTH & RESOURCE CONSTRAINTS

- Design must fit within FPGA resource limits (ALMs, DSPs, memory).
- Minimize zero-padding and buffering to stay within feasible output bandwidth.

ROBUSTNESS & ERROR HANDLING

- Must tolerate corrupted frames, link errors, misalignment and synchronization losses.
- Common error handling and auto-recovery mechanisms required.

VERIFICATION & DEBUGGING COMPLEXITY

- Custom protocols and high-speed interfaces demand extensive simulation, emulation and hardware-level validation.
- Need to inject nominal and faulty data, including NZS and error scenarios.

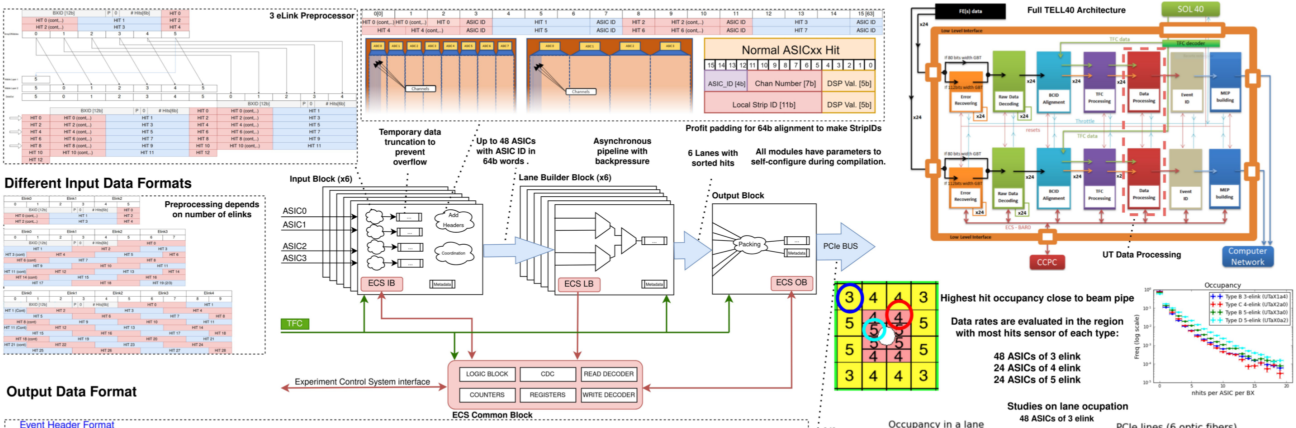
Final architecture

PreProcessors depend on the number of elinks.

IB Output format is common, so the rest of the system is common to all cases.

3, 4, 5 eLinks

3 Input formats



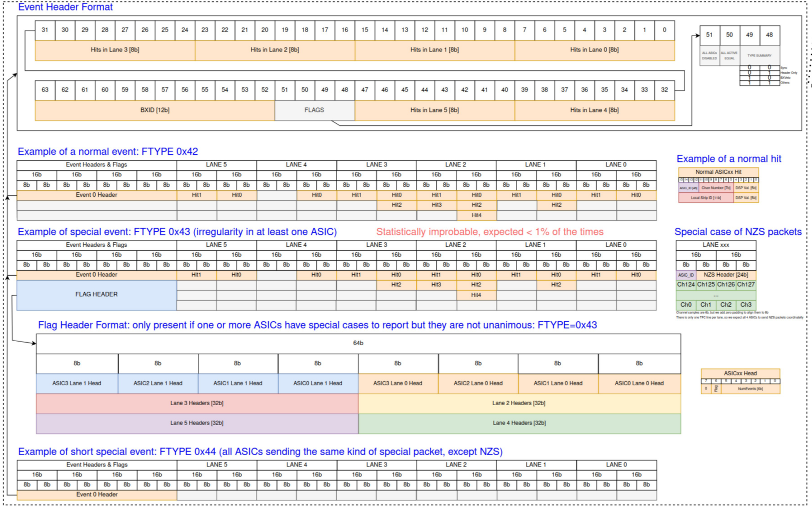
Output Data Format

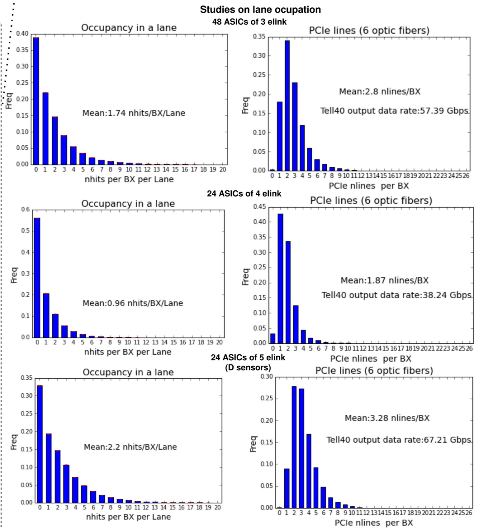
Data format trades efficiency for ease of implementation.

Ease of implementation reduces FPGA resource usage.

Some bandwidth is lost in the process, but it is far from being the limiting factor.

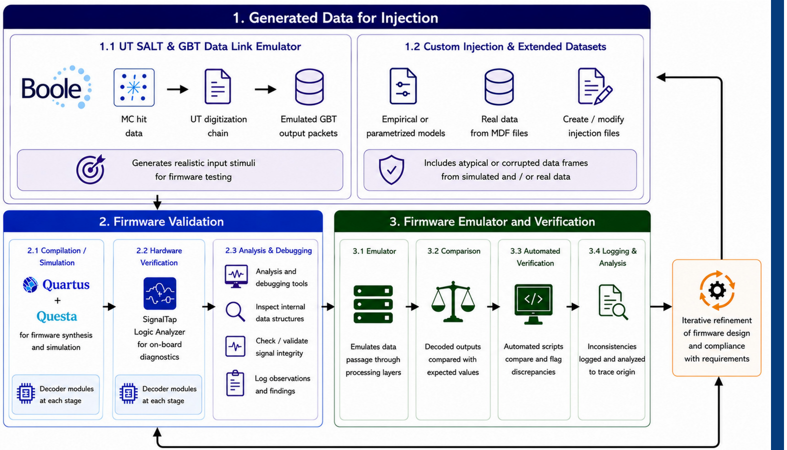
Data format allows all ASICs to report any of their non-standard packets with minimal disruption for the system and losing no data.





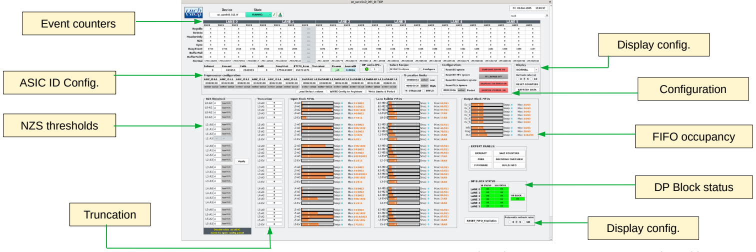
PCIe BW of 128Gbps not fully used.
Limiting factor is FPGA resource usage.

Verification and debugging



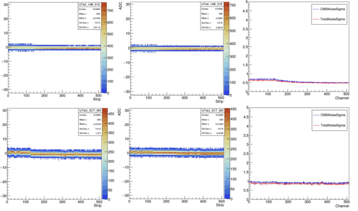
Software: control, analysis and decoding

EXPERIMENT CONTROL SYSTEM (ECS)



ANALYSIS AND DECODING

- Front-end calibration, temporal detector alignment, and online monitoring tools developed for the UT played an invaluable role in the hardware and firmware commissioning of the UT detector.
- Developed within the Gaudi event-processing framework, the standard software architecture used by LHCb.
- Vetra framework extended with TbUT reconstruction and monitoring algorithms for LHCb Collaboration data quality monitoring and validation.
- Analogue calibration and monitoring using precise baseline tuning with an 8-bit trim DAC register. Digital calibration and monitoring employing a complementary 6-bit pedestal register for baseline correction.
- Computation of common-mode noise and identification of low-voltage oscillation effects.
- Determination of hit thresholds based on common-mode–subtracted signal levels.
- Automated identification and masking of noisy and faulty detector channels.



[1] M. Firlej et al., *SALT3 chip documentation*, `https://twiki.cern.ch/twiki/pub/LHCb/StripAsic/salt_v5_spec.pdf`

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