Temperature-Induced Delay Drift in Xilinx FPGA Multi-gigabit Transceivers

Ruiyang Wang, Lingyun Li, Yonggang Wang

Department of Modern Physics, University of Science and Technology of China, Hefei Anhui, China

ABSTRACT – In large-scale physical experiments, the multi-gigabit transceivers (MGTs) in field-programmable gate arrays (FPGAs) have become a prevalent choice for high-precision clock distribution. However, the temperature-induced delay drift in MGTs poses a significant challenge to synchronization stability at picosecond levels. This paper characterizes the temperature coefficients of MGTs in a Xilinx Kintex UltraScale+ FPGA and implements temperature compensation in the system. Utilizing an on-chip, temperature-robust Dual-Mixer Time Difference (DDMTD) method, the temperature coefficients in the transmitter (TX) and receiver (RX) are measured as 1.42 ps/°C and 0.59 ps/°C respectively. After applying compensation, within a 35°C to 80°C range, the maximum drift of the clock distribution is reduced from 90.7 ps to 7.6 ps. The significant temperature effect in the TX is also theoretically analyzed.

Methodology and implementation

Fig. 1 shows the experimental setup of the proposed FPGA MGT-based clock distribution and synchronization system. The leader and follower nodes are implemented with two identical FPGA evaluation boards, linked by two 1-meter optical fibers (the temperature effect of the fibers is negligible due to their short length). The system clock is transmitted through the leader's MGT TX to the follower's MGT RX over the downlink fiber, while the recovered clock (RXRECCLKOUT) is transmitted back over the uplink fiber for automatic synchronization.

To characterize the temperature-induced delays accurately, an on-chip Dual-Mixer Time Difference (DDMTD) measurement method is utilized. The measurement steps are as follows: 1. The DDMTD (TX) module measures the phase difference between the leader's system clock and TXOUTCLKPCS (the final stage clock for serialized transmission) to reflect the TX delay and its thermal drift. 2. The DDMTD (loop) module measures the phase difference between the leader's system clock and the loop-backed recovered clock to reflect the total loop delay. 3. The RX delay is then derived by subtracting the measured TX delay from the loop delay.

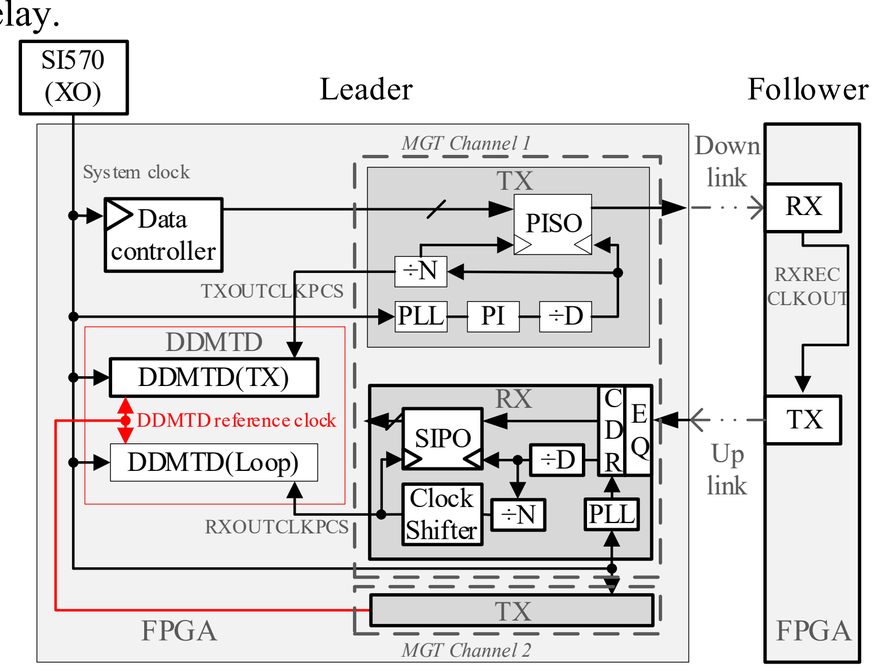

Fig. 1. Block diagram of the FPGA MGT-based clock distribution and synchronization system for temperature effects characterization and compensation.

Temperature-robust DDMTD

Traditionally, the DDMTD method requires an extra reference clock generated by a dedicated external source or an auxiliary PLL, which may introduce extra frequency drift or increase system complexity. To optimize this, a novel internal generation scheme was implemented, as shown in Fig. 2. This reference clock is generated directly from the system clock via the PLL, phase interpolator (PI), and D-Divider within MGT Channel 2. Consequently, although the system clock frequency varies with temperature, the generated DDMTD reference clock exhibits coherent drift, successfully maintaining a stable frequency difference and a constant measurement resolution.

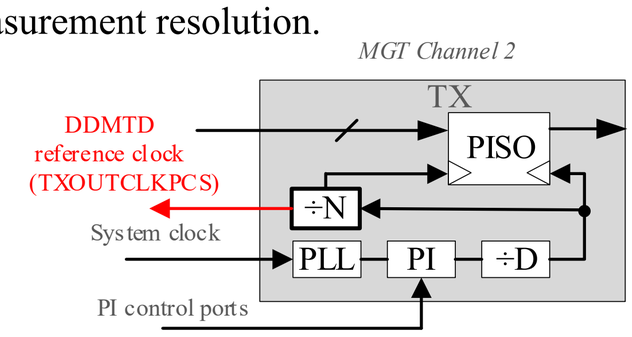

Fig. 2. Block diagram of the proposed temperature-robust DDMTD reference clock generation utilizing internal MGT resources.

Test Results

By varying the leader node's temperature, the measured TX and RX delay drifts exhibited linear coefficients of 1.42 ps/°C and 0.59 ps/°C, respectively (Fig. 3(a) and (b)). The notably larger TX drift is attributed to the PLL's steady-state error. For a step input, this error is calculated as

$$\theta_e(\infty) = \lim_{s\to\infty} \frac{s^2 \cdot 2\pi f_{in}}{s^2(s + K_0 K_d F(s)/N)} = \frac{Na \cdot 2\pi f_{in}}{K_0 K_d b}$$

where $F(s)$ represents the transfer function of the loop filter in the PLLs featuring non-zero constants a and b, and N is the frequency divider ratio. The parameters K_0 and K_d are temperature-dependent, constituting the primary source of temperature effects within the PLL and serving as the dominant contributors to the TX delay drift.

To ensure stability, bidirectional compensation was implemented by adjusting the TX Phase Interpolator (PI) on both nodes to counteract their combined drifts. As shown in Fig. 3(c), this compensation drastically reduced the maximum clock distribution drift from 90.7 ps to 7.6 ps across the 35°C – 80°C range.

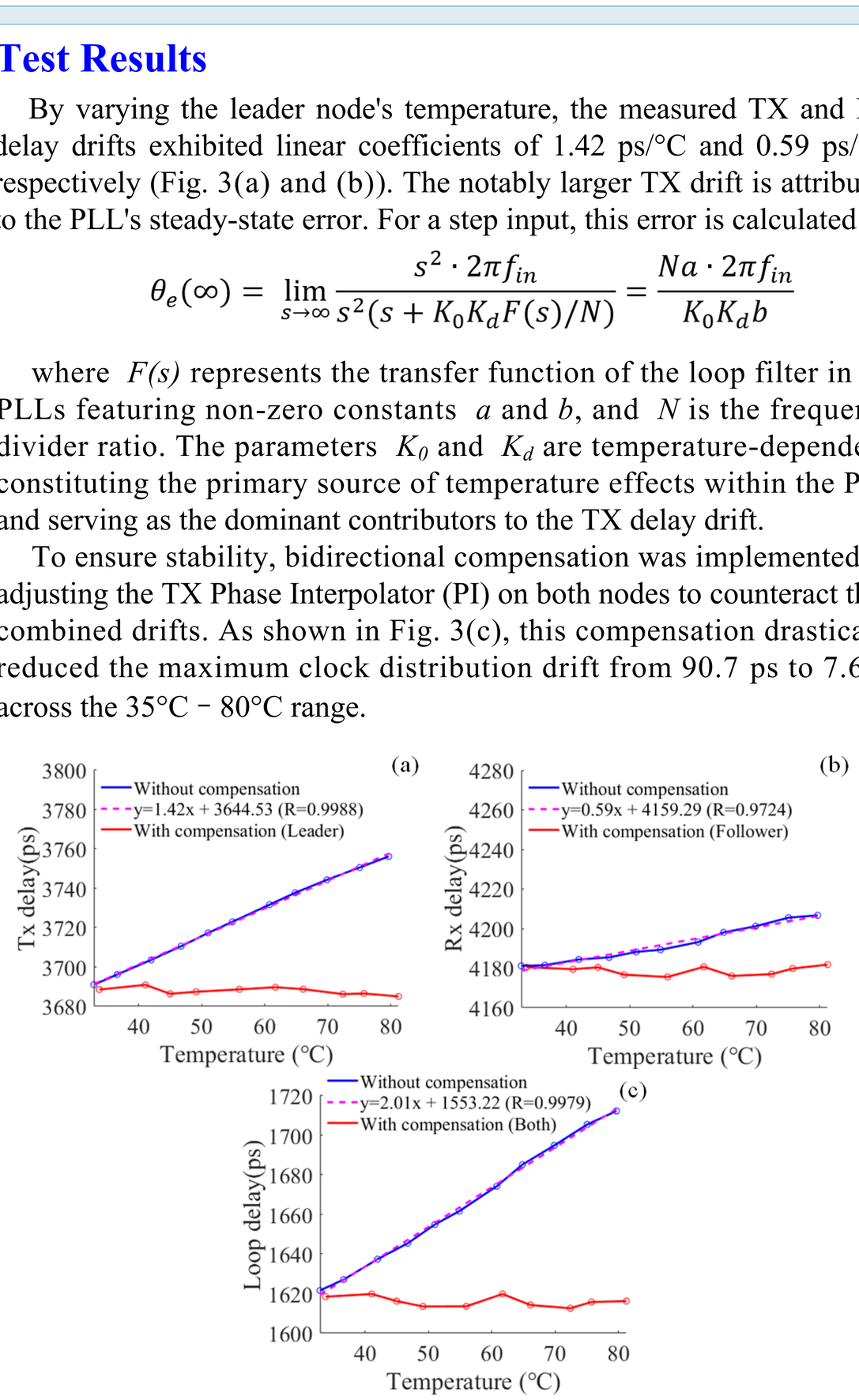

Fig. 3. Measured drift of (a) TX delay, (b) RX delay, and (c) loop delay under varying leader node temperature and fixed follower node temperature.

Conclusion

We proposed and implemented a novel on-chip, temperature-robust DDMTD measurement and bidirectional compensation method for FPGA MGT-based clock distribution and synchronization. Compared with the uncompensated conditions, the proposed scheme simplifies the overall architecture without the need for additional peripheral devices , and achieves a significantly better synchronization stability by reducing the maximum delay drift from 90.7 ps to 7.6 ps across a 35°C to 80°C range. Furthermore, we theoretically propose that the temperature-dependent steady-state error of the PLL is the dominant contributor to the TX delay drift.

Acknowlegement

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