25th IEEE Real Time Conference - May 25-29, 2026 - Elba, Italy

Development of the SAMIDARE Board: A New Acquisition System for TPCs

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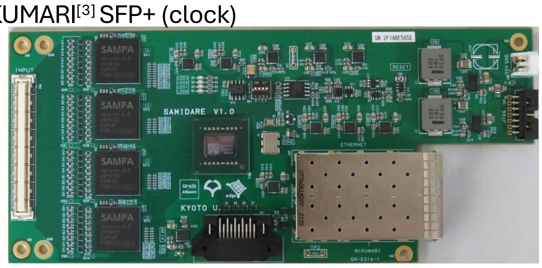
Introduction

- High-intensity beams require higher-throughput TPC readout.
- Active-target TPCs need many channels and online background rejection.
- GET electronics is becoming obsolete.
- Towards streaming-capable TPC front-end electronics.

SAMIDARE Board

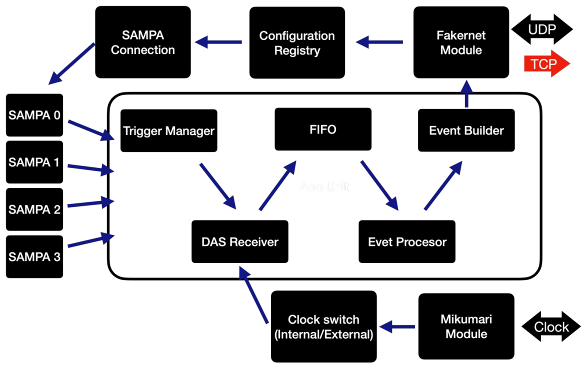
- 4 x SAMPA[1] chips (32 Ch, 10 bit @ 10 MHz)
- FPGA: Artix UltraScale+[2]
- 8 channels GPIO
- SFP+: GbE/10GbE
- MIKUMARI[3] SFP+ (clock)



Samidare prototype board

Firmware Design

The firmware implements the full acquisition path from the SAMPA data stream to Ethernet transmission. Its modular structure separates real-time parallel processing from sequential event formatting and readout.

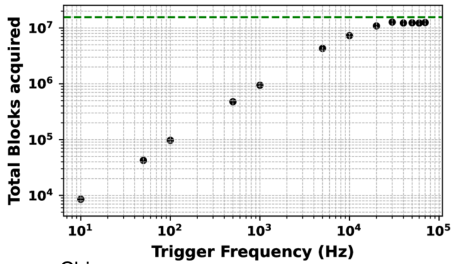


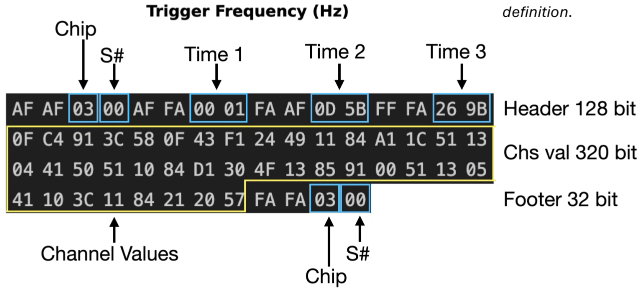
Firmware schematic implementation

Trigger Manager: buffers incoming samples and generates triggers from GPIO or threshold logic.
Data RX: stores a programmable pre/post-trigger window and adds timestamp, sample index, and chip ID.
Async FIFOs: one per SAMPA chip, used for buffering and clock-domain crossing.
Event Processor / Builder: reads event fragments, adds headers, and sends TCP payloads through Fakernet[4].
Clock: internal/external clock for standalone or synchronized multi-board operation.

Implementation

- End-to-end acquisition validated with prototype firmware[5] and backend software[6].
- Current bottleneck: 1 GbE TCP transmission path.
- Event fragments are formatted with header, channel payload, and footer.
- Metadata include chip ID, sample index, and timestamp information.





(Left) Number of event blocks acquired for 10 s acquisition run as a function of trigger rate. The green dashed line indicates the ideal maximum achievable with1 GbE link, excluding TCP headers. (Bottom) Event block definition.

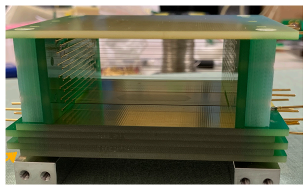
Applications and Outlooks

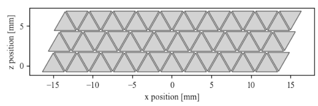
Current status

- SAMPA readout
- Trigger handling
- Pre/post-trigger window
- FIFO buffering
- Event encode/decode
- Data Transmission

Early Adoption [7] [Jan 2026]:

- 2 x 60 ch. Mini TPC) on a single board
- Self-trigger/External Clock





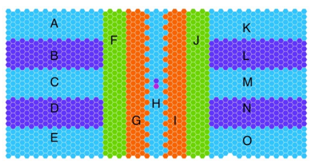
(Top) Mini TPC detector (Bottom) Mini TPC Anode readout pads

Future Development:

- 10 GbE data transmission.
- Zero suppression to reduce transferred data volume.
- Evaluation of SAMPA DSP mode.
- Event repackaging for more efficient backend handling.
- FPGA-based online filtering for beam-background rejection.

Future application [Early 2027]:

- TRIP Active Target TPC
- 1723 ch. on 15 SAMIDARE
- Inter-board Trig/Mikumari



TRIP Active Target TPC Anode Readout pads

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[5] https://github.com/spadi-alliance/SAMIDARE-StrADC
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References