GAROP3: A Gated Readout ASIC for the Proton Beam Monitor of the COMET Experiment

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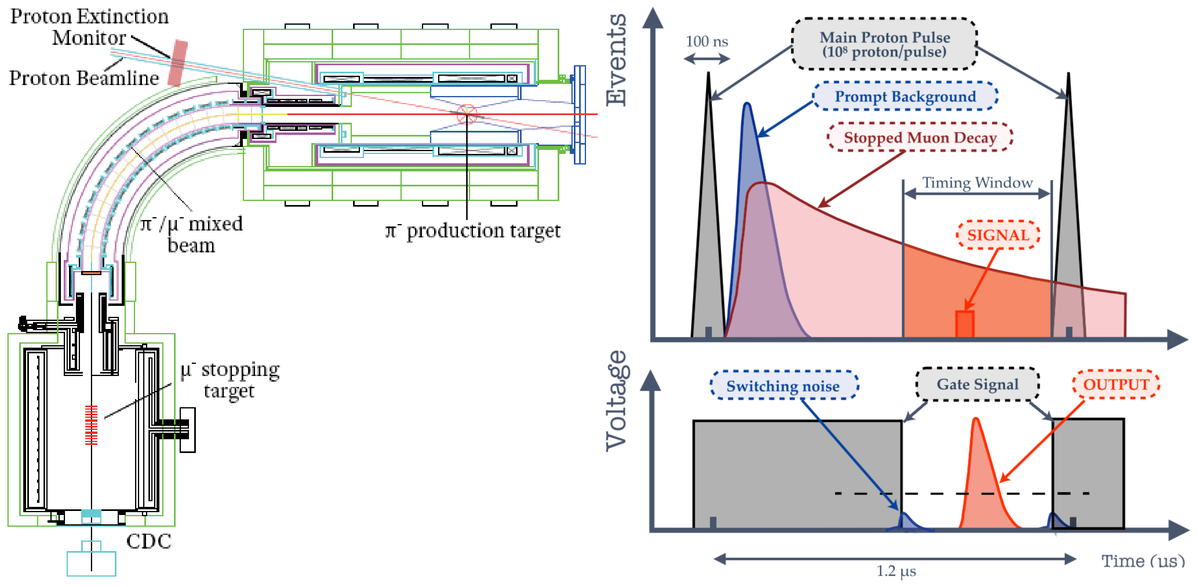
Points to Pick

- GAROP-3 is a readout chip that is continuously switching on-and-off at 1 MHz.
- It has multiple switches controlled independently to determine the optimal setup, which was successfully achieved.
- Two types of analogue circuits are compared in this chip.

Motivation

The GAROP (GAted-ReadOut Proton) is a readout circuit dedicated for the proton extinction monitor for the COMET (COherent Muon to Electron Transition) experiment.

The COMET searches for the rare neutrino-less $\mu - e$ transition process , where proton pulses are used to bombard a target to produce π^- and μ^-. A SiC pixel proton extinction monitor is proposed on the axis of the proton beam pipe to veto leaked protons. The monitor will be turned on by the gate only between proton bunches, and are turned off by the gate during the main bunch to prevent saturation. They only record the hit counts.



(a) The schematic of the COMET Phase-I. [1] (b) The duty cycle of the proton beam of J-PARC.[2]

Figure 1. The COMET schematic and J-PARC proton beam.

Designed Functions

Given the proposed application, GAROP should achieve:

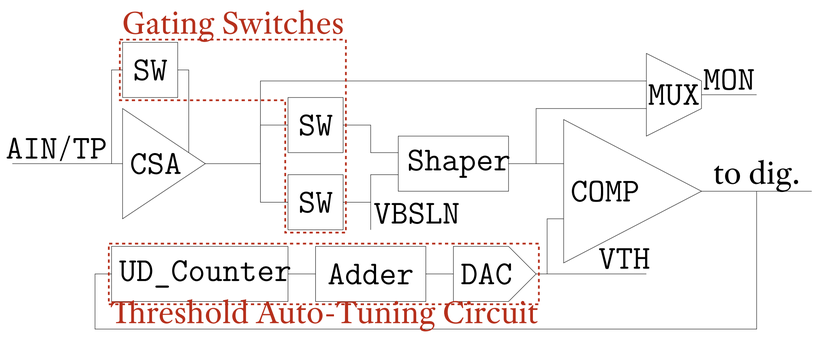
- **Signal Processing:** The chip should detect the charge pulse, and output hit count.
- **Gating:** A ∼1 MHz gate is required to turn off the GAROP during proton pulse.
- **Threshold Auto-Tuning:** To compensate for the manufacturing variation, the threshold voltage (VTH) at comparator should be tuned to meet shaper baseline.

Circuit Structure

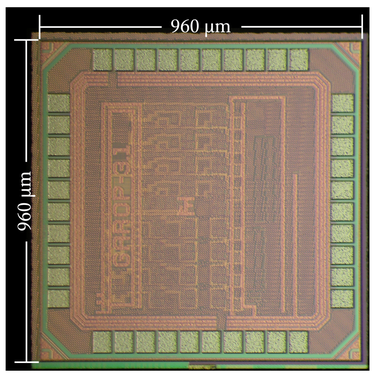
The GAROP-3 has two flavours of analogue circuits, namely type A & B. Type A uses a normal CRRC, while type B has two CRRC cascaded. Each flavour has four channels.

GAROP uses 65 nm technology and has a size of 960 μm × 960 μm. The circuit includes:

- **CSA** (Charge Sensitive Amplifier) receives charge and outputs a voltage shift.
- **CRRC Shaper** behaves as an integrator and amplifies the signal from the CSA.
- **Comparator** compares the shaper output and threshold voltage VTH.
- **Switch:** Three switches are used to control the circuit. The inputs of the three switches are now independent to allow gating sequence and delay tuning.
  - **SW_CSA** bypasses the CSA if turned on.
  - **SW_CRRC** cuts off signal path if turned off.
  - **SW_BSLN** passes the input level to shaper to prevent input floating if turned on.
- **Threshold Auto-Tuning Circuit** tunes the VTH to approach shaper baseline.
  - **UD_Counter** responds to the comparator output.
  - **Adder** applies an additional offset over the counter.
  - **DAC** interprets the bits from counter and adder into VTH.
- **Register:** A series of daisy chain SPI registers are responsible for enabling the functionalities and controlling the digital circuits.



(a) A simplified schematic of one analogue channel of the GAROP-3.



(b) The GAROP-3 die-shot.

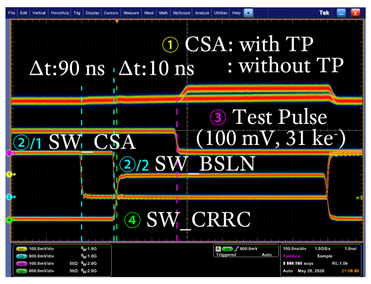
Figure 2. The GAROP-3 single channel schematic and photo.

Gating Results

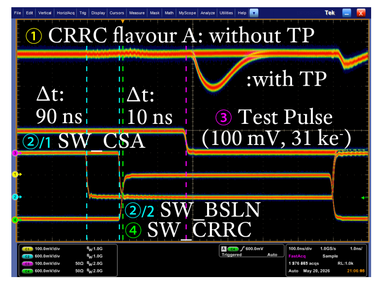
The optimum operation point of the analogue circuit was different depending on whether it was gated or not. Thus, all tests were conducted with a gating period of 1.2 μs.

Five chips were tested, yet an assembly issue caused extra thermal cycles for all samples, and three showed compromised performance. The results below come from #5.

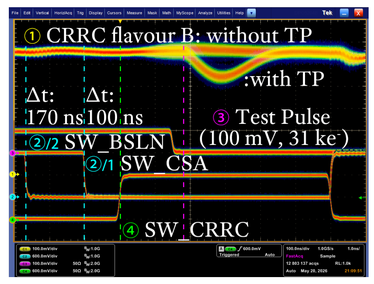
The measurement was conducted by injecting a pulse into an in-chip 50 fF capacitor, and the VTP was 20, 50, 100, 200 and 300 mV , or equivalently 6, 15, 31, 62 and 93 ke^-.



(a) CSA under gating.



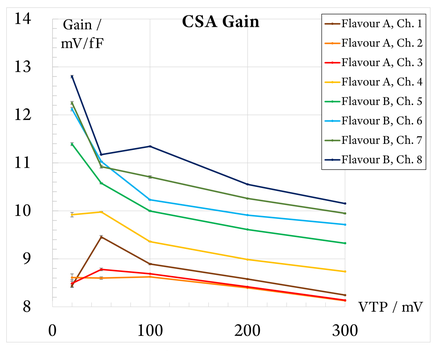
(b) CRRC flavour A under gating.



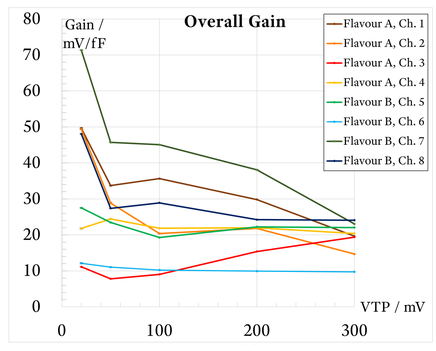
(c) CRRC flavour B under gating.

Figure 3. The GAROP-3 gating test results.

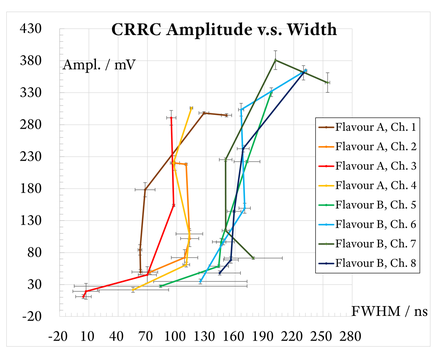
The delays between gating signals were tuned to eliminate the switching noise, as shown in Fig.3. Fig.3c shows that, different flavours request different gating setup.



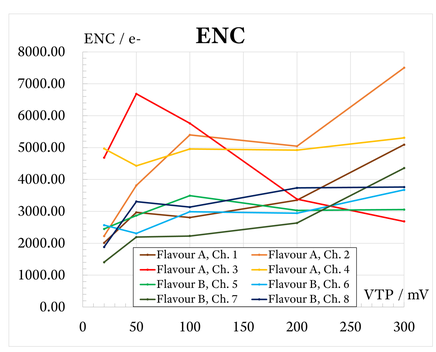
(a) CSA gain.



(b) Overall gain.



(c) CRRC shape.



(d) Overall ENC.

Figure 4. The GAROP-3 gain and waveform measurement results.

Both flavours work well for VTP within 50-200 mV. Smaller signals cannot be distinguished from the baseline; while larger signals cause saturation for both flavours. The flavours differ in the waveform width more than the amplitude, as shown in Fig.4c.

Manufacturing variation also contributes to the performance difference. Future cross-chip tests will investigate whether the difference is related to the position of the channels.

Threshold Auto-Tuning Circuit

In threshold tuning mode, the counter will raise VTH if it is lower than the shaper output, and vice versa. Then it can be frozen, at which point an offset can be added to VTH.

The idea of this circuit has been validated in GAROP-2, yet the clock signal crosstalk and shaper baseline noise prevented us from reaching optimal performance in that test.

GAROP-3 uses an external clock, yet the counter was not triggered. Also, testing on the adder indicated that the DAC could only drive 160 mV to VTH, far below the shaper baseline of 360 mV. The incorrect DAC output buffering could be the major reason for this.

Conclusion

The test of the first GAROP-3 samples validated it as a prototype front-end readout chip with MHz level gating. Furthermore, the uncoupled gating signal allows investigation into the optimum gating sequence and delay setup, and finally the possible signal window, which was not feasible in the previous iterations.

The threshold-tuning circuit failed due to the low driving limit of the DAC, requiring optimized output buffering of the DAC to fulfill all functionalities intended.

References

[1] Tetsuichi Kishishita et al. “SiC p+ n junction diodes toward beam monitor applications”. In: ***IEEE Transactions on Nuclear Science*** 68.12 (2021), pp. 2787–2793.

[2] Tetsuichi Kishishita et al. “Hybrid SiC Pixel Detector for Charged-Particle Beam Monitor”. In: ***IEEE Transactions on Nuclear Science*** 70.6 (2023), pp. 1210–1214.