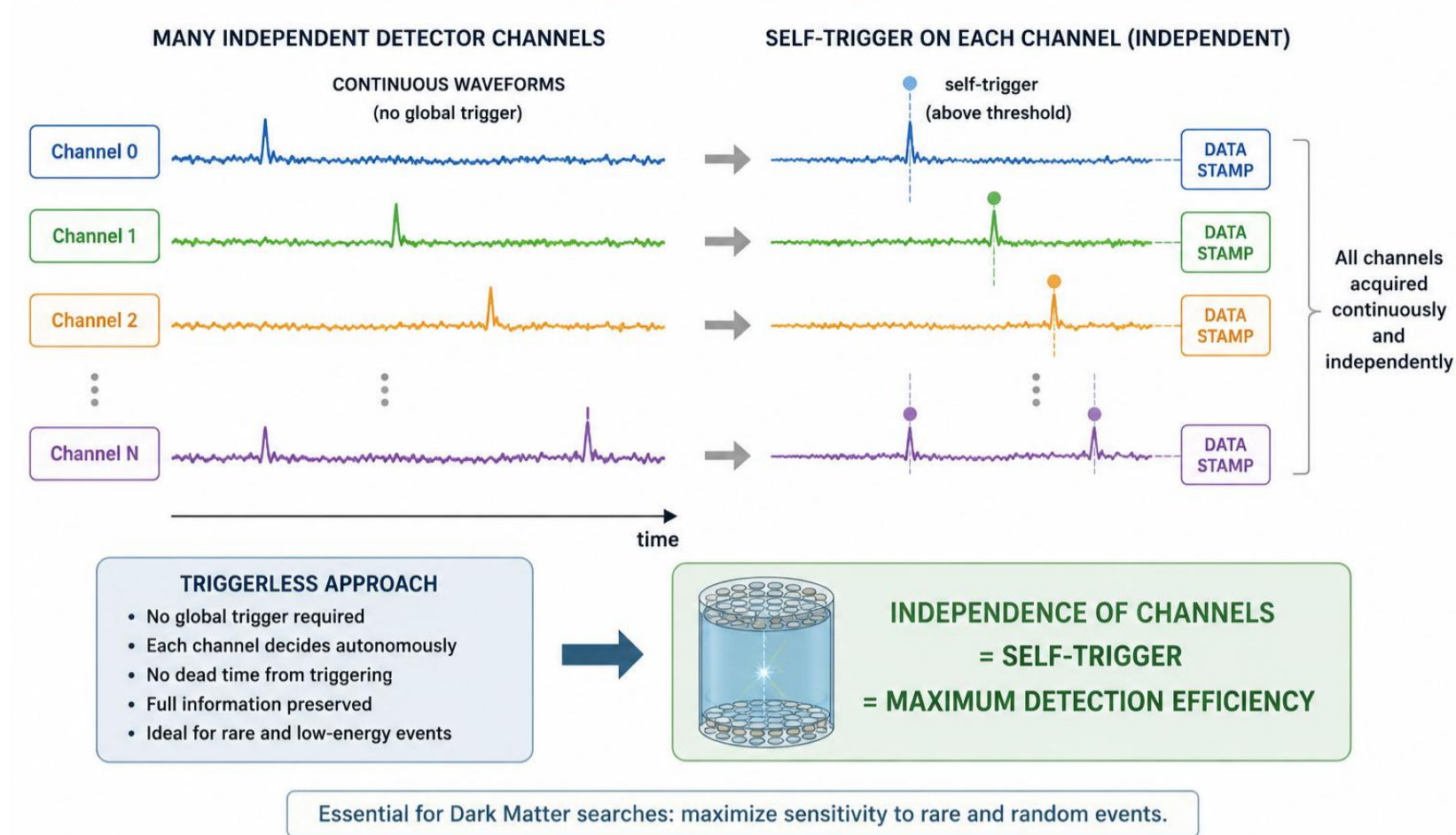


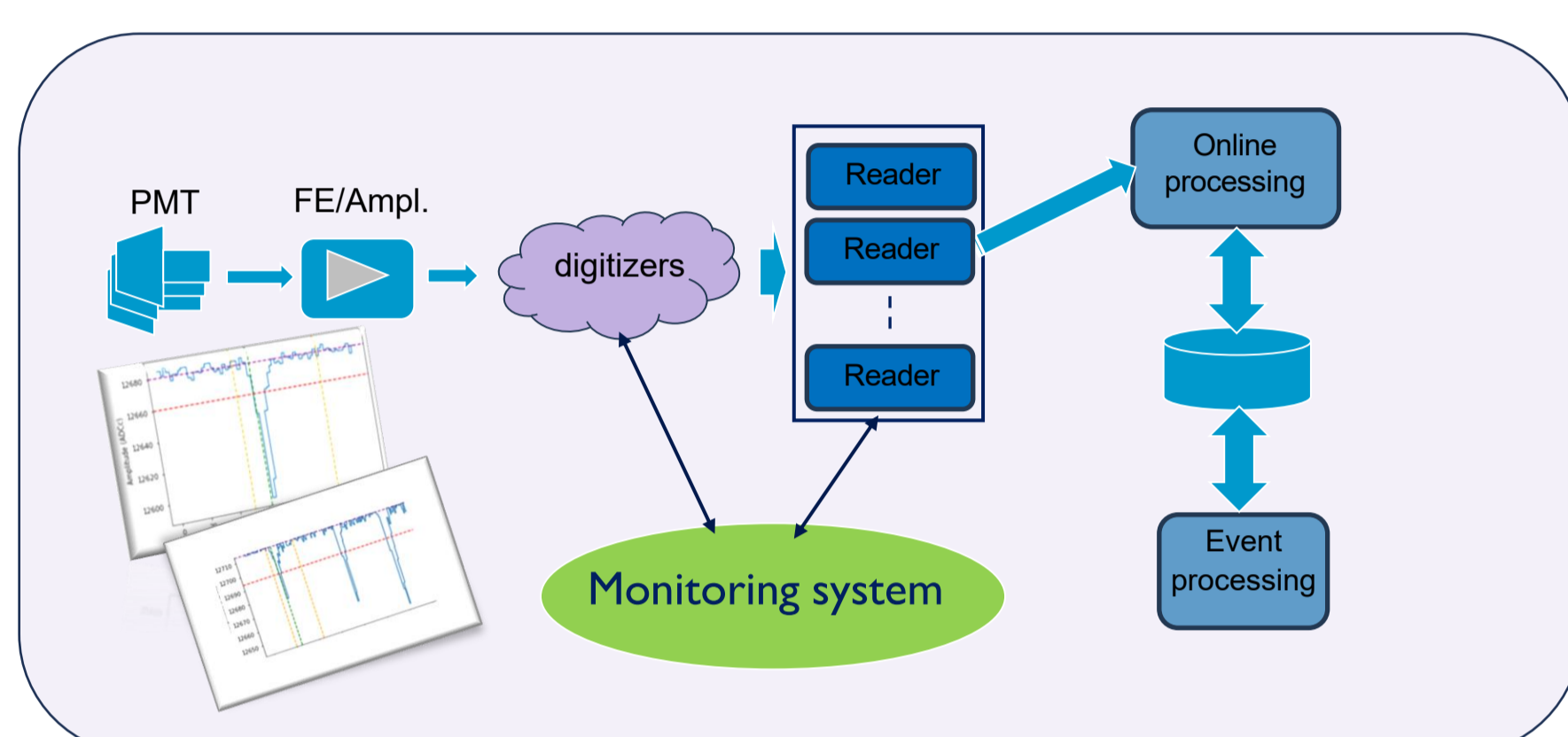
TRIGGERLESS DAQ IN DARK MATTER EXPERIMENTS

Continuous and independent data acquisition on each channel



- Next-generation direct dark matter experiments require large detectors with thousands of readout channels, ultra-low background conditions, and very low energy thresholds to maximize sensitivity to rare WIMP interactions.
- Conventional trigger-based DAQ systems limit flexibility, scalability, and sensitivity, especially for low-energy signals, calibration runs, and non-standard physics analyses.
- Triggerless DAQ architectures overcome these limitations by continuously digitizing and time-stamping detector signals, allowing event reconstruction and selection to be performed offline through temporal correlations.
- Continuous high-throughput data acquisition requires real-time monitoring and control systems capable of tracking buffer occupancy, synchronization, throughput, and errors.
- FPGA-based online monitoring systems provide low-latency hardware-level supervision of the DAQ data flow without interfering with the acquisition stream.

Front-End electronics & online processing



Triggerless DAQ Architectures

- detector signal are **continuously digitized** and time-stamped
 - Down to a fraction of SPE on short duration (< 100 ns)
 - Up to thousands of SPE (~ hundreds of μ s)
- **event reconstruction** is performed **offline** using temporal correlations.
- multiple, analysis-specific event definitions and supports a broader range of physics searches, detector commissioning activities, and calibration campaigns.

The Monitoring System

It operates on CPU-based systems after data have been transferred through the DAQ chain. In triggerless architectures with continuous data streams and very high channel counts, software-only monitoring may introduce:

- Software**
- latency
 - additional bandwidth usage
 - CPU overhead
 - limited scalability



It observes the data stream in real time without interfering with acquisition. It is particularly effective for:

- Hardware**
- buffer occupancy tracking
 - timing synchronization
 - throughput measurements
 - link integrity checks
 - error detection
 - low-latency alarm generation

It scales efficiently with large detector systems and high data rates typical of next-generation dark matter and neutrino experiments.

Interface between readout modules and data processing and Calibration system

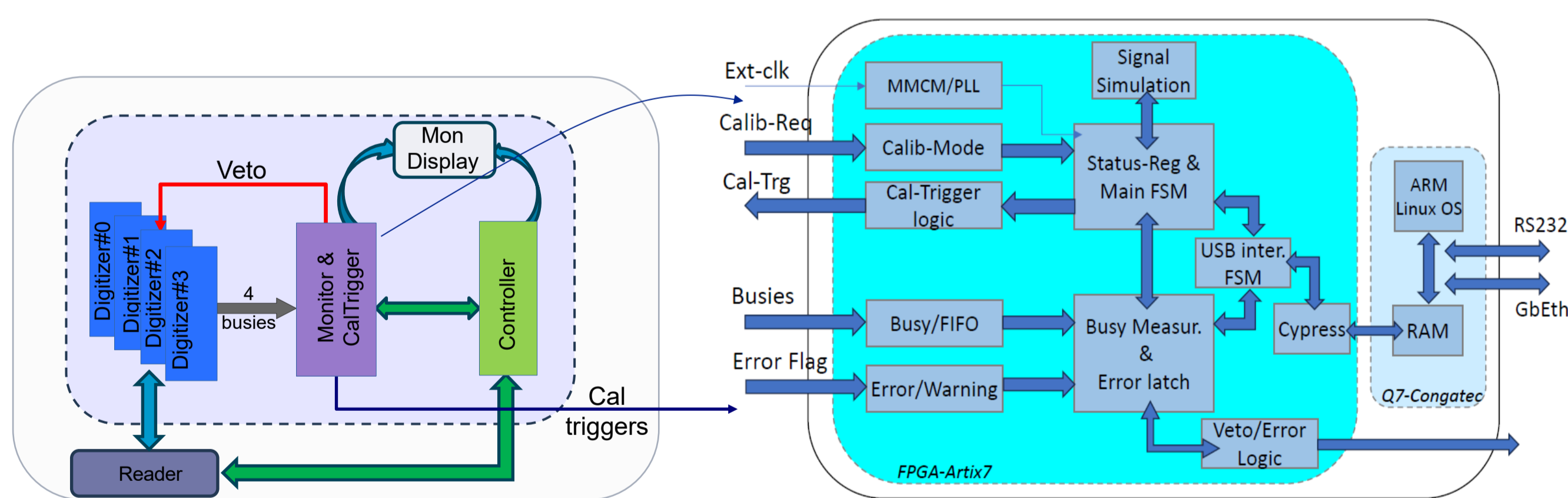
- ✓ **distribution of timing signals** (Veto, Start of digitization etc..) during the science runs and triggers during calibration runs

Hardware real-time control

- ✓ Dead time (Busy) monitor for each channel to optimize the overall performance
- ✓ Real-time selection of a complex Busy pattern as a logic-analyzer
- ✓ Troubleshoot the system in case of an error or anomalous data transfer (i.e. due to detector noise or faults in the DAQ equipment)

Architecture & implementation

Monitoring board: **interface** between the **DAQ modules** and **Controller** and **Calibration**



Digitizer setup

- ✓ 4 Fast digitizers (CAEN V1730S): 14-bit resolution @500 MHz sampling rate
- ✓ FW: digital pulse processing with dynamic acquisition windows (**DPP-DAW**)
 - baseline suppression
 - dynamically-sized acquisition windows
 - **Self-Trigger mode** with a 9-10 ADC count threshold values ~ heavily driven by electronic noise

FPGA-based monitoring board

The board is equipped with an FPGA-Artix7 and **Q7-congatec** embedded processor:

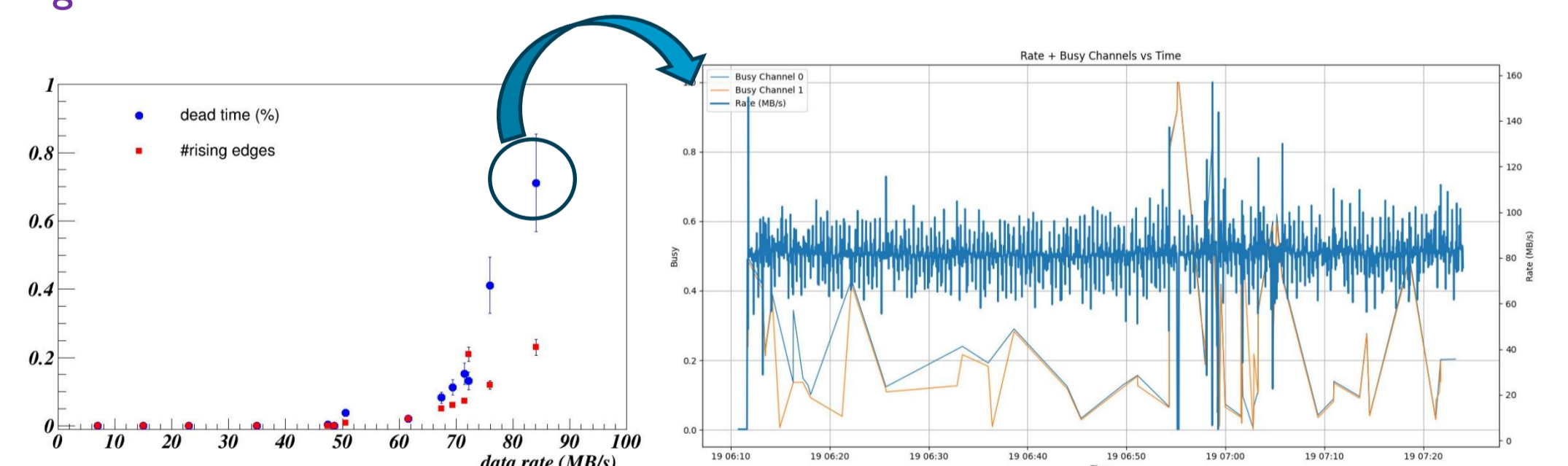
- The FPGA manages the I/O peripherals, Busy/Veto logic, Error/Warning latches, data throughput and Calibration trigger Logic
- Thanks to a fast connection between FPGA and processor (PCIx and USB2) the monitoring data can be processed and published on the web monitor service

The board has been successfully used in DAQ system for Muon g-2 Calibration system[1][2]

Test Results

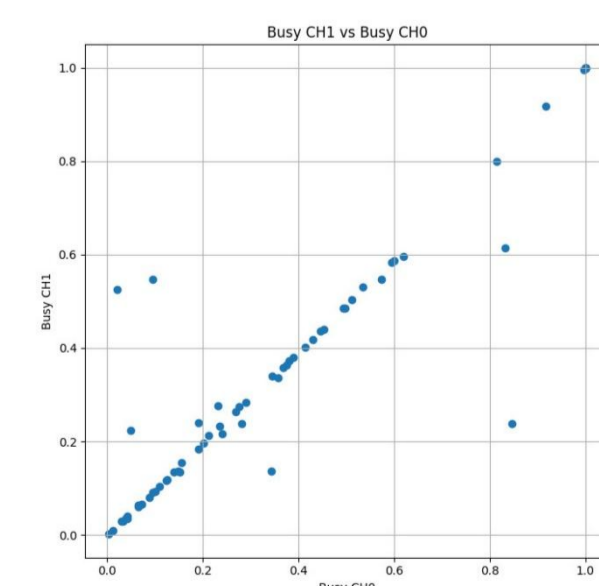
Tests and installation

The board has been configured to monitor busy signals, Unlock PLL conditions, FIFO status etc.. to evaluate the stability and performance of the DAQ system. Within this test, a PCI card (CAEN A5818) has been used to readout the digitizers.

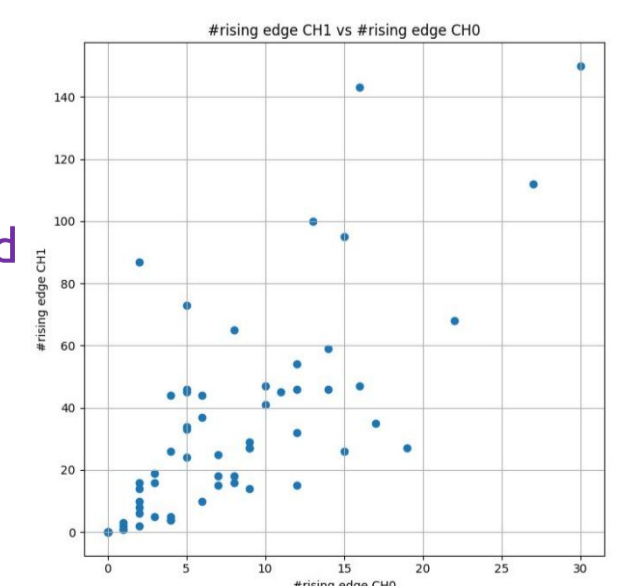


Duty cycle and the number rising edges shown versus the data rate for different ADC threshold settings.

Data link fully saturated (> 85 MB/s): Busy dead cycle ~ 0% except for some spikes that reach 20%.



Good correlation between the two Busy duty cycles and # rising edges



Conclusions

The FPGA-based monitoring board demonstrated the capability to provide real-time diagnostics of the DAQ. Following successful validation, the VHDL design was further optimized and implemented on CAEN V2495 FPGA board, enabling tighter integration with the Neutron Veto DAQ system while improving the reliability and long-term stability of triggerless readout. Its successful deployment demonstrates the effectiveness of FPGA-based low-level monitoring solutions for large-scale triggerless DAQ systems and represents a scalable approach for future multi-ton dark matter experiments.

References:

- [1] A. Anastasi et al., "The laser control of the muon g-2 experiment at Fermilab", JINST 13 (2018) no.02, T02009
[2] S. Mastroianni, "The Readout Controller for the Calibration System of the Muon g-2 experiment", IEEE Trans. Nucl. Sci., 65 (2018), 1033.

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