

AI Enhanced LLRF Controller for Ultra-lightweight SC Cyclotron CYCIAE-100B

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Abstract

The China Institute of Atomic Energy (CIAE) is developing an ultra-lightweight, high-temperature superconducting cyclotron accelerator CYCIAE-100B. This cyclotron operates under high beam current loads and requires fully automated, unattended operation of the RF system. The cyclotron RF cavity is driven by a 20-kW solid-state power amplifier, directly coupled to a high-Q load, and controlled by the LLRF system at 77 MHz. The LLRF system maintains stable amplitude and phase control of the RF field and determines when to establish or withdraw RF voltage. This paper presents a digital LLRF controller designed for CYCIAE-100B, which operates in generator-driven mode. The hardware is based on the System-on-Chip (SoC) chip ZYNQ-7045 and integrates high-speed AD/DA converters to achieve digital demodulation/modulation and fast PID algorithms for amplitude-phase control. It includes a phase-adjusting network to align high-speed sampling phases. To achieve automatic fault recovery, advanced interlock protection logic is implemented in the firmware. Spark detection is performed through digital signal tracking, and corresponding protection is implemented via fuzzy logic control. Additionally, supervised learning is integrated into the LLRF system to diagnose RF system faults. During cyclotron testing, RF system parameters (e.g., the driven, detuning, forward, reflected, and sparks) are recorded in real time upon triggering. This dataset will be used for machine learning (ML) fault module training, which is expected to yield valuable results for the LLRF protection logic. This paper reviews the design of the digital LLRF controller and presents preliminary test results.

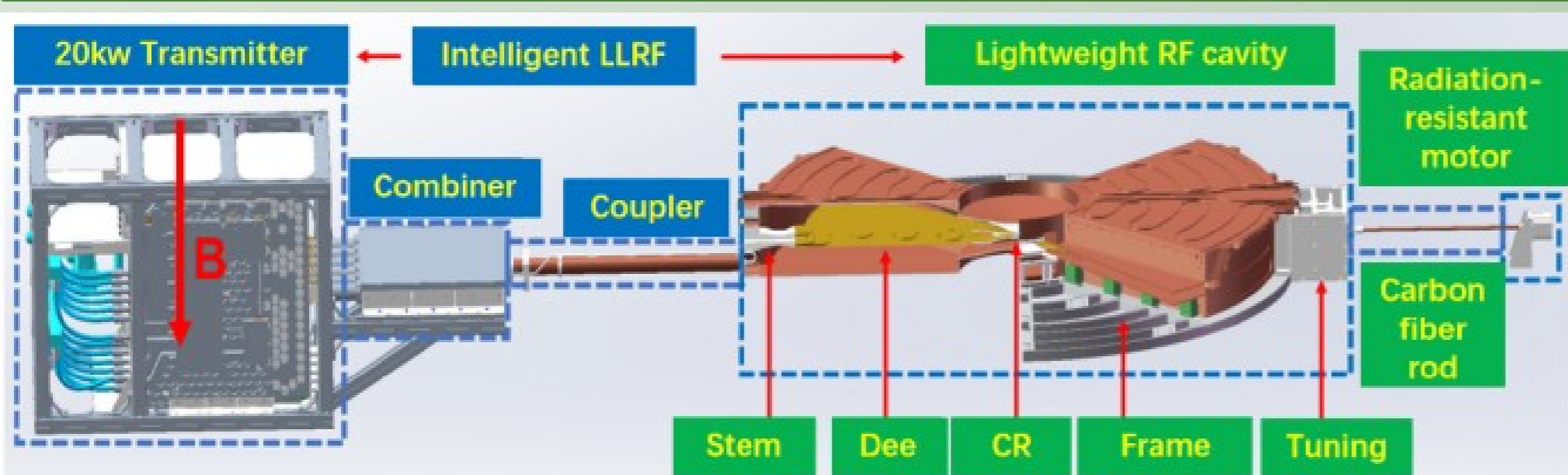
Ultra-lightweight SC Cyclotron CYCIAE-100B

100 MeV high-temperature superconducting cyclotron

- Extracted proton beam current: ~10uA
- Iron-free magnet configuration

RF system of CYCIAE-100B

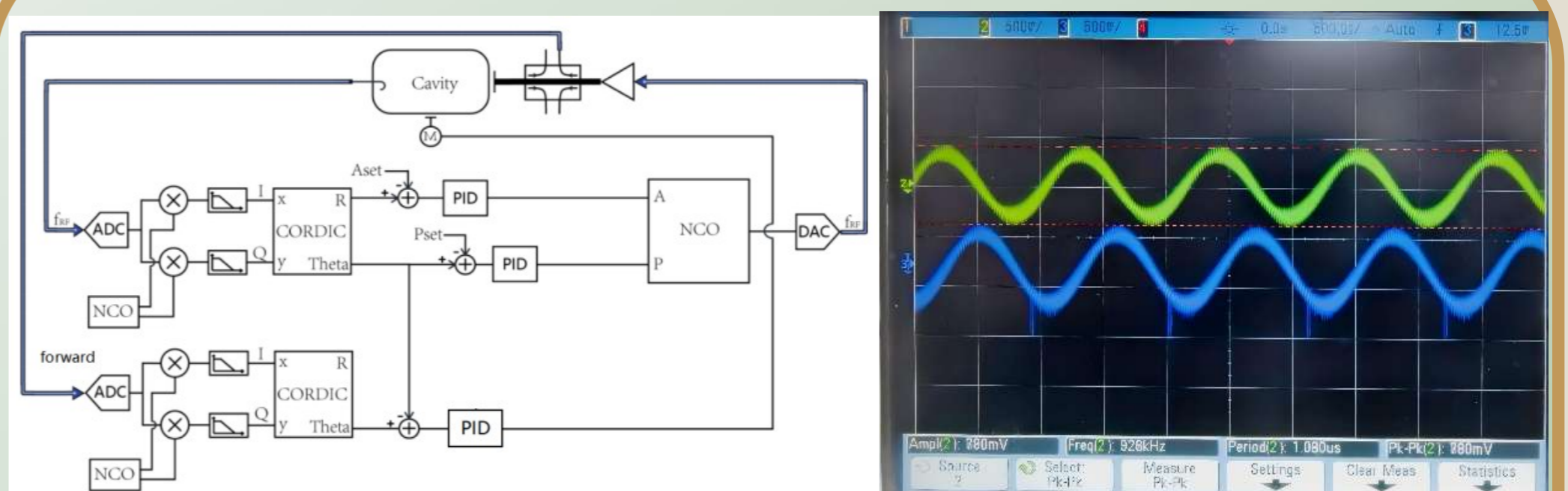
- A lightweight, high-Q cavity
- A compact solid-state amplifier
- An intelligent LLRF



RF system parameters

RF frequency	~77 MHz
Harmonic Mode	2
Number of cavities	2
Unloaded quality factor	5040
Transmitter power	20 kW
Dissipated power	17 kW

The tuning loop and A/P controller



Control Loop and the testing of modulated signal output

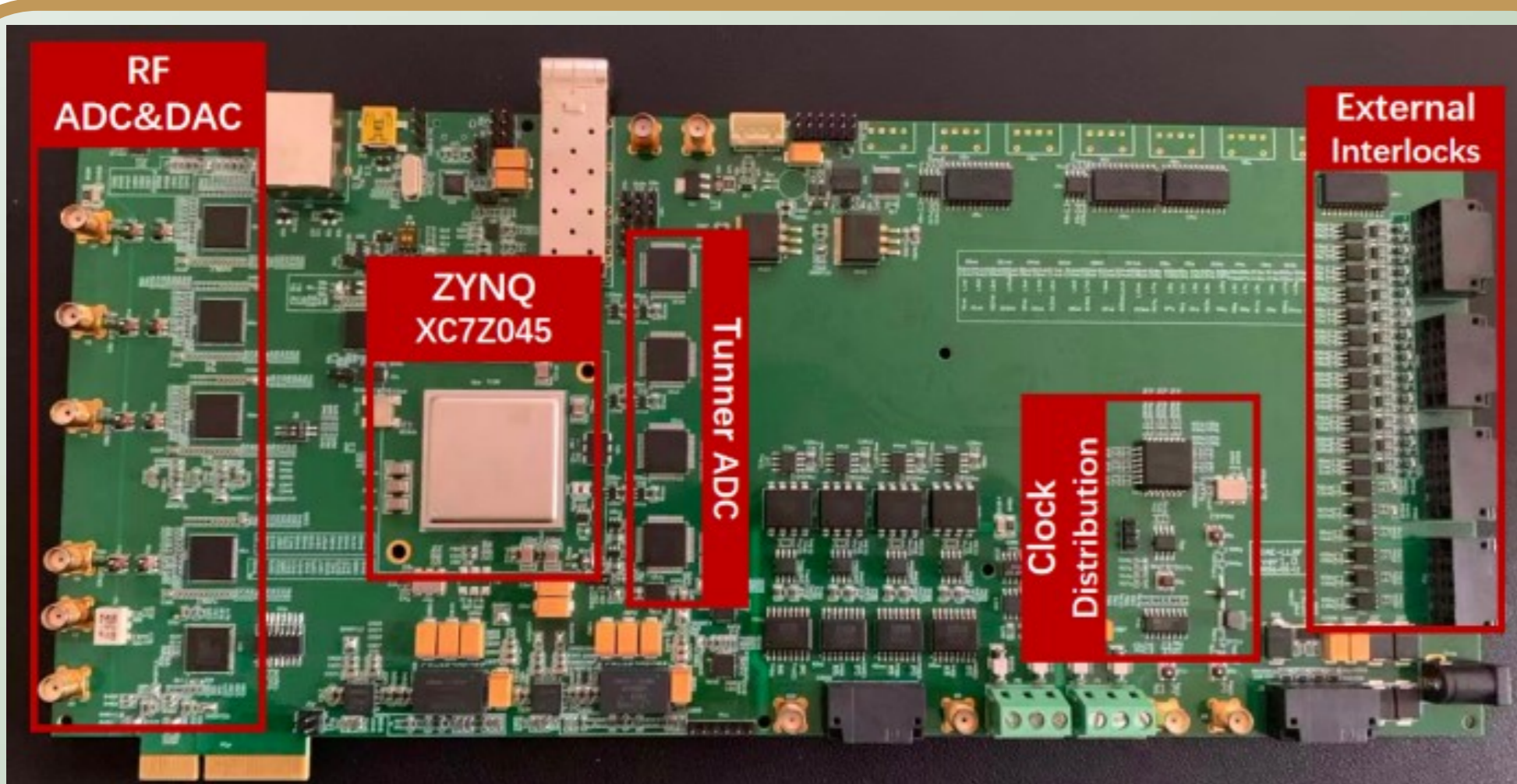
Tuning Loop

- A pre-tuning module is designed to perform tuning at low power.
- For cavity tuning control, a sample signal is usually taken from both the cavity and the transmission line. The phase difference between these two signals is calculated.
- A PID algorithm then dynamically adjusts the output value. This output drives the tuning motor via a PWM module.

A/P controller

- A/P demodulation is achieved by DDC and CORDIC.
- Using direct digital synthesis (DDS) for modulation.

The Hardware of LLRF

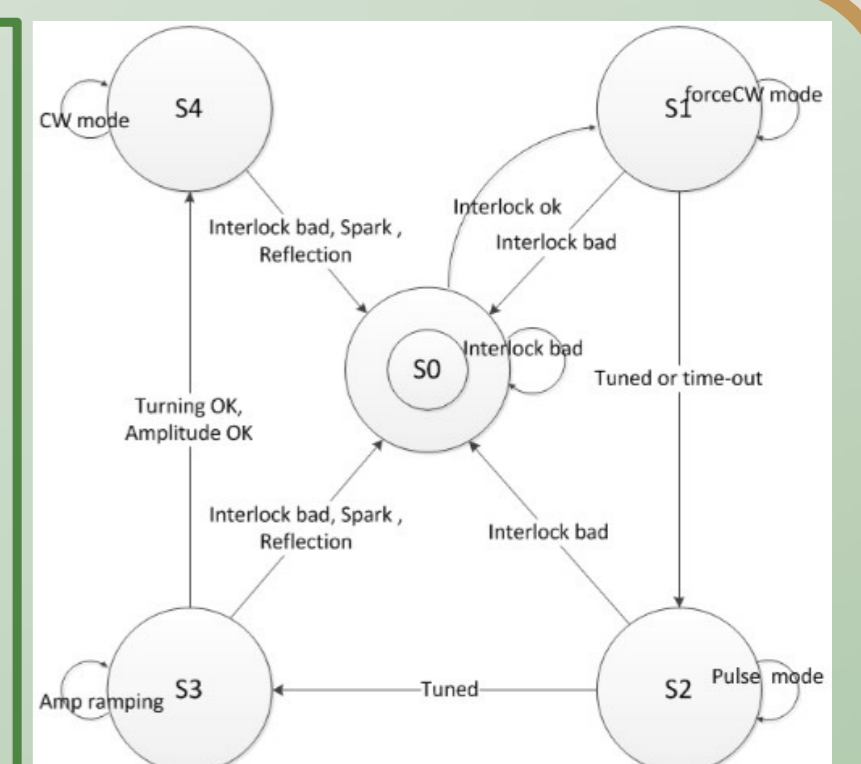


The fully digital low-level system is implemented as a highly integrated digital board on a 14-layer PCB measuring 20 cm × 15 cm. The hardware design follows a high-speed ADC + SoC + DAC architecture, in which high-speed ADCs directly sample the RF signal.

The application of intelligent algorithms in LLRF

Automatic start of the RF system

- The F.S.M is configured in the core to guide the LLRF to perform corresponding actions based on the state transition sequence.
- Using supervised learning to determine the optimal cavity startup timing and improve startup success rate.



Interlock protection loop:

- **Arcing:** The comparator detects when the envelope falls below a preset threshold. A fuzzy logic controller activates the appropriate interlock-protection rules based on the corresponding membership degree derived from the count.
- **Excessive reflected power:** The LLRF logs parameters during fault, which are then sent to a supervised learning model for offline training. The trained model is subsequently deployed on the FPGA.

Conclusions

CIAE is developing an ultra-lightweight, high-temperature superconducting cyclotron, CYCIAE-100B, for which a dedicated digital LLRF controller has been designed. The hardware is based on the SoC device ZYNQ-7045, integrating high-speed analog-to-digital converters and digital-to-analog converters. The RF field is maintained by a digital amplitude-phase controller. Digital phase detectors achieve tuning, and the pre-tuning method accelerates the establishment of the RF field. Moreover, intelligence-oriented research has been conducted for this LLRF system, combining supervised learning to select the best startup strategies and diagnose the causes of anomalies. Additionally, fuzzy logic control has been implemented to monitor sparks. Preliminary test results indicate that the LLRF system has achieved digital control and demonstrates performance suitable for intelligent applications.