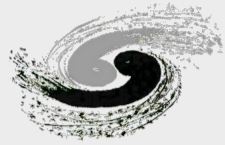


# A Full Trigger Data Readout Scheme for the BESIII MDC Subtrigger System



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## Motivation

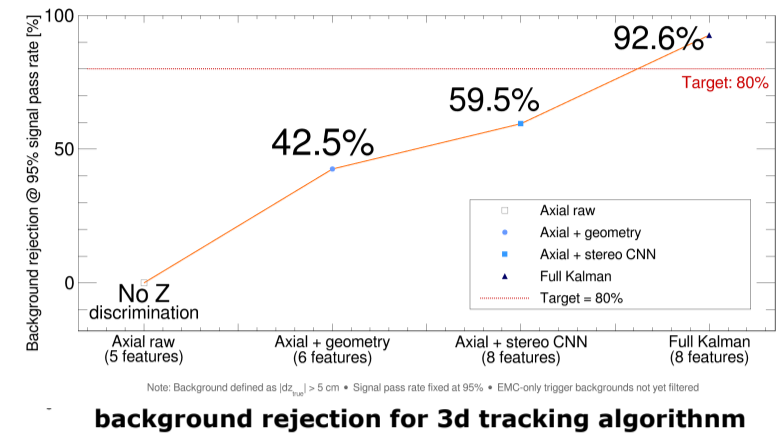
The BESIII luminosity upgrade will increase the background level and event complexity in the future. The MDC stereo-wire layers provide additional spatial information, making 3D track trigger algorithms a promising upgrade direction for background suppression. To better study and develop such trigger algorithms, access to raw MDC detector data is essential.

**This work focuses on:**

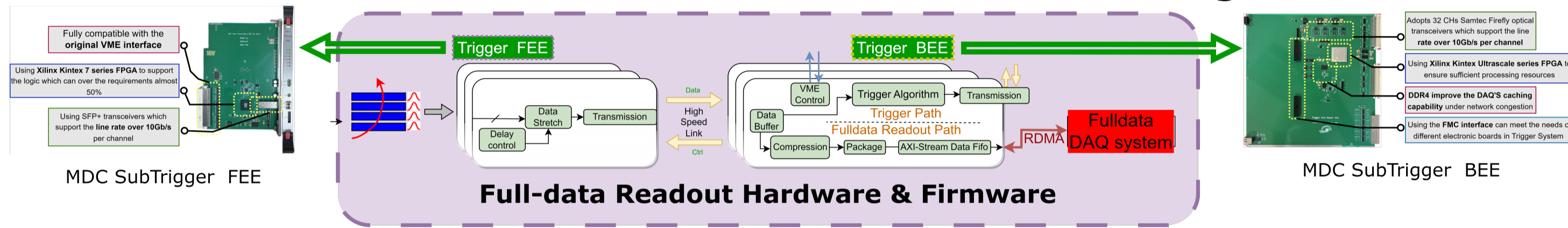
- Building a full trigger data readout path based on the new MDC Sub-trigger FEE/BEE electronics and high-speed links
- Designing a data compression and block-based packaging scheme for continuous MDC raw data
- Using RDMA-based transmission to read out complete data blocks to a server for offline analysis and validation

Table 1: MDC layer structure and geometry parameters.

Superlayer	Type	N <sub>layer</sub>	N <sub>wire</sub> / layer	Radius (mm)	Length (mm)
3	A	4	76,76,88,88	197 - 246	1092 - 1272
4	A	4	100,100,112,112	262 - 311	1442 - 1612
5	A	4	128,128,140,140	327 - 375	1782 - 1952
6	U	4	160 × 4	400 - 448	2174 - 2192
7	V	4	176 × 4	464 - 514	2198 - 2216
8	U	4	208 × 4	530 - 579	2222 - 2240
9	V	4	240 × 4	595 - 642	2246 - 2264
10	A	4	256 × 4	667 - 716	2276 - 2294
11	A	3	288 × 3	732 - 763	2300 - 2306



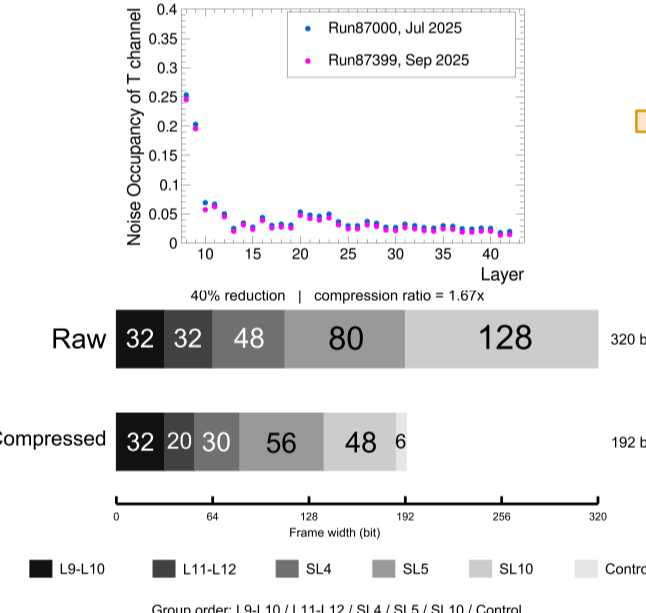
## Full-Data Readout Workflow & Frame Design



### 01 Raw Data and Compression

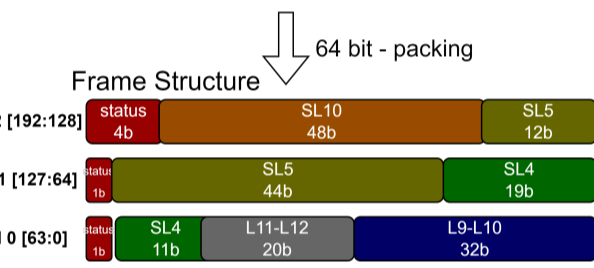
The detector's original bitmap contains many '0' and only a few '1', so zero compression is the most effective compression strategy; Meanwhile, the hit rates vary across different superlayers.

In response to the different fire rates at different layers, we also designed different compression ratios for different layers



### 02 Block Builder & Frame

After zero suppression  
L9-L10 (32b), L11-L12 (20b), SL4 (30b), SL5 (56b), SL10 (48b)

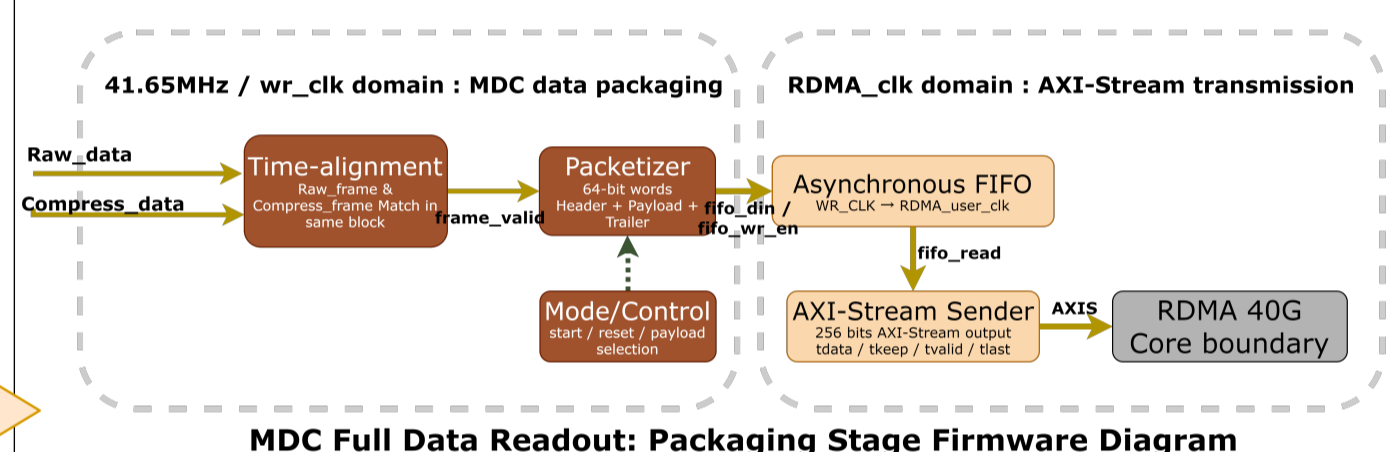


- Add Header & Trailer
- Timestamp
- Frame counter
- Data Type Control
- Payload Length
- Overflow Symbol

#### One Block (example)

Mode 0 (Compressed)  
192 bit × 256 = 49152 bit  
= 6144 Byte  
Header + Trailer = 128 bit  
Total = 6160 Byte

### 03 Packetizer & AXI-Stream

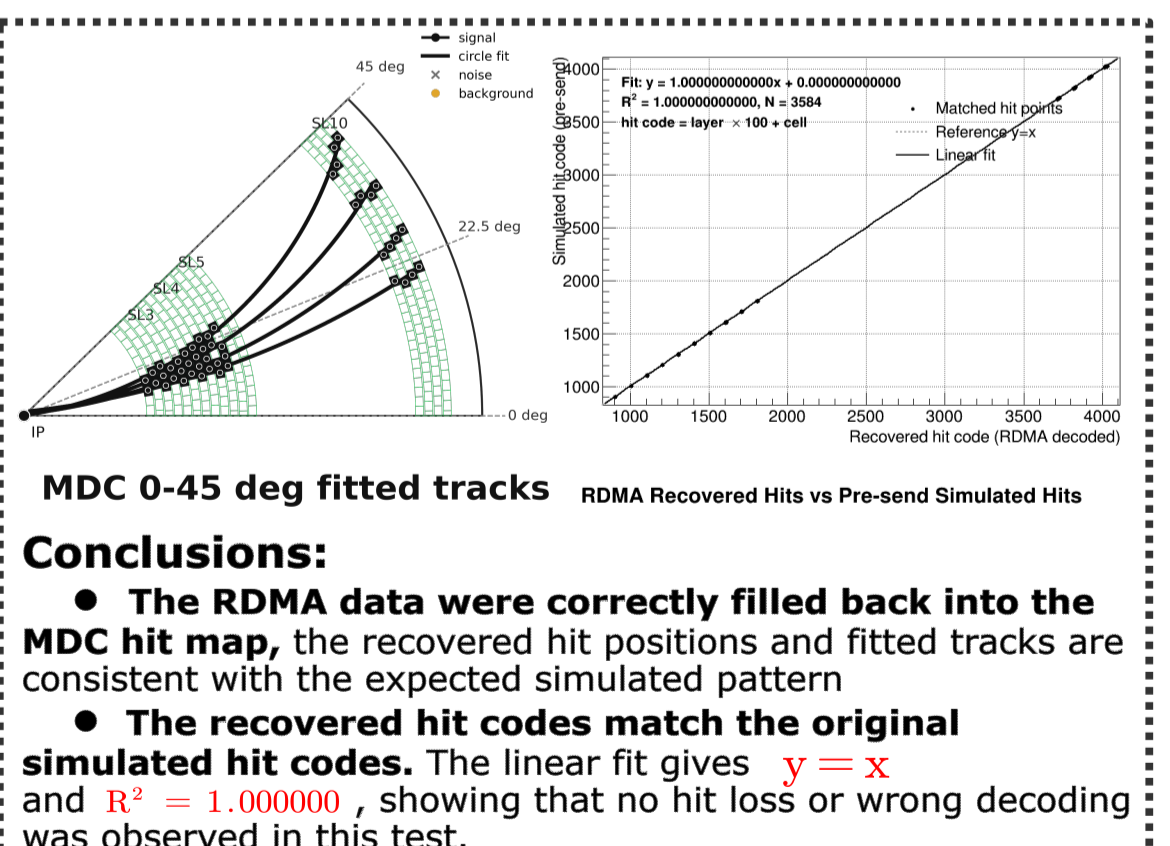
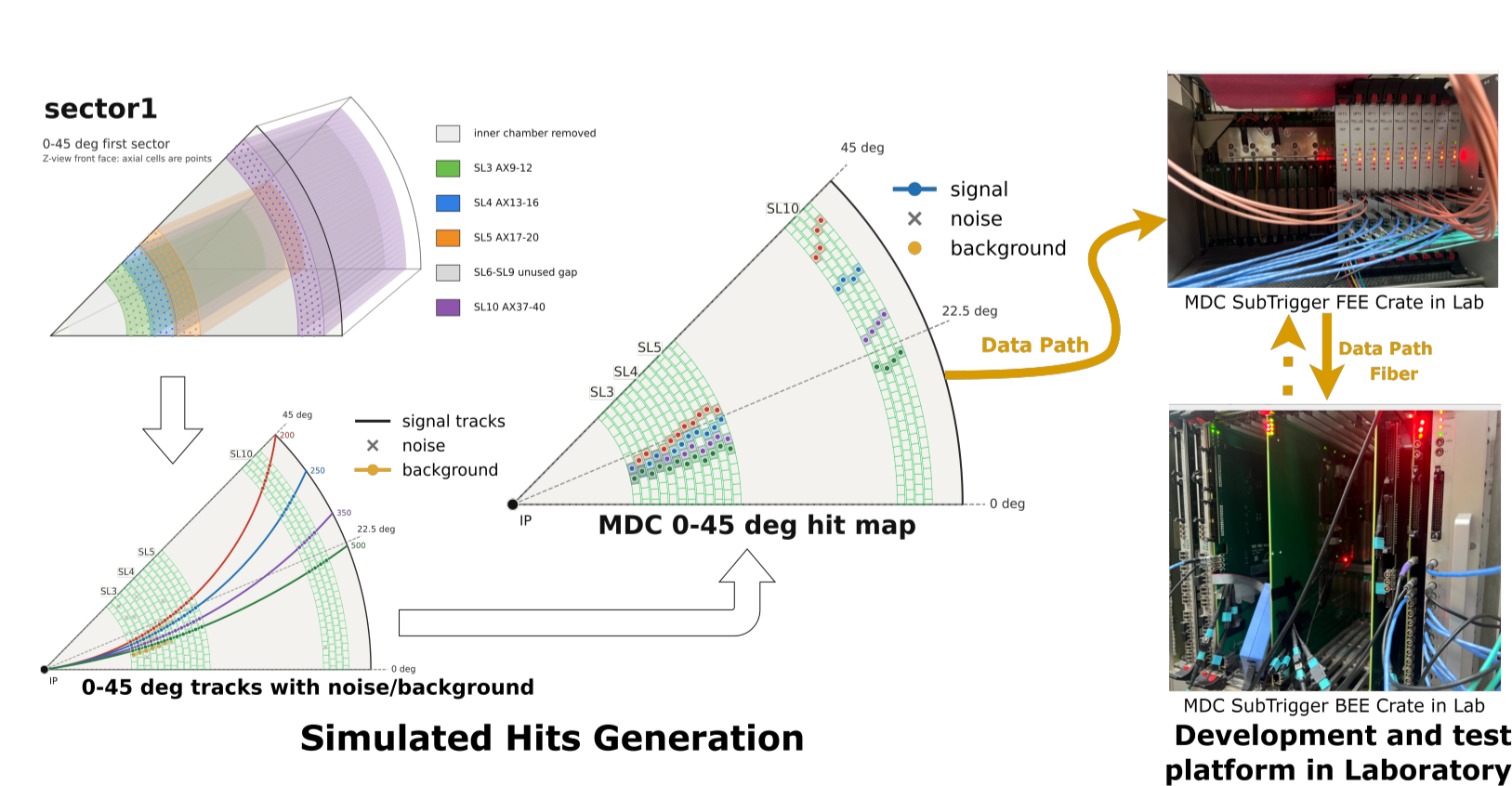


4 × 64-bit words Logical block boundaries are packed into one 256-bit AXI beat (AXI beat boundaries)

Compressed and raw frames are serialized into different numbers of 64-bit words, then packed into continuous 256-bit AXI beats without changing the original block order

Using RDMA (40G) as the data readout method. For detailed RDMA implementation and performance evaluation, please refer to **Chang Xu's poster: "No.134: FPGA based RDMA for BEE Readout"**.

## Results & Validation

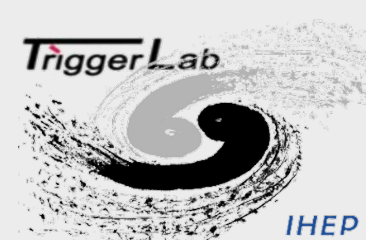


### Conclusions:

- The RDMA data were correctly filled back into the MDC hit map, the recovered hit positions and fitted tracks are consistent with the expected simulated pattern
- The recovered hit codes match the original simulated hit codes. The linear fit gives  $y = x$  and  $R^2 = 1.000000$ , showing that no hit loss or wrong decoding was observed in this test.

## Future Work & Extension

- Improve the readout control mechanism to keep full-data transmission stable under high-rate conditions
- Provide reliable MDC raw hit data for 3D track-trigger studies, helping to develop and test new trigger algorithms



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