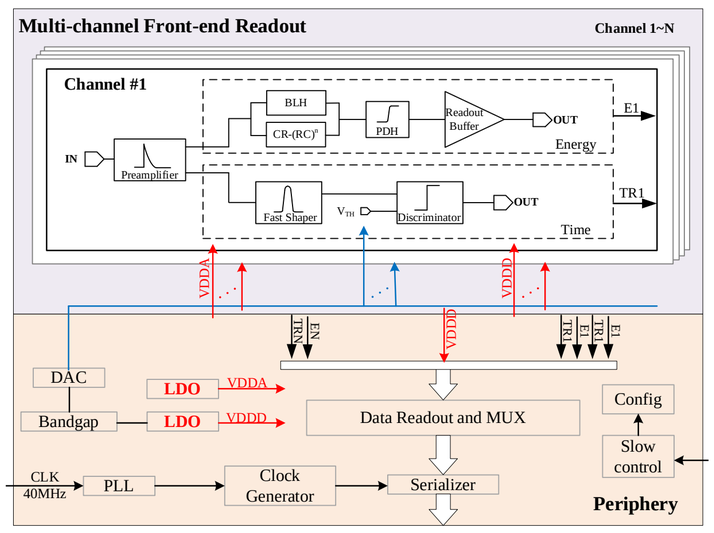
A Full on-Chip LDO Regulator with self-adapting compensation networks for Front-end Readout Circuit

Xiayu Wang[1], Jia Wang[2*], Yongcai Hu[1]

1. School of Computer Science, Northwestern Polytechnical University, Xi'an, China
2. School of Integrated Circuit and Microelectronics, Northwestern Polytechnical University, Xi'an, China

xiayuwang@mail.nwpu.edu.cn
jwang@nwpu.edu.cn

DESIGN MOTIVATION



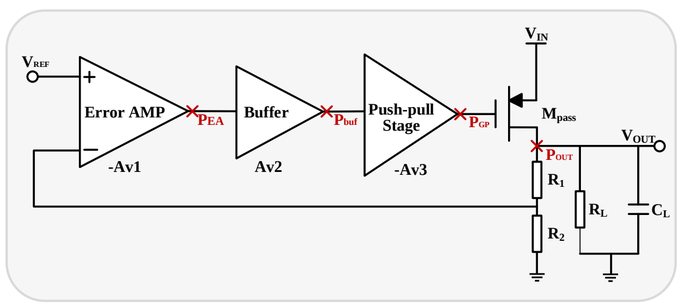
To provide a stable and clean supply voltage for front-end readout electronics, a low-dropout (LDO) regulator must meet several key requirements:

1) Capacitor-less output, which eliminates the need for a large off-chip capacitor, is advantageous for compact size.

2) Stable operation over a wide load current (I_L) range.

CIRCUIT DESIGN

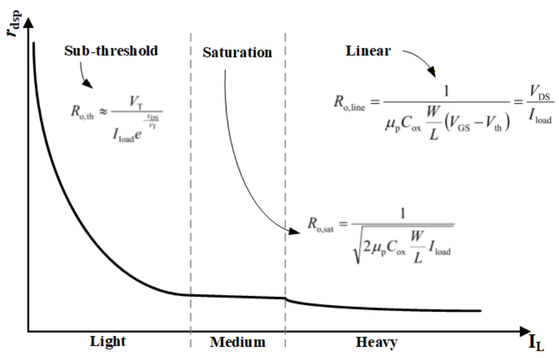
Structue of the proposed LDO

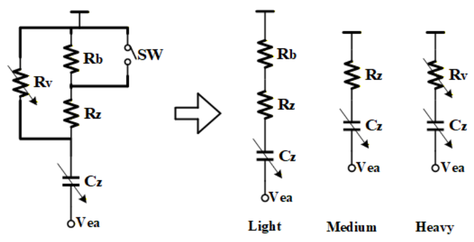


Four poles exist in the loop, with two located below the UGF that directly impact stability. The two main poles are given as:

$$P_{EA} = \frac{1}{2\pi R_{EA} C_G}$$

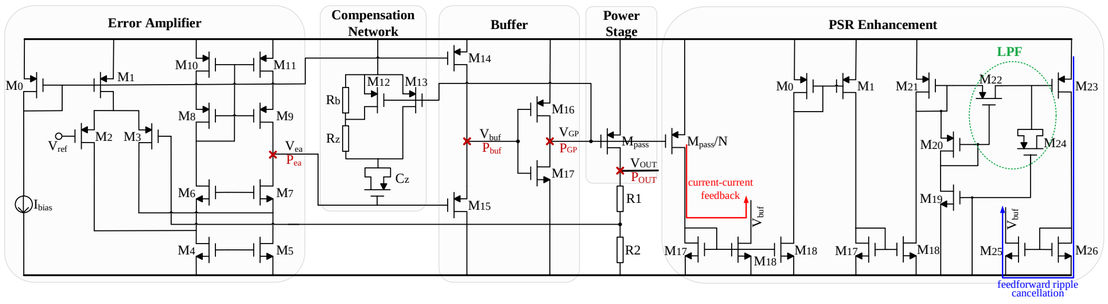
$$P_{OUT} = \frac{1}{2\pi[(R_1 + R_2) r_{o,M_p} || R_L] C_L}$$





- Since P_{OUT} varies widely with I_L, fixed zero compensation is insufficient to satisfy stability requirements across a wide I_L range.
- Depending on the MOSFET's operating region (sub-threshld, saturation and linear), the compensation circuit is configured into three corresponding topologies to track P_{OUT} better.

Circuit Implementation

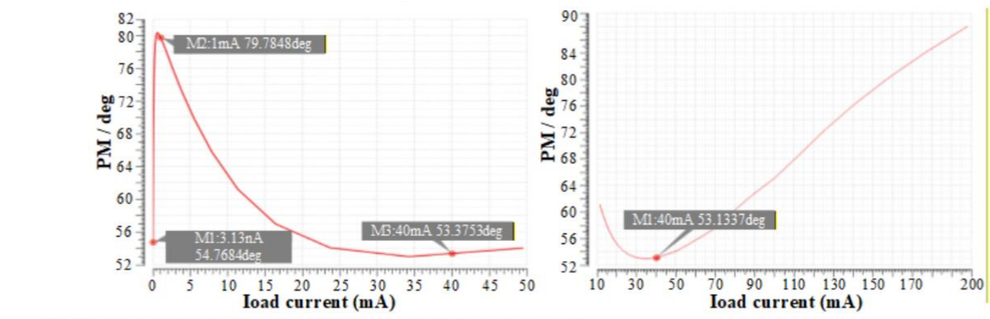


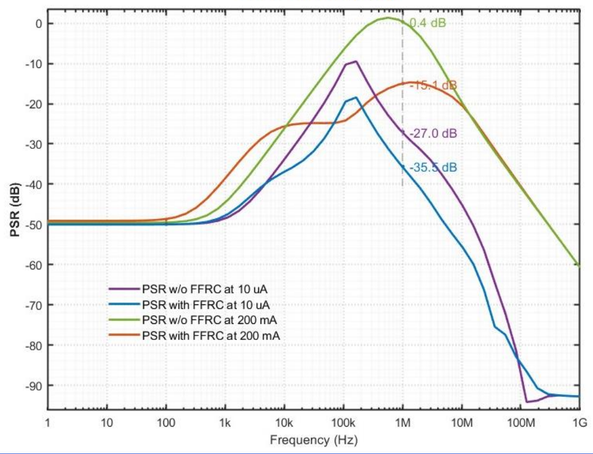
The transistor-level implementation of the proposed LDO is shown above. The inserted zero is given as:

$$Z_z = \frac{1}{C_z\{R_{M12} || [R_z + (R_{M13} || R_b)]\}}$$

It varies with P_{OUT}, ensuring sufficient phase margin over the entire I_L range. Furthermore, a feedforward ripple cancellation path is integrated to improve the mid-to-high frequency power supply rejection (PSR) of the converter. The phase margin is 65.7° at a load current of 100 mA, and 89.8° at 200 mA. The minimum observed phase margin is 53.4°,

which remains within acceptable limits.





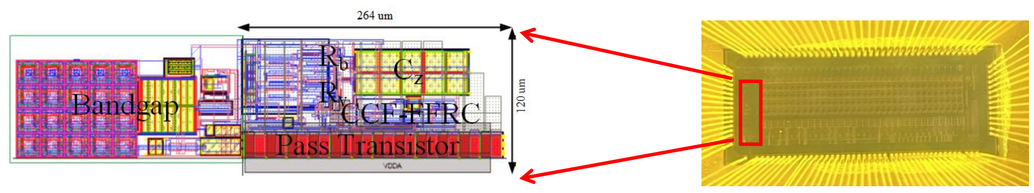
- **PSR improvement**

At a light load (10 μA), the PSR at 1 MHz improves from -27 dB to -35.5 dB, while at a heavy load (200 mA), it improves from 0 dB to -15 dB.

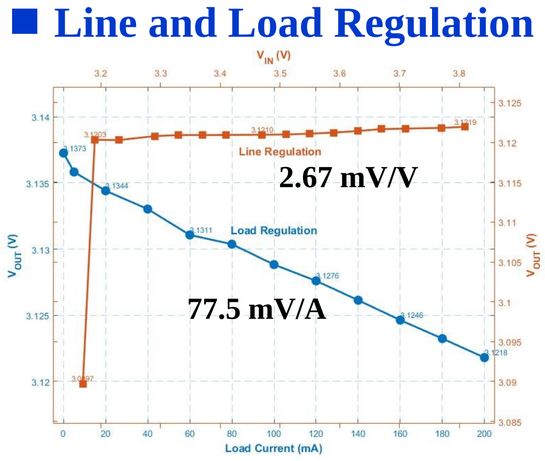
LAYOUT AND TEST RESULTS

Layout

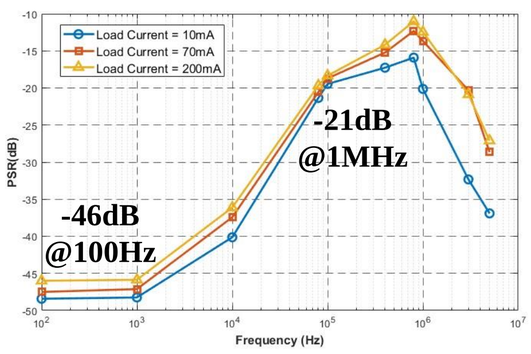
Technology: 180nm CMOS Area: 120×265 um²



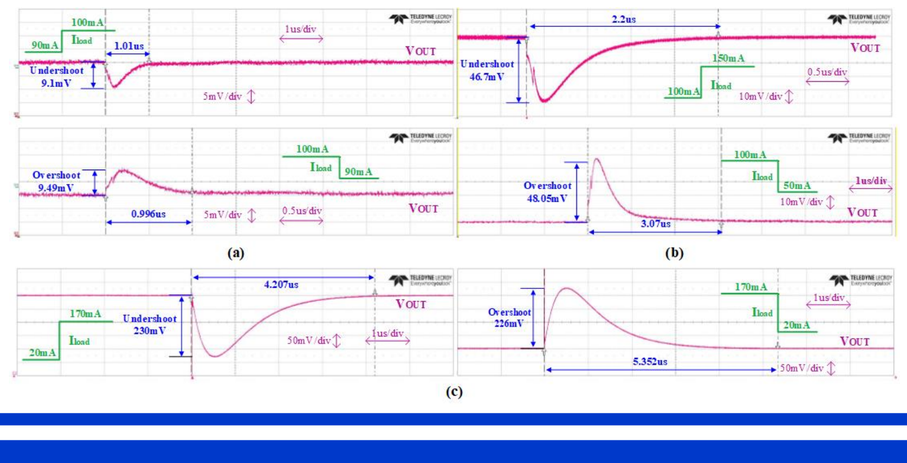
Line and Load Regulation



PSR



Load Transient Response



CONCLUSION AND COMPARISION

Table I. Performance summary and comparison with state-of-the-art designs.

	[1]	[2]	[3]	[4]	This Work
Technology (nm)	180	28	180	180	180
$I_{out,max}$ (mA)	200	10	50	200	200
Dropout Voltage (mV)	30	200	268.9	200	70
Line Regulation (mV/V)	0.346	1.71	3.484	/	4.09
Load Regulation (mV/A)	9.5	219	476	50	77.3
Undershoot ΔV_{out} (mV)@ΔI_{load} (mA)	/	50@9.8	152@50	210@190	230@150
Overshoot ΔV_{out} (mV)@ΔI_{load} (mA)	/	51@9.8	126.9@50	270@190	226@150
PSR (dB)@Frequency (Hz)	-47@100 -37@100 k	-36@1 M	-49.4@10 k -12.6@1 M	/	-48@100 -21@ 1M
Active Area(mm²)	0.18	0.012	0.17	0.148	0.0317

[1]M. Kim and S. Cho, "An Output-Capacitorless Analog LDO Featuring Frequency Compensation of Four-Stage Amplifier," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 2, pp. 642-654, Feb. 2023.
[2] J.-G. Lee and H.-S. Kim, "A Fully Integrated, Domino-Like-Buffered LDO Regulator With High Power-Supply Rejection Across the Full Frequency Spectrum," in IEEE Journal of Solid-State Circuits, vol. 59, no. 12, pp. 4088-4100, Dec. 2024.
[3] P. Li, X. Zhao, X. Zhang et al., "General Performance Enhancement for Capacitor-Less Low-Dropout Regulator Using Local Positive-Feedback Technique," in IEEE Transactions on Power Electronics, vol. 40, no. 1, pp. 1498-1507, Jan. 2025.
[4] M.-S. Kim, J.-H. Kim, S. Jeong et al., "A Wide Load Range Output Capacitor-Less LDO With Load Tracking Zero Compensation for IoT Applications," in IEEE Transactions on Industrial Electronics, vol. 73, no. 1, pp. 1499-1504, Jan. 2026.