A Multi-Mode Waveform Digitization System Based on Switched Capacitor Array Chips

Dingjun Li, Jiajun Qin, Hexiang Wang, Yuelei Ma, Kairen Chen, Zhe Cao, and Lei Zhao

***Abstract*—A configurable waveform digitization architecture based on cascaded Switched Capacitor Array (SCA) chips is proposed for detector readout applications in nuclear and particle physics experiments. To accommodate the diverse waveform digitization requirements of different detector systems, including high sampling rate, high sampling depth, and high event-processing capability, the proposed architecture configures the sampling-clock phase relationship and trigger allocation among multiple SCA chips to support three corresponding operating modes. An 8-channels prototype system incorporating two self-developed SCA ASICs was developed to validate the proposed architecture. Experimental results demonstrate an equivalent sampling rate of 10.24 Gsps through time-interleaved sampling, an effective sampling depth of 512 samples through waveform concatenation, and an event-processing capability of approximately 100 kHz through alternating trigger allocation. Joint tests with a PICOSEC Micromegas detector further verify the reliable operation of the proposed architecture in a realistic detector readout environment. The proposed architecture provides a flexible and scalable solution for high-performance waveform digitization systems.**

***Index Terms*—Readout electronics, Waveform digitization, Switched capacitor array (SCA)**

I. Introduction

THE output waveform of particle detectors contains comprehensive information about detector signals, including both timing and charge information. Conventional detector readout electronics typically rely on dedicated analog circuits to extract these quantities separately. In contrast, waveform digitization directly samples and digitizes the detector signals, preserving the complete waveform for digital signal processing and enabling more flexible and precise extraction of timing and charge information [1].

Compared with ultra-high-speed ADC-based waveform digitization solutions, SCA-based architectures provide lower power consumption, higher integration density, and higher achievable sampling rates. In SCA-based systems, high-speed waveform sampling is followed by analog-to-digital conversion using low-speed ADCs, making them a cost-effective and scalable solution for high-speed detector readout [2,3].

As a result, SCA-based waveform digitization has become a widely adopted solution for high-speed detector readout in nuclear and particle physics experiments. Representative implementations include the DRS4 developed by the Paul Scherrer Institute [4], which has been employed in experiments such as MAGIC-II [5], PADME [6], and CTA [7], and the PSEC4 developed by the LAPPD Collaboration [8], which has been applied to large-area picosecond photodetectors (LAPPD) [9] and optical time-projection chamber (OTPC) [10] systems.

Despite their widespread adoption, different detector systems impose different requirements on waveform digitization, with some applications prioritizing high sampling rates, while others emphasize sampling depth, or event-processing capability. Meeting these different requirements by developing dedicated application-specific integrated circuits (ASICs) is both costly and time-consuming. Therefore, enhancing the performance of existing SCA ASICs through system-level design provides a flexible and scalable solution that can accommodate diverse application requirements while offering higher integration than oscilloscope-based solutions.

Motivated by this system-level design approach, this paper proposes a configurable waveform digitization architecture based on cascaded SCA chips. By employing programmable sampling-clock phase control and flexible trigger management, the architecture supports multiple acquisition modes, enabling optimization for high sampling rate, high sampling depth, or high event rate according to experimental requirements. A two-chip prototype system was developed to validate the proposed architecture, demonstrating that a single hardware platform can be reconfigured to support the three acquisition modes without hardware modification.

The remainder of this paper is organized as follows. Section II introduces the proposed configurable multi-mode waveform digitization architecture and its operating principles. Section III describes the implementation of the prototype system and the key hardware modules. Section IV presents the experimental setup and evaluates the system performance under different operating modes. Finally, Section V concludes the paper.

Manuscript submitted July 6th, 2026.

This work was supported in part by the National Natural Science Foundation of China under Grant 12325509 and in part by the Youth Innovation Promotion Association Chinese Academy of Sciences (CAS).

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II. Architecture

A. Principle of the Multi-Mode Digitization Scheme

The proposed architecture is motivated by two considerations. First, the performance limitations of a single SCA chip can be overcome by coordinating multiple chips to operate collaboratively. Second, different waveform digitization objectives can be achieved by properly configuring the sampling clock relationship and trigger allocation among multiple SCA chips. Based on these principles, all operating modes share a common physical structure, in which the input signal is equally divided and simultaneously sampled by multiple SCA chips. The mode dependent behavior is determined by two configurable parameters:

(1) the relative timing of trigger signals applied to different SCA chips;

(2) the phase or delay relationship among their sampling clocks.

Through programmable control of these parameters, the architecture can be dynamically configured to operate in high sampling rate, high sampling depth, or high event rate modes without modification of the hardware structure.

B. High Sampling Rate Mode

In the high sampling rate mode, multiple SCA chips operate in a time-interleaved manner. A configurable clock distribution circuit generates phase-shifted reference clocks whose phase offsets are selected such that the sampling clocks of adjacent SCA chips are separated by T_s/N, where T_s is the sampling period of a single SCA chip and N is the number of cascaded chips. Consequently, the sampling points of different chips are uniformly distributed within one sampling period, forming an interleaved sampling sequence with an equivalent sampling interval of T_s/N. This architecture allows an effective sampling rate N times higher than that of a single SCA chip. To ensure proper waveform reconstruction, all SCA chips receive the same trigger signal and terminate sampling simultaneously.

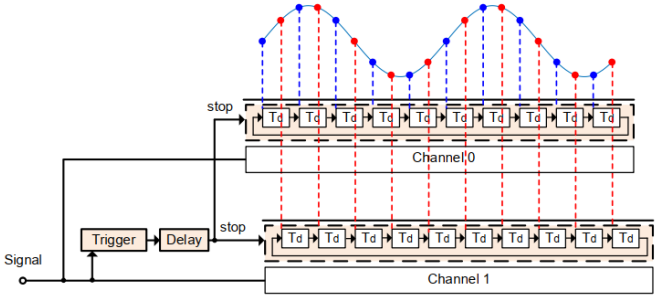

Fig. 1. Principle of the high sampling rate mode.

C. High Sampling Depth Mode

In the high sampling depth mode, all SCA chips operate with in-phase sampling clocks, while their trigger signals are applied sequentially. The trigger signal for each successive chip is delayed by one complete sampling window relative to the previous chip, causing different chips to record consecutive portions of the input waveform. Since all chips sample at the same rate and share a common time base, the acquired waveform segments can be directly concatenated to reconstruct a longer continuous waveform. Consequently, the effective sampling depth is extended to N times that of a single SCA chip without affecting the sampling rate.

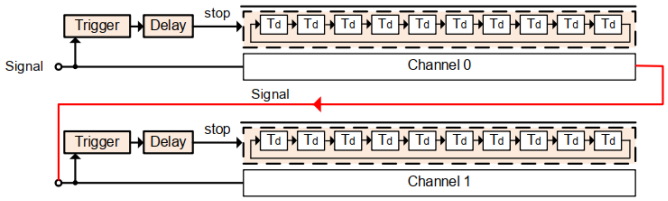

Fig. 2. Principle of the high sampling depth mode.

D. High Event Rate Mode

In the high event rate mode, all SCA chips operate with in-phase sampling clocks, while trigger events are distributed alternately among different chips. For each trigger event, only one SCA chip terminates sampling and proceeds to waveform digitization and readout, whereas the remaining chips continue sampling and remain ready to capture subsequent events. By alternating trigger allocation among multiple SCA chips, waveform acquisition and data readout can be performed in parallel. As a result, the dead time imposed by the readout process of a single SCA chip is significantly reduced, leading to a significant improvement in the overall event-processing capability of the architecture.

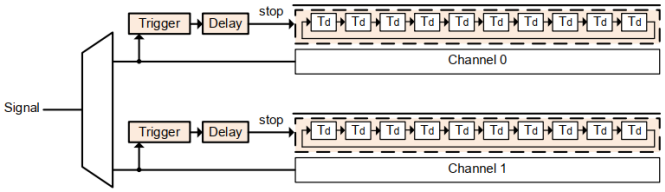

Fig. 3. Principle of the high event rate mode.

E. Comparison of Operating Modes

TABLE I
COMPARISON OF OPERATION MODES

Mode	Sample Clock	Trigger
High sampling rate	Phase offset of Ts/N	Synchronous
High sampling depth	Synchronous	Sequentially delayed
High event rate	Synchronous	Alternately allocated

III. Hardware Implementation

A. System Overview

To validate the proposed configurable multi-mode waveform digitization architecture, a prototype system based on two cascaded SCA chips was developed, as shown in Fig. 4. The system consists of a power splitter network, analog signal conditioning circuits, two self-developed SCA ASICs, a programmable clock-generation circuit, FPGA-based trigger and control logic, and a DAQ interface.

The eight analog input channels are first processed by the analog front-end, which comprises the power splitter network and analog signal conditioning circuits, and are then simultaneously sampled by the two SCA ASICs. Meanwhile,

the analog signal conditioning circuits incorporate discriminator circuits that generate sixteen hit signals upon the arrival of detector pulses. These hit signals are transmitted to the FPGA for trigger generation.

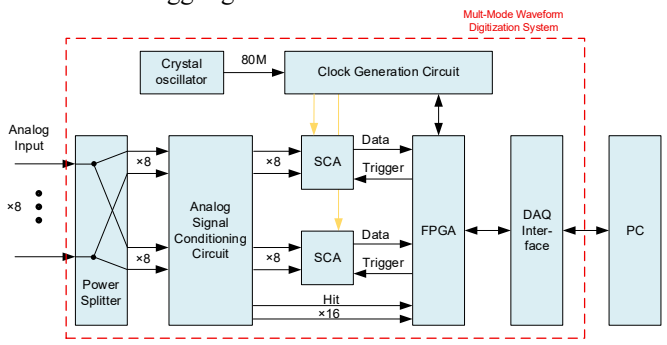

Fig. 4. Hardware block diagram.

The programmable clock-generation circuit, driven by an 80 MHz crystal oscillator, provides configurable reference clocks for the SCA ASICs. Under FPGA control, the clock generator is configured according to the selected operating mode, while the FPGA performs trigger generation and allocation, acquisition control, and system configuration as described in Section II.

After waveform digitization, the acquired data are transferred from the SCA ASICs to the FPGA and subsequently transmitted to the host computer through the DAQ interface for waveform reconstruction and further analysis.

B. Self-Developed SCA ASIC Specifications

TABLE II
SPECIFICATION OF THE SELF-DEVELOPED SCA ASIC

Function	Parameter
Technology (nm)	180
Channels	8
Sampling depth	256
Sampling rate (Gsps)	<1-5.12
Input Range (V)	1.2
Noise (mV)	0.7
On-chip ADC	Yes
ADC resolution (bit)	12
Best timing precision (RMS, ps)	< 4
Power consumption (mW)	200

The waveform acquisition function is implemented using two self-developed SCA ASICs. Each ASIC supports a programmable sampling rate from 1 to 5.12 Gsps and provides an analog input bandwidth of 470 MHz. The analog input stage has an input capacitance of 12 pF, accommodates a maximum input signal swing of 1.2 V, and exhibits an intrinsic noise of approximately 1 mV. The sampling clock is internally generated by multiplying the external reference clock by a factor of 256, enabling flexible control of the sampling phase through reference-clock adjustment. Each ASIC integrates eight input channels with 256 sampling cells per channel. Due to the increased tracking error associated with the boundary sampling cells, several edge samples are discarded during waveform reconstruction, resulting in an effective sampling depth of 248 samples per channel. The ASIC further integrates on-chip analog-to-digital conversion and exhibits a dead time of 19.685 μs, corresponding to a maximum event-processing rate of approximately 50.8 kHz [11].

C. Power Splitter Selection

To ensure consistent waveform acquisition among multiple SCA chips, the signal distribution network should provide sufficient bandwidth and good amplitude matching between output channels. Therefore, a wideband passive power splitter (SBTC-2-10X+, Mini-Circuits) was selected. The device provides an operating bandwidth from 5 MHz to 1000 MHz, which exceeds the 470 MHz analog input bandwidth of the SCA ASIC. To evaluate its suitability, the manufacturer-provided S-parameter model was simulated using Keysight ADS and the corresponding simulated insertion-loss results are shown in Fig. 5. The insertion losses of the two output ports remain approximately 3.3 dB with good agreement over the frequency range of interest, indicating adequate amplitude matching for the proposed waveform digitization system.

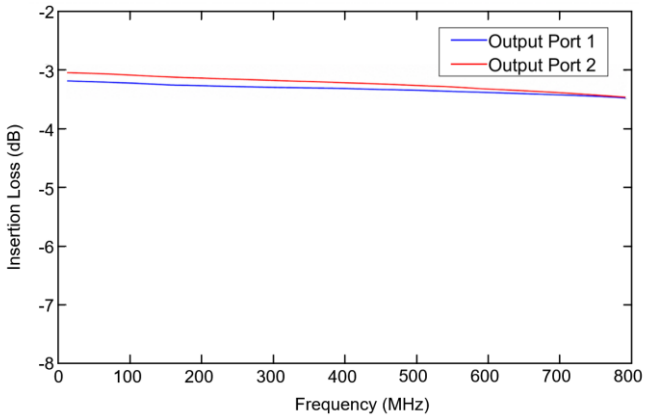

Fig. 5. Simulated insertion losses of the two output ports.

D. Analog Front-End Amplifier Design

The analog front-end amplifier should provide sufficient bandwidth, drive capability, and low noise to satisfy the requirements of high-speed waveform acquisition. To avoid limiting the system bandwidth, the amplifier bandwidth was required to exceed 500 MHz. Based on the maximum input signal swing of 1.2 V, the minimum slew-rate requirement was estimated to be approximately 2260 V/μs. In addition, considering the 12 pF input capacitance of the SCA ASIC and the maximum sampling rate of 5.12 Gsps, the required output drive current was calculated to be approximately 90 mA.

Noise performance was also considered during device selection. Assuming white-noise-dominated behavior within the operating bandwidth and targeting an amplifier noise contribution significantly lower than the intrinsic noise of the SCA ASIC ($\approx$1 mV), the input-referred voltage noise density was required to be below approximately 3.6 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

Based on these considerations, the THS4508 fully differential amplifier from Texas Instruments was selected. The device provides a slew rate of 6400 V/μs, an output drive

current of 96 mA, and an input voltage noise density of 2.3 $nV/\sqrt{Hz}$, satisfying the design requirements. The simulated frequency response obtained using Keysight ADS is shown in Fig. 6. The amplifier exhibits a −3 dB bandwidth of approximately 610 MHz, which is sufficient for the proposed waveform digitization system.

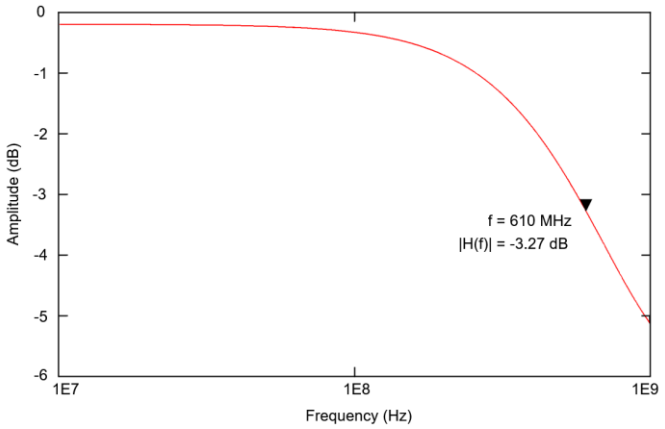

Fig. 6. Simulated small-signal frequency response.

E. Programmable Clock Generation Circuit

To support the high sampling rate mode, the clock generation circuit must provide reference clocks with programmable phase relationships for multiple SCA chips. Since each SCA ASIC internally generates its sampling clock by multiplying the external reference clock by a factor of 256, the relative phase between the reference clocks directly determines the phase relationship of the sampling clocks. Therefore, time-interleaved sampling can be realized by adjusting the relative phase of the reference clocks supplied to different SCA chips.

The clock generation circuit, shown in Fig. 7, is implemented using an LMK04832 clock synthesizer with programmable output-clock delay. An 80 MHz crystal oscillator serves as the system clock source, while the LMK04832 generates two independent 20 MHz reference clocks for the SCA ASICs. The relative delay between the two reference clocks is configured by the FPGA through the SPI interface, allowing flexible phase adjustment without any hardware modification.

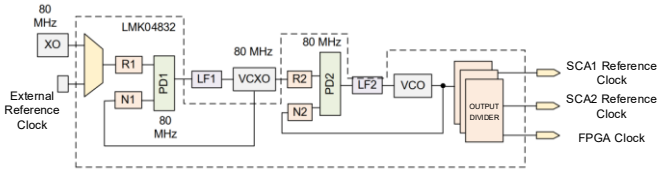

Fig. 7. Hardware implementation of the programmable clock generation circuit.

For the prototype system, each SCA ASIC operates at a sampling rate of 5.12 Gsps. To realize two-chip time-interleaved sampling, the two sampling clocks are required to maintain a phase difference of one-half of the sampling period (97.656 ps). This phase relationship is established by introducing an appropriate delay between the two reference clocks. As illustrated in Fig. 8, only the sampling-clock phase modulo one sampling period affects the interleaving relationship. Therefore, the reference-clock delay is not required to be exactly 97.656 ps. Any delay satisfying

$$\Delta t = \frac{T_s}{2} + kT_s \quad (1)$$

where T_s is the sampling period of a single SCA chip and k is an integer, produces the same sampling-clock phase relationship after clock multiplication. This equivalent-delay characteristic significantly relaxes the implementation constraints of the clock generation circuit, since multiple reference-clock delays correspond to the desired interleaving phase.

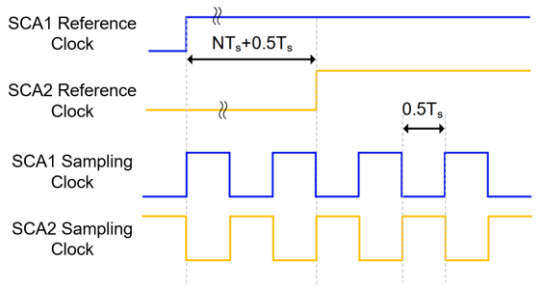

Fig. 8. Relationship between reference-clock delay and sampling-clock phase in two-chip time-interleaved sampling.

The LMK04832 realizes this phase adjustment by digitally delaying its output clocks with a resolution of one VCO period. In the high sampling rate mode, the internal VCO operates at 3.04 GHz and is divided by 152 to generate the 20 MHz reference clocks. The frequency ratio between the VCO clock and the SCA sampling clock is therefore 19:32, where the two numbers are coprime. Consequently, delaying the reference clock by successive VCO periods produces 19 uniformly distributed equivalent sampling-clock phase positions within one sampling period. By programming the output delay from 0 to 18 VCO cycles, the sampling-clock phase can be adjusted with an equivalent resolution of approximately 10.28 ps. As a result, the desired interleaving phase can be obtained by selecting the closest equivalent phase position among the 19 available delay settings.

F. FPGA Logic Architecture and Trigger Allocation

The FPGA logic architecture of the proposed system is illustrated in Fig. 9. In addition to system control, the FPGA implements waveform acquisition control, trigger generation and allocation, data reception and processing, data framing, and high-speed data transmission to the DAQ interface. Among these functions, the trigger generation and allocation logic is the key component enabling the configurable multi-mode operation of the proposed architecture.

As shown in Fig. 9, the sixteen analog input channels are first processed by discriminator circuits, whose threshold voltages are configured by a DAC under FPGA control. When the input signal exceeds the preset threshold, the corresponding discriminator generates a hit signal. After entering the FPGA, the hit signals are first pulse-stretched and synchronized to the system clock domain. They are then passed through a programmable delay stage to ensure that sufficient waveform samples have been acquired before the corresponding SCA chip is stopped.

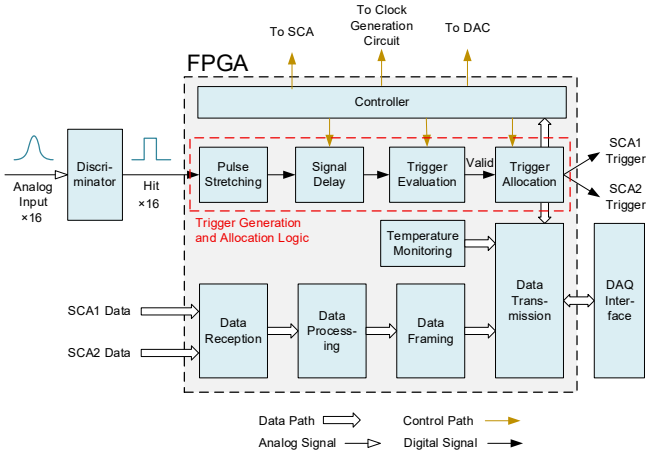

Fig. 9. FPGA logic architecture of the proposed waveform digitization system.

The delayed hit signals are subsequently processed by the trigger evaluation logic, which determines whether the configured trigger conditions are satisfied. When a valid trigger condition is met, a valid signal is generated. In addition, the trigger evaluation logic supports software-controlled generation of the valid signal, providing a manual trigger mechanism for system debugging and calibration.

The generated valid signal is finally delivered to the trigger-allocation logic, which distributes trigger signals to the two SCA chips according to the selected operating mode. The timing relationships corresponding to the three operating modes are illustrated in Fig. 10.

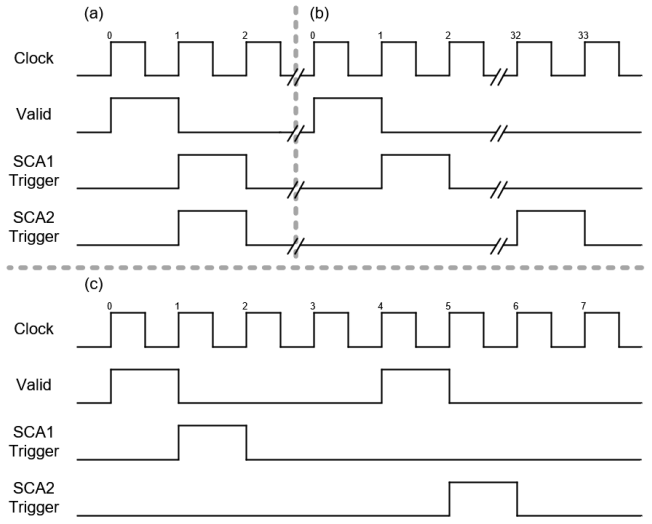

Fig. 10. Trigger timing diagrams for the three operating modes: (a) high sampling rate mode, (b) high sampling depth mode, and (c) high event rate mode.

Fig. 10(a) illustrates the high sampling rate mode, in which both SCA chips simultaneously sample the same input signal with different sampling-clock phases. Therefore, the FPGA issues trigger signals to both SCA chips simultaneously, ensuring that the two acquired waveforms correspond to the same detector event.

Fig. 10(b) illustrates the high sampling depth mode, in which the trigger signal applied to the second SCA chip is delayed by one complete sampling window relative to the first trigger, allowing the two SCA chips to acquire consecutive portions of the input waveform. At a sampling rate of 5.12 Gsps, the effective sampling depth of each SCA chip is 248 samples, corresponding to a sampling window of 48.4375 ns. The trigger delay is generated by a binary counter driven by a 640 MHz clock derived from the same clock source as the SCA reference clock. Consequently, the second trigger is generated 31 clock cycles after the first trigger, enabling seamless concatenation of the waveforms acquired by the two SCA chips.

Fig. 10(c) illustrates the high event rate mode, in which the FPGA alternately allocates trigger signals to the two SCA chips. After a valid trigger event is generated, a trigger is first issued to one SCA chip and an internal state flag is toggled. Upon the next valid trigger event, the FPGA generates a trigger for the other SCA chip and toggles the state flag back. By alternating trigger allocation in this manner, one SCA chip remains available for waveform acquisition while the other performs analog-to-digital conversion and data readout, thereby reducing the system dead time and increasing the maximum event-processing rate.

IV. Performance Evaluation

A. Experimental Setup

The test platform is illustrated in Fig. 11. An RF signal generator was used to generate high purity sinusoidal signals, while an arbitrary waveform generator provided pulse signals for waveform acquisition measurements. A high bandwidth digital oscilloscope served as a reference instrument for waveform verification. All experiments were conducted under laboratory conditions.

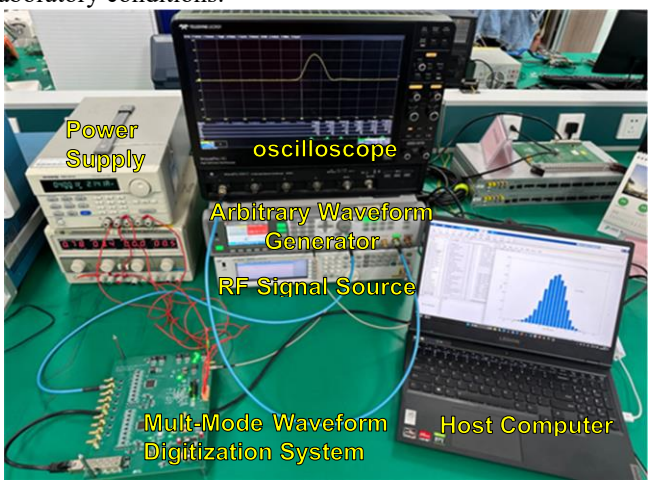

Fig. 11. Experimental platform.

B. System Calibration and Functional Verification

Before evaluating the operating modes of the proposed dual-chip architecture, the waveform acquisition performance of a single SCA acquisition channel in the prototype system was first calibrated and verified to establish the baseline performance of the hardware. The amplitude responses and sampling time intervals of all sampling cells were calibrated to compensate for process-induced mismatches among the sampling cells [11,12]. The resulting calibration parameters

were subsequently applied during waveform reconstruction to improve the timing and amplitude accuracy of the acquired waveforms.

After calibration, the basic waveform acquisition capability of the prototype was verified under single-chip operation. A high-purity sinusoidal signal was sampled at 5.12 Gsps, and Fig. 12 compares the reconstructed waveform with that measured by a high-bandwidth digital oscilloscope. Excellent agreement is observed between the two waveforms, demonstrating the correctness of the calibration procedure and the waveform reconstruction algorithm.

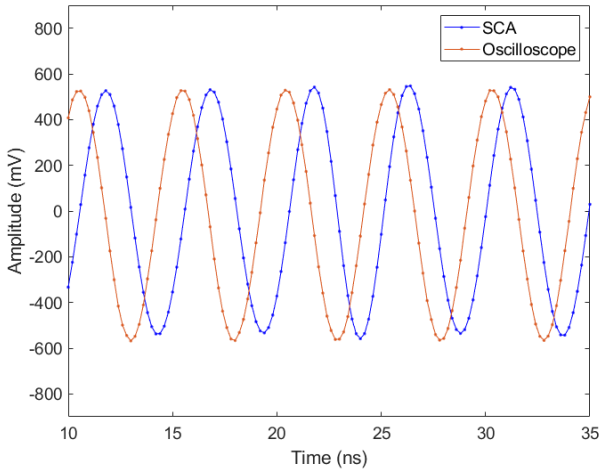

Fig. 12. Comparison of the reconstructed sinusoidal waveform and the oscilloscope measurement.

The analog bandwidth of the prototype was further characterized by sweeping the input sinusoidal frequency from 10 MHz to 640 MHz. For each frequency, the reconstructed waveform amplitude was extracted to obtain the frequency response shown in Fig. 13. The measured −3 dB bandwidth is approximately 540 MHz, which agrees well with the design target and confirms the bandwidth performance of the single-chip analog front-end.

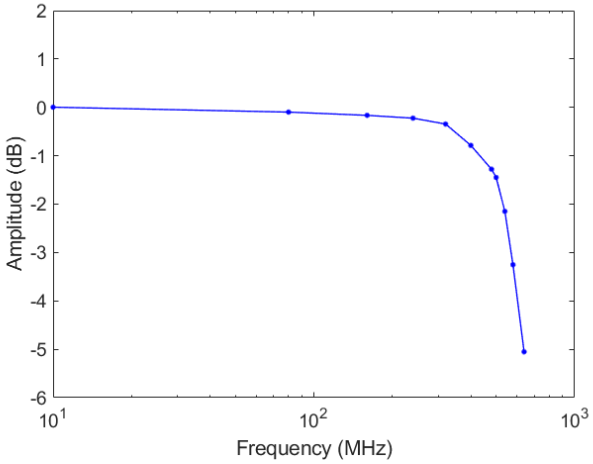

Fig. 13. Measured frequency response of the waveform digitization system.

C. High Sampling Rate Mode

In the high sampling rate mode, each SCA channel operated at 5.12 Gsps. A 300 MHz sinusoidal signal was used as the input waveform for evaluation. The sampled data from the two SCA chips were reordered according to the time-interleaving scheme described in Section II, forming a reconstructed waveform with an effective sampling rate of 10.24 Gsps. The reconstruction result is shown in Fig. 14, demonstrating correct operation of the proposed time-interleaved sampling architecture.

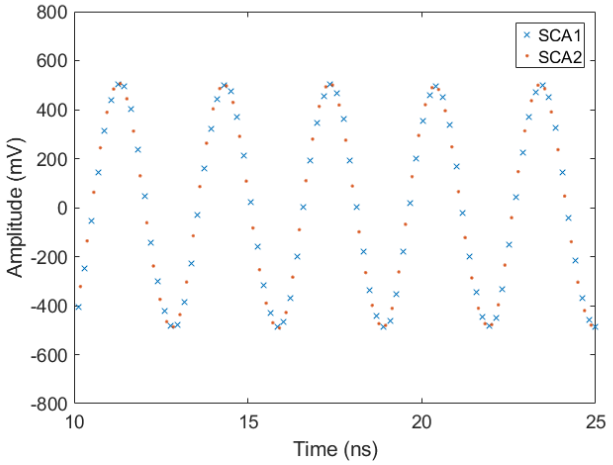

Fig. 14. Reconstructed waveform in high sampling rate mode.

D. High Sampling Depth Mode

In the high sampling depth mode, the effective sampling depth was increased by cascading two SCA chips. A 202 MHz sinusoidal signal was applied to the system, and the reconstructed waveform is shown in Fig. 15. The sampling depth was extended from 256 samples to 512 samples, corresponding to a continuous sampling window of approximately 99.2 ns at 5 Gsps, which is consistent with the design target.

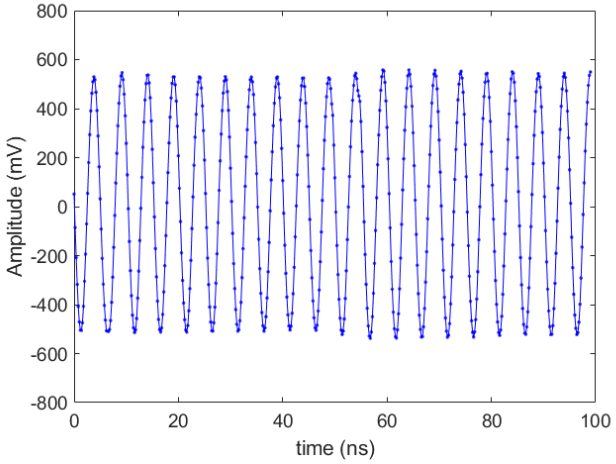

Fig. 15. Reconstructed waveform in high sampling depth mode.

E. High Event Rate Mode

In the high event rate mode, since waveform acquisition and data readout are alternately assigned to two SCA chips, the effective dead time of the system is reduced to approximately half that of a single chip. Given the measured dead time of 19.685 μs for one SCA chip, the maximum achievable event-processing rate is increased from 50.8 kHz to 101.6 kHz. To verify the capability of processing successive events, two pulses separated by 100 ns were applied to the input. The sampling

result shown in Fig. 16 confirms that both pulses can be correctly acquired and reconstructed.

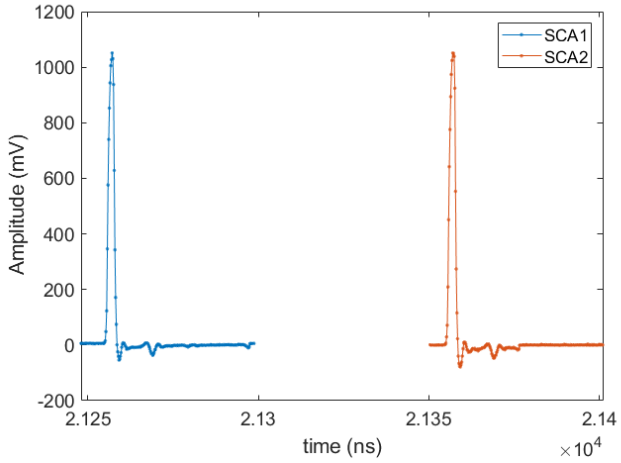

Fig. 16. Sampling result for two pulses separated by 100 ns in high event rate mode.

To verify stable operation at the target event rate, a 100 kHz periodic pulse train was continuously applied to the system input. The arrival time of each pulse was extracted from the reconstructed waveforms, and the intervals between consecutive pulses were calculated. Fig.17 presents the measured pulse-to-pulse intervals as a function of event number. The measured intervals remain centered around to the expected 10 μs period throughout the acquisition, indicating reliable event capture without event loss at 100 kHz.

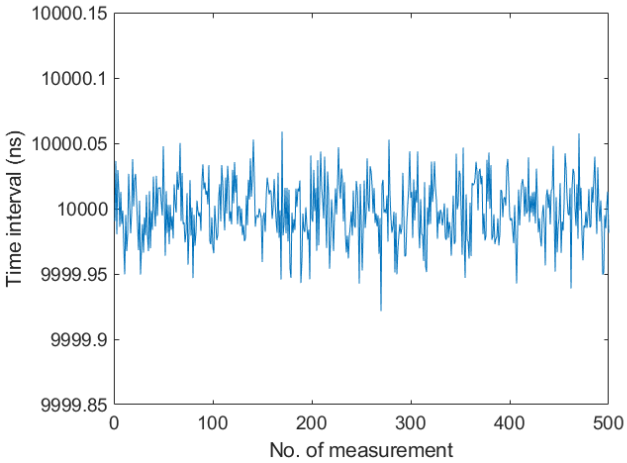

Fig. 17. Measured intervals between consecutive pulses for a 100 kHz periodic pulse train.

F. Detector Test with PICOSEC Micromegas detector

To further validate the proposed waveform digitization architecture under realistic experimental conditions, a joint test was carried out with a PICOSEC Micromegas detector. The PICOSEC Micromegas detector is designed for ultra-fast timing applications and produces detector signals with sub-nanosecond leading edges [13], making it well suited for evaluating the high sampling rate mode of the proposed architecture. The experimental setup is shown in Fig. 18(a), where the proposed prototype was integrated into the detector readout system and operated at an equivalent sampling rate of 10.24 Gsps. Figure 18(b) compares the original waveform acquired by a single SCA ASIC with the waveform reconstructed using two-chip time-interleaved sampling. Compared with the original waveform, the time-interleaved waveform provides approximately twice the sampling density while preserving the waveform shape and continuity, with no observable discontinuities at the stitching boundary between the two SCA ASICs. These results demonstrate the effectiveness of the proposed high sampling rate architecture for fast detector signal acquisition.

(a)

(b)

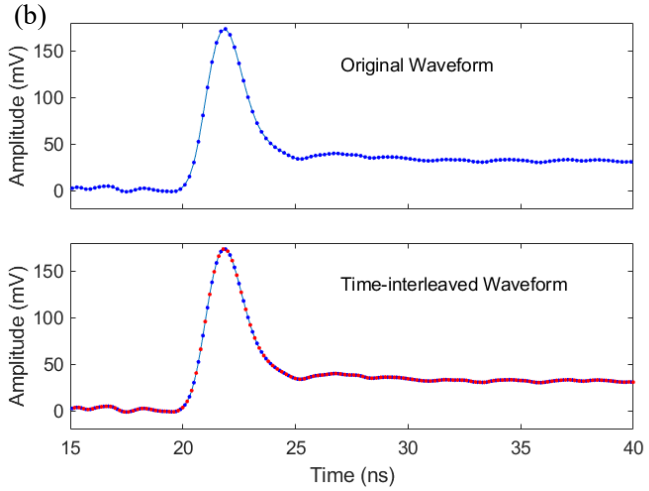

Fig. 18. PICOSEC Micromegas detector joint test: (a) experimental setup; (b) comparison of the original waveform and the time-interleaved waveform.

V. Conclusion

A configurable multi-mode waveform digitization architecture based on cascaded switched capacitor array (SCA) ASICs has been proposed and experimentally demonstrated. By configuring the sampling-clock phase relationship and trigger allocation among multiple SCA chips, the proposed architecture supports high sampling rate, high sampling depth, and high event rate acquisition within a unified hardware architecture. Unlike conventional SCA-based waveform digitizers that are typically optimized for a single acquisition objective, the proposed architecture can be dynamically adapted to different experimental requirements through programmable clock and

trigger configuration.

A two-chip prototype was implemented to validate the proposed concept. Experimental results demonstrate an equivalent sampling rate of 10.24 Gsps, a continuous sampling window of approximately 100 ns, and an event-processing capability of approximately 100 kHz. Joint tests with a PICOSEC Micromegas detector further verified the applicability of the proposed architecture in a realistic detector readout environment. The proposed architecture provides a flexible and scalable solution for future high-performance waveform digitization systems in nuclear and particle physics experiments.

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