A Multi-Mode Waveform Digitization System Based on Switched Capacitor Array Chips

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Abstract——Waveform digitization directly samples detector analog signals and extracts timing and amplitude information via digital signal processing, and is widely used in readout electronics for nuclear and particle physics experiments. Switched Capacitor Array (SCA) architectures combine high-speed analog sampling with low-speed analog-to-digital converters (ADCs), offering advantages in power consumption, integration level, and achievable sampling rate compared with ultra-high-speed ADC-based solutions.
This work proposes a configurable waveform digitization architecture based on cascading multiple in-house developed SCA chips. For a two-chip configuration, the input signal is equally split by a wideband passive power divider and fed into two SCA chips. A phase-locked loop (PLL) controls the sampling clock phases, while FPGA-based trigger logic enables multiple operating modes. Time-interleaved sampling with a 180° phase offset achieves high sampling rates, waveform concatenation extends sampling depth, and alternating trigger allocation improves event rate.
Based on this concept, a multi-mode waveform digitization prototype was designed and implemented. Laboratory measurements demonstrate sampling rates of up to 10 Gsps, a continuous sampling window of approximately 100 ns, and an event processing capability of about 100 kHz. Further joint tests with a Picosecond Micromegas detector validate a 10 Gsps effective sampling rate and achieve a timing resolution better than 26 ps in cross-chip operation.

Overview of the system

The proposed configurable multi-mode waveform digitization system supports three operation modes: high sampling rate, high depth, and high event rate. As shown in Fig. 1, the system cascades multiple Switched Capacitor Array (SCA) chips and enables mode reconfiguration via programmable clock phase control and trigger timing, without hardware changes. In Fig. 1, the input analog signal is equally split by a wideband passive power divider, then conditioned by single-ended-to-differential conversion to meet SCA input requirements. The conditioned signals are sampled and stored by two SCA chips. Upon trigger arrival, sampling stops, the stored analog samples are digitized, and the data are transferred in time order to the digital back-end for waveform reconstruction and analysis.

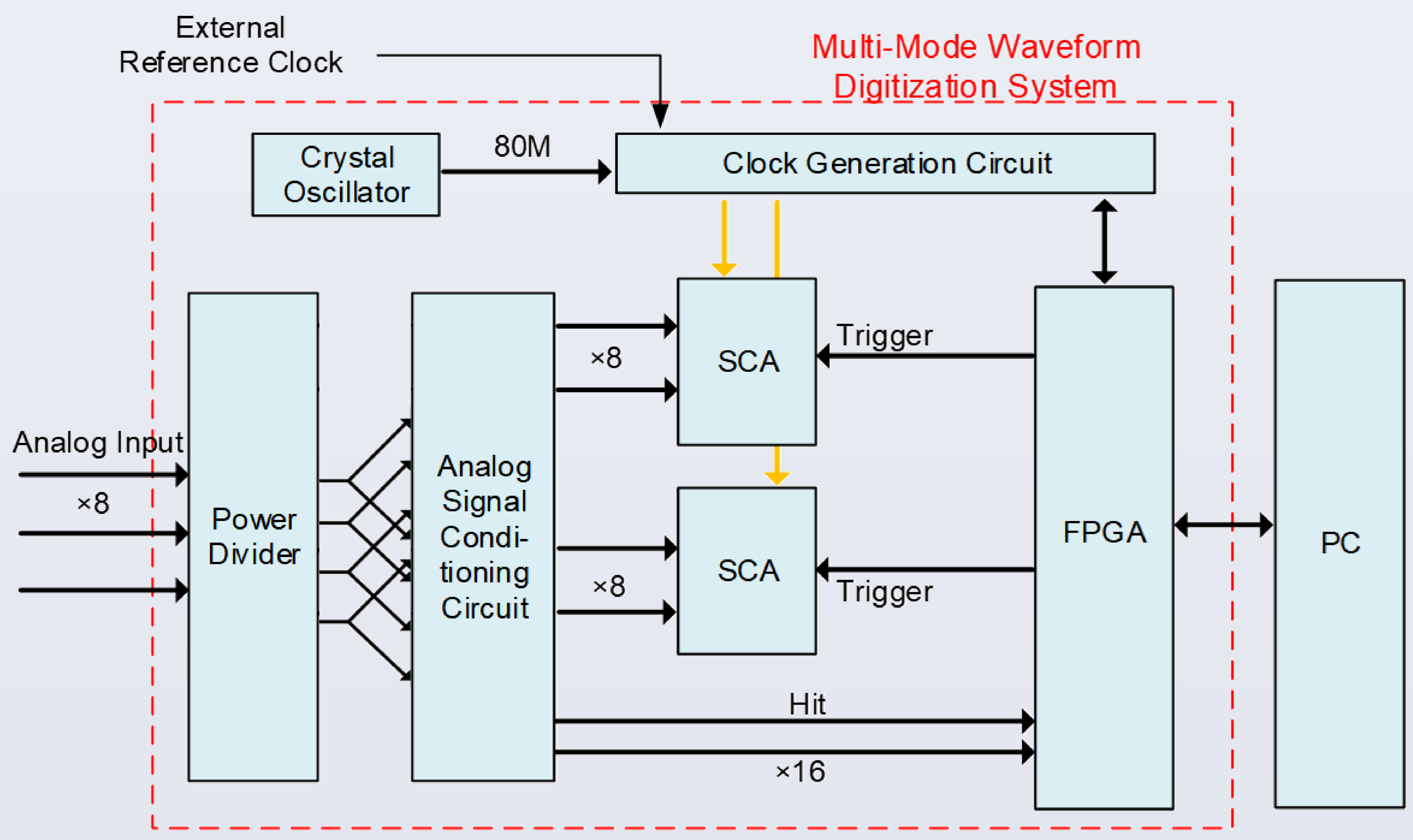

Fig. 1 Overall system block diagram

Multi-mode digitization scheme

By configuring the sampling clock phase and trigger timing, multiple functional modes can be realized without modifying hardware structure.

- **High sampling rate mode**: Two sampling clocks with 180° phase offset enable time-interleaved sampling, halving the effective sampling period and doubling the equivalent rate. Both sampling chains stop simultaneously upon trigger.
- **High sampling depth mode**: Two SCAs use in-phase sampling clocks, with the second SCA's trigger delayed by one full sampling window relative to the first. The sequentially sampled waveforms are time-concatenated, doubling the sampling depth.
- **High event rate mode**: SCAs operate with in-phase clocks, but triggers are alternately assigned. When one SCA is busy with readout, the other remains available for sampling, reducing dead time and improving event throughput.

Mode	Sample clock	Trigger
High sampling rate	180° phase offset	synchronous
High sampling depth	synchronous	delay of SCA sampling time
High event rate	synchronous	alternate

Table 1 Sampling clock phase and trigger timing in three functional modes

Test Results

- **High sampling rate mode**: two SCA channels are time-interleaved to achieve an effective sampling rate of 10.24 Gsps.
- **High event rate mode**: two input pulses with a time difference of 100 ns were successfully processed.
- **High sampling depth mode**: cascading two SCA channels yields a record length of 99.2 ns at 5 Gsps.
- **The joint test with the MRPC detector** shows that the time measurement precision of the electronics and detector system reaches 24.7 ps.

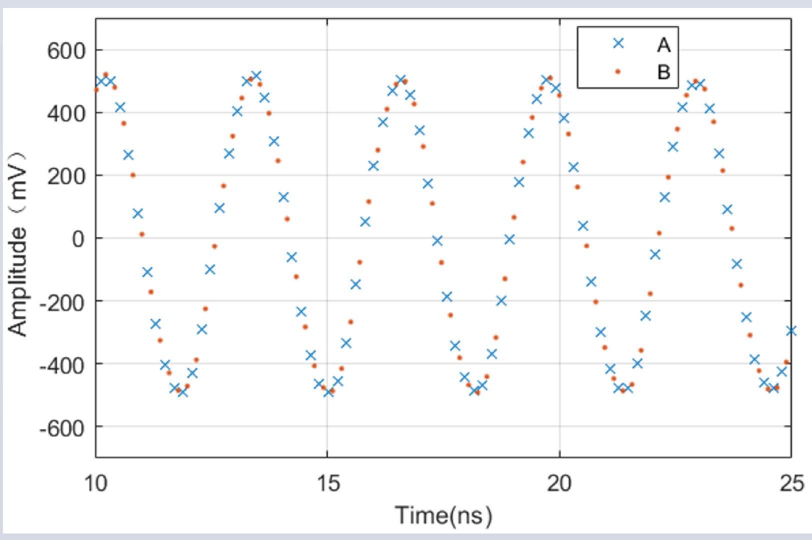

Fig. 2 Two-channel time-interleaved reconstructed waveform

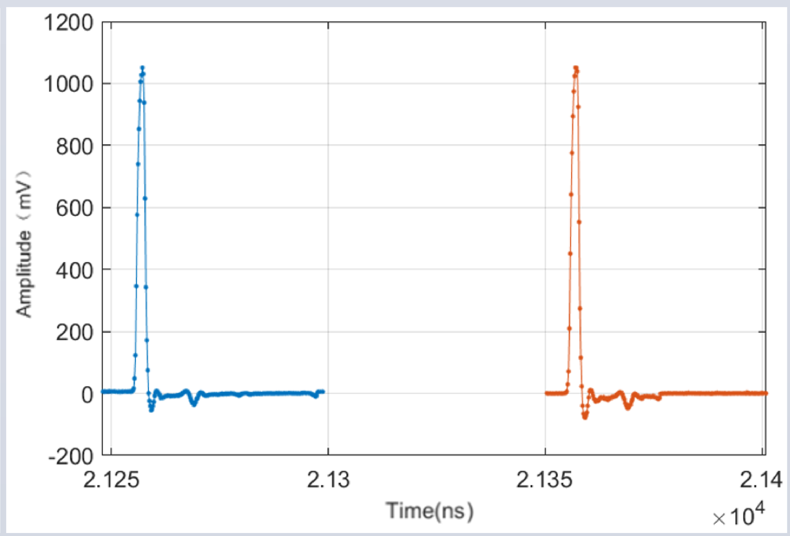

Fig. 3 Sampling results for two pulses separated by 100 ns

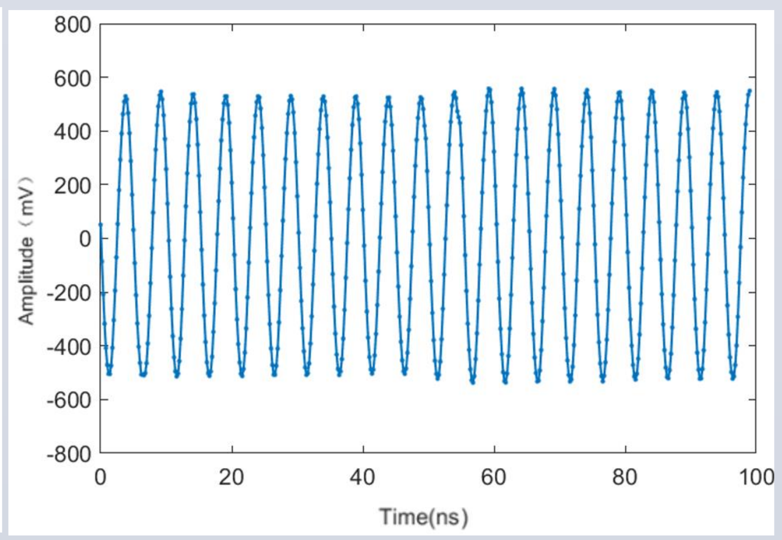

Fig. 4 Wave form sampling results of a 202 MHz sinusoidal signal

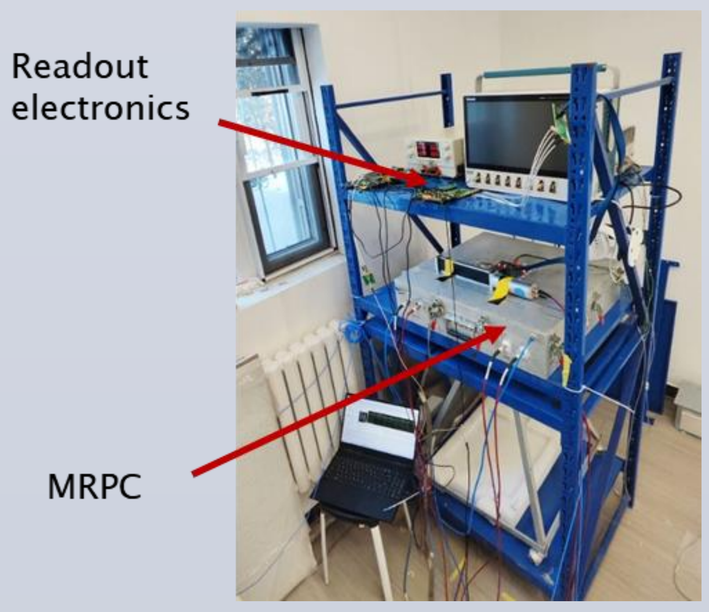

Fig. 5 Test platform with MRPC detector

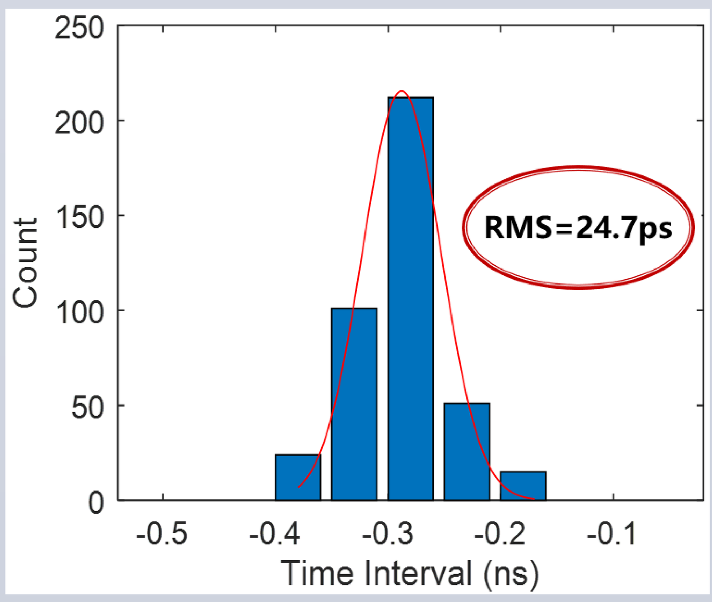

Fig. 6 Electronics-detector time measurement precision

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