Design of Transmission Cable Delay Calibration Method for Large-Scale Electron Accelerators

Haoqian Xu, Ziliang Qi, Junzhi Cheng, Zhe Cao, Jiajun Qin, Kairen Chen, Lei Zhao

***Abstract*—Beam position monitors (BPMs) are widely used in large-scale accelerator facilities for beam diagnostics and feedback control, including beam orbit monitoring and beam dynamics studies. In recent years, there is a growing need for high precision measurement of bunch parameters. However, during the long-term operation of accelerators, signal transmission over long cables suffers from time-delay drift due to factors such as environmental temperature fluctuations, introducing errors in longitudinal position results. To address this problem, this paper proposes a high-precision real-time cable delay calibration method based on multi-frequency differential phase measurement. This method converts cable delay variations into phase differences between signals by injecting multiple sinusoidal calibration signals of different frequencies into the transmission path. This differential measurement approach effectively suppresses common-mode interference and does not require dedicated measurement channels. The calibration signals are coupled into the existing signal path and can operate continuously during normal beam operation without interruption or manual intervention, ensuring non-invasive and real-time calibration. A field-programmable gate array (FPGA)-based digital signal processing architecture is designed to implement the method, supporting continuous, real-time correction of cable delay variations. To validate the method, specialized signal coupling electronics was designed. A dedicated test platform was constructed, and controlled temperature variation tests on a 20-meter cable demonstrate that the proposed method achieves a single-channel delay measurement precision better than 10 fs RMS, which is well within the requirements of bunch-by-bunch longitudinal phase measurement.**

***Index Terms*—accelerator, beam position monitor (BPM), cable delay, FPGA**

I. Introduction

IN modern light source systems, beam position monitors (BPMs) are widely used in accelerator operation and beam studies. Signals from the button-type probes are typically used in areas such as beam orbit monitoring and control, bunch oscillation feedback, beam dynamics studies and machine protection [1-3]. With the continuous advancement of electronics technology and the increasing demands of accelerator design, for new-generation synchrotron radiation light sources and electron-positron colliders, precise measurement of bunch characteristics is essential to enable transient monitoring and real-time adjustment of varying beam parameters [4-6]. In recent years, a series of research efforts have been conducted, leading to high-precision measurement of key parameters such as bunch charge [7,8], transverse position [9,10] and longitudinal phase [11,12].

In large-scale electron accelerators, several key beam diagnostics such as longitudinal phase measurement, high-precision transverse position readout and bunch-by-bunch feedback systems, rely on precise timing of signal transmission [9,13]. Among these applications, bunch-by-bunch longitudinal phase measurement requires especially high time precision [12,14]. At the Shanghai Synchrotron Radiation Facility (SSRF), the time precision of bunch-by-bunch longitudinal position measurement has achieved approximately 0.2 ps RMS [15]. While measurement precision continues to improve, the signal transmission path introduces a new challenge to the long-term stability and absolute accuracy of the system [16,17]. In large accelerator complexes, BPM probes are distributed around the storage ring, connected to centralized data acquisition electronics via tens to hundreds of meters of cables [18,19]. However, the propagation delay through these cables is not static, which is primarily sensitive to ambient temperature fluctuations. For example, in SSRF, the distance between the BPM probes and the phase measurement electronics spans at least 50 meters of cable. For phase-stable cables with a temperature drift parameter of 30 ppm/°C, a temperature variation of 1°C induces approximately 6 ps of signal delay variation. This shift is much larger than the time precision of longitudinal phase measurement, making it necessary to correct such errors.

In regular operation at SSRF, the delay of signal cables is typically calibrated during the experimental platform setup by connecting a time domain reflectometer (TDR) or vector network analyzer (VNA) to the cable [20-22]. The machine is subsequently disconnected, and the cable is then connected to the measurement electronics. However, this calibration approach cannot track slow drifts caused by factors like environmental temperature fluctuations during long-term operation. Post-removal recalibration of cables would not only raise operational complexity and cost, but also interrupt beam time and risk introducing new uncertainties through mechanical reconnection. To address these problems, this paper presents an

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FPGA-based real-time cable delay variation calibration method for large-scale electron accelerators. The method effectively compensates for slow drifts during long-term operation. It features continuous and non-invasive operation with high-precision measurement, thereby enabling real-time correction of cable delay variation without disrupting normal beam operations.

In Section II, the design and the system architecture of the proposed cable delay calibration technique are presented, followed by simulation results. In Section III, the instantiation of the method based on FPGA is presented. Section IV details the experimental setup and presents the measured cable delay variation and precision results. Finally, the conclusion is described in Section V.

II. Cable Delay Calibration Technique

A. Fundamental Model

The foundation of the proposed cable delay calibration method is based on converting the time-domain delay variations into measurable phase variations. This transformation is based on the linear relationship between the propagation delay in a transmission cable and the phase shift of sinusoidal signals. For a calibration signal with frequency f_k, propagating through a cable of a certain length, a slight delay variation Δt introduces a corresponding phase shift according to (1).

$$\delta\varphi = 2\pi f \Delta t \tag{1}$$

However, a single-frequency measurement is sensitive to common-mode interference. To solve this problem, a differential phase measurement model employing multiple calibration frequencies is introduced, using the difference in phase shifts between frequencies to suppress common-mode errors. Considering two calibration signals with frequencies f_1 and f_2, the cable delay variation Δt could be calculated using the equation:

$$\Delta t = \frac{\delta\varphi_1 - \delta\varphi_2}{2\pi(f_1 - f_2)}, \tag{2}$$

The model could be extended to more frequencies. The slope K_{fit} is obtained by performing a linear fit on the dataset (f_k, $\delta\varphi_k$), and the delay variation is computed as $\Delta t = K_{fit}/(2\pi)$. Fitting with multiple appropriately chosen frequencies not only reduces the influence of noise but also allows for the assessment of measurement reliability.

Besides, the differential model also has the function of eliminating phase ambiguity. A single-frequency phase measurement is ambiguous for delay changes greater than $1/f$. In contrast, the differential phase extends the unambiguous range to $1/(f_1 - f_2)$.

B. System Architecture

To achieve real-time cable delay variation calibration, the proposed method establishes a comprehensive workflow for the generation and processing of multi-frequency calibration signals, as shown in the system architecture of Fig. 1. At the input of the transmission cable, multiple sinusoidal calibration signals with frequencies f_1, f_2, …f_n are combined into a single composite signal via a combiner and then coupled onto the original signal transmission path. The calibration tones are set to a sufficiently low power level to avoid saturating the main signal chain, while maintaining an appropriate signal-to-noise ratio (SNR) for phase measurement. If the signal to be processed occupies a relatively narrow frequency band, the calibration signal frequencies could be carefully selected to avoid spectral overlap. This allows for simultaneous signal transmission and delay calibration without mutual interference. Conversely, if the original signal is broadband but transmitted intermittently—for instance, there are multiple unfilled RF buckets in the filling pattern of bunches [23,24]—the calibration signals can be activated during intervals when the original signal is absent.

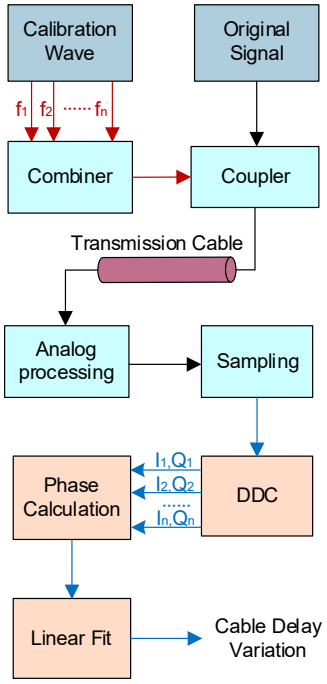

Fig. 1. The block diagram of the architecture

At the receiving end, the combined signal is first passed through an analog circuit to adjust the amplitude of the waveform. It is then digitized by a high-speed sampling circuit, providing the data sequence for subsequent real-time processing.

The goal of the digital signal processing stage is to extract the cable delay information from the mixed digital waveform sequence. First, n sets of orthogonal digital reference sequences are generated, precisely matched to the calibration signal frequencies. These sequences are respectively mixed with the acquired sampled data sequence. Digital low-pass filters are applied to remove the high-frequency components and suppress out-of-band noise. Using (3), N sets of baseband in-phase (I) and quadrature (Q) components containing the amplitude and phase information of the calibration signals are obtained.

$$\begin{aligned} I_k &= A_k cos(\varphi_k) \\ Q_k &= A_k \sin(\varphi_k) \end{aligned} \tag{3}$$

where A_k is the amplitude and φ_k is the phase. The precise phase variation $\delta\varphi_k$ value is calculated in real time using a Coordinate Rotation Digital Computer (CORDIC) algorithm,

which computes: $\varphi_k = arctan2(Q_k, I_k)$. This process runs in parallel for all calibration frequencies, producing a series of phase values $[\varphi_1, \varphi_2, ..., \varphi_n]$.

After phase unwrapping, the phase variation $\delta\varphi_k$ is obtained by differencing the current phase result with that of the last time. Finally, the phase variations $[\delta\varphi_1, \delta\varphi_2, ..., \delta\varphi_n]$ and the known frequencies $[f_1, f_2, ..., f_n]$ are fed into a linear fitting unit. The cable delay variation result is then transmitted for real-time correction of the longitudinal phase measurement result of BPM signals.

C. Simulation

To preliminarily validate the feasibility and measurement precision of the proposed method, a comprehensive simulation model was established. This simulation model includes the entire signal chain, including calibration signal generation, cable transmission, analog signal conditioning, sampling quantization, and digital signal processing. For the calibration signals, three distinct frequencies—100 MHz, 125 MHz, and 166.7 MHz—were selected and subsequently synthesized into a composite waveform. Currently, the Analog-to-Digital Converters (ADCs) employed in bunch-by-bunch longitudinal phase measurement systems generally operate at the GSps level. The state-of-the-art electronic system, which achieves the highest reported phase measurement precision of 0.2 ps at SSRF [15], utilizes a sampling rate of 10 GSps. To maintain a sufficient design margin, an ADC operating at a sampling rate of 2.5 GSps was adopted in the simulation. To emulate the cable-induced delay variation Δt, a 6 ps variation was introduced in the signal transmission.

Based on the parameters of the clock circuits integrated in the existing high-speed data acquisition card, ADC sampling clock jitter was incorporated into the simulation [25]. Furthermore, thermal noise contributions arising from attenuators, amplifiers within the analog processing circuits, and the ADC were accounted for, thereby modeling the analog white noise and ADC noise in the electronics. The noise parameters used here are extracted from the datasheets of the actual chips in the data acquisition card used in the test system [26], ensuring that the simulated noise environment closely reflects the real hardware conditions. To accommodate the operational mode of combining the calibration signal with the BPM signal, the amplitude of the synthesized sinusoidal waves was set to a relatively low level, which degrades the SNR of the calibration tones and poses a challenge to the time precision measurement. The signal spectrum obtained from the ADC sampling simulation is presented in Fig. 2, where the SNR for a single-frequency sinusoidal wave is approximately -26.9 dB.

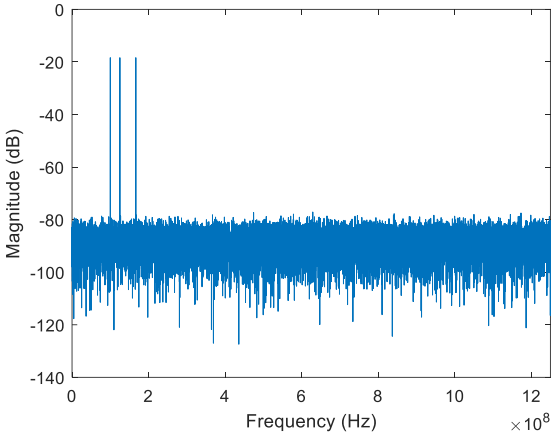

Fig. 2. Signal spectrum of ADC sampling simulation

To evaluate the digital signal processing algorithm, simulations of the mixing and low-pass filtering stages were conducted. To reduce the sampling rate and improve the SNR, multi-stage Cascaded Integrator-Comb (CIC) decimation filtering was applied to extract the DC I/Q components for each frequency point. To further mitigate the impact of low-frequency noise, an additional Finite Impulse Response (FIR) filter was incorporated at the end, from which the phase variation was subsequently calculated. Finally, the cable delay variation Δt was computed using the three-frequency linear fitting method.

The simulation results are shown in Fig. 3. The time precision of the proposed cable delay measurement method is approximately 5 fs RMS, which is well below the design target of 50 fs. This simulation result is achieved under the low SNR of the sampled signal, confirming the robustness of the proposed method against challenging signal conditions.

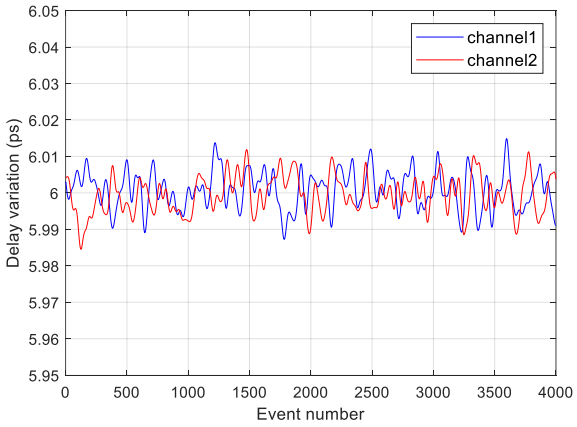

Fig. 3. Simulation results

These simulation results theoretically confirm the correctness and feasibility of the cable delay variation calibration method.

III. Instantiation of Cable Delay Calibration Logic

To realize real-time calibration of cable delay variations and correction of longitudinal phase results, an FPGA logic based on a pipeline structure is designed. The overall logic

architecture is illustrated in Fig. 4, including data acquisition and preprocessing, cable delay variation calculation algorithm based on multi-frequency differential phase measurement, result screening and assembly, among other functions. A system clock, derived from a high-performance external phase-locked loop (PLL), serves as the timing reference for all synchronous logic. In consideration of the practical operational scenario where a single board receives four channels of BPM signals, the design incorporates four parallel delay variation calculation channels alongside longitudinal BPM phase calculation channels.

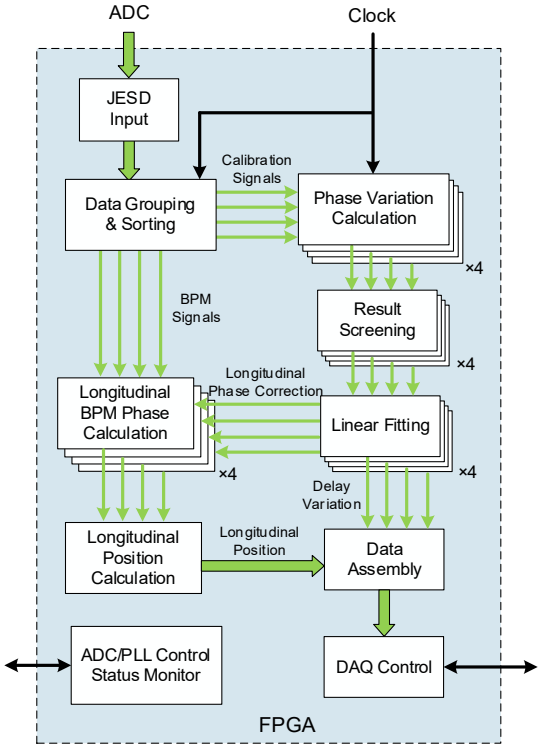

Fig. 4. Block diagram of logic architecture

First, the serial data streams from the ADCs are reconstructed into parallel data in accordance with the JESD204B high-speed serial interface protocol. The recovered sampled data is then grouped and sorted based on its sampling timestamp and channel identifier. This allows for the routing of calibration signals and beam signals to their respective calculation modules.

At the algorithmic stage, calibration signals are processed through mixing, filtering, and phase extraction to obtain a preliminary estimation of the phase variation. To further improve the accuracy of measurement, a Result Screening module is incorporated into the system. This module conducts validity screening on the calculated phase variation values, identifying and discarding invalid data caused by signal disturbances or similar effects. The validated data is then implemented to linear fitting, which smooths the phase drift trend and outputs a more precise delay variation value. This computed delay variation is utilized as a feedback quantity to correct the longitudinal phase measurement results of BPM signals for each channel over a defined time interval. Concurrently, the phase variation data and the delay variation data are assembled and packaged into event packets according to a regulated data format. These packets are ultimately transmitted via a high-speed data interface to the data acquisition system. Furthermore, the logic also integrates the function of the configuration of ADC and PLL, as well as electronics status monitoring.

The block diagram of the phase variation calculation logic module of one channel is presented in Fig. 5, which adopts a multi-frequency parallel digital signal processing architecture. The ADC-sampled data stream is distributed across three independent processing channels, enabling synchronous analysis and computation of the three distinct frequency components constituting the composite sinusoidal signal.

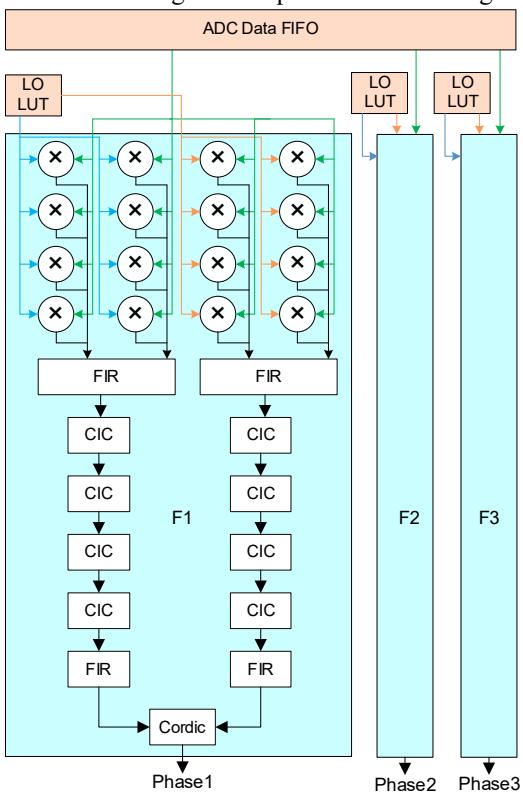

Fig. 5. Block diagram of the phase calculation logic

The system initially generates orthogonal local oscillator signals via a Local Oscillator (LO) Look-Up Table (LUT). These LO signals are subsequently mixed with the incoming ADC data stream through dedicated multiplier units, effecting a frequency translation of the signal components at disparate frequencies down to baseband. This down-conversion facilitates subsequent efficient digital processing by extracting the in-phase and quadrature components of the signal. Following the mixing stage, the resulting signals are directed into a CIC filter array. To attain high-precision measurement and adequate anti-aliasing performance, a cascade of five CIC filter stages is configured, which effectively suppresses high-frequency components and retains only the baseband I/Q signals at an output rate of 800 Hz. Owing to the fact that the ADC sampling frequency is higher than the maximum achievable logic frequency of the FPGA, the ADC data is partitioned into eight parallel groups. The mixing operation is realized through parallel multiply-accumulate computations,

and the initial filtering stage is implemented using FIR filter structures loaded with the equivalent CIC coefficients.

After decimation by the CIC filters, the data undergoes further processing by FIR filters, which provide finer frequency response shaping and enhance the signal-to-noise ratio. Finally, the CORDIC algorithm is utilized to efficiently extract the phase information, yielding the instantaneous phase values for each frequency component. By calculating the difference between the current phase result and that acquired at the preceding time instant, the phase variation results for all three frequencies are determined. These results are then used in subsequent linear fitting to obtain the cable delay variation results.

IV. Implementation and Validation

A. Design of Evaluation System

To validate the precision and real-time performance of the proposed real-time cable delay calibration method, a dedicated test system shown in Fig. 6 was constructed.

The test system primarily consists of calibration signal module, long transmission cables, and data acquisition card. A waveform generator produces simulated beam signals, which are evenly split into multiple channels via a power divider. Within the calibration signal generation module, these signals are combined with calibration signals via a coupler before being injected into the cable. The data acquisition card first performs analog processing and high-speed sampling of the signals received from the transmission cable. Real-time processing of the algorithm is then performed by the FPGA, and the calibration results are output.

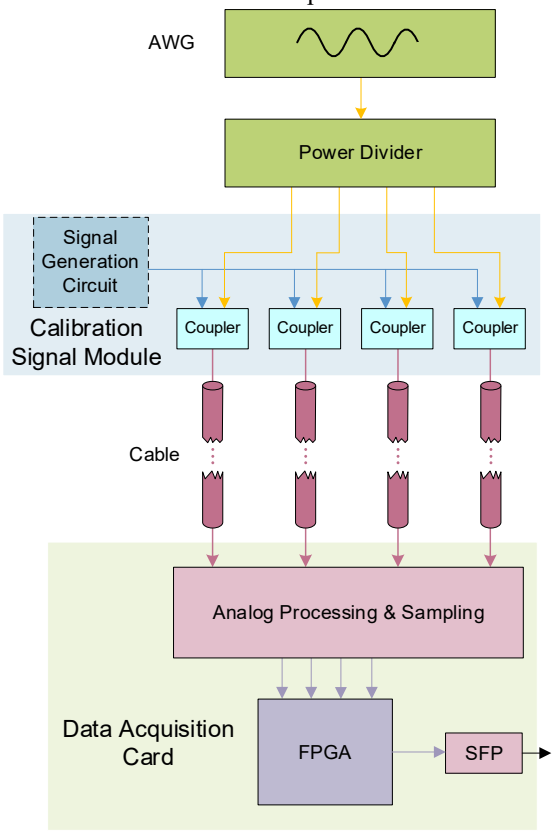

Fig. 6. Block diagram of the test system

The analog front end of the data acquisition card adjusts signal gain via programmable attenuators and amplifier circuits. Signal waveforms are then sampled by the 14-bit ADCs operating at a sampling rate of 2.5 Gsps [25]. The ADC sampling clock, which shares a common source clock with the calibration signals, is generated by a high-precision PLL, with an output clock jitter of approximately 70 fs [26]. This PLL also supplies the reference clock for the JESD interface and the system clock for the FPGA. The real-time cable delay correction algorithm is implemented on a Xilinx XCKU085 FPGA [27], which provides sufficient logic resources to support pipelined digital down-conversion (DDC) and delay calculation. The real-time computation results are transmitted to the host computer via an small form-factor pluggable (SFP)-based Ethernet interface.

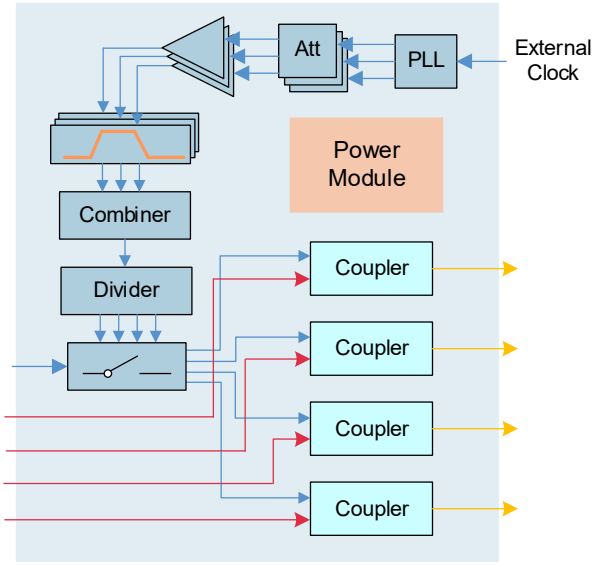

Fig. 7. Block diagram of calibration signal module

The dedicated calibration signal module, as block diagram shown in Fig. 7, was specifically designed and developed for the application of the proposed method. An external reference clock is fed into the PLL, which synthesizes and outputs three clock channels. Each clock frequency corresponds to one of the three sinusoidal calibration frequencies. The signals pass sequentially through adjustable attenuators and RF amplifiers to adjust the waveform amplitude and improve the SNR of the signals. The signals are then filtered by bandpass filters with different bandwidths to suppress harmonics and out-of-band noise, thereby generating sinusoidal waves at the proposed calibration frequencies. The signals from all three channels are combined via a power combiner to form the required calibration signal, which is then divided into the four channels through a power divider. The calibration waves are then coupled into the main signal paths through couplers. The coupling function of the signal is controlled via a programmable switch. The photograph of the calibration signal module is shown in Fig. 8.

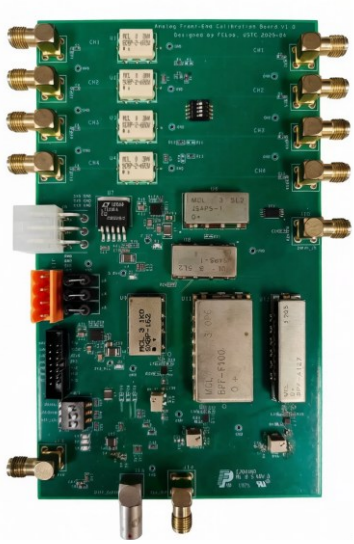

Fig. 8. Photograph of calibration signal module

B. *Test and Results*

Considering the performance differences of cables at various temperatures, to simulate the temperature drift in actual accelerator environments, a test platform was constructed based on a temperature chamber capable of wide-range temperature adjustment. The test setup is shown in Fig. 9. The structure of the temperature chamber test platform is similar to that shown in Fig. 6, except that only one cable is used and the cable output is split via a power divider into two channels for evaluating the precision of single-channel delay variation measurement. A 20-meter cable used in the accelerator system was placed inside the temperature chamber. The temperature was gradually increased from 0 °C to 40 °C, with a pause at every 5 °C increment. This temperature range fully covers the ambient cable temperatures in actual beam experiments.

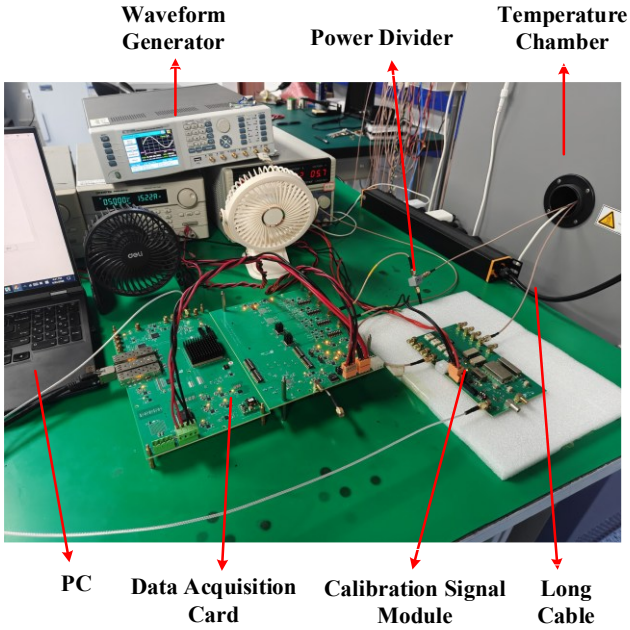

Fig. 9. Photo of the test platform

During the temperature chamber test, the system continuously recorded cable delay variations at an update rate of 800 Hz. Fig. 10 presents the cable delay variation as a function of temperature. As shown in the figure, the cable delay increases with rising temperature. For the same temperature variation of 5°C, the cable delay variation exhibits different magnitudes at different baseline temperatures. For a 40°C variation in ambient temperature, the cable delay shift was over 400 ps. This corresponds to a temperature sensitivity of 10 ps/°C, which is much larger than the precision of longitudinal phase measurements. The entire temperature curve was obtained from a single two-hour measurement run, demonstrating that the proposed method is capable of continuously capturing cable delay variation induced by temperature fluctuations in real time.

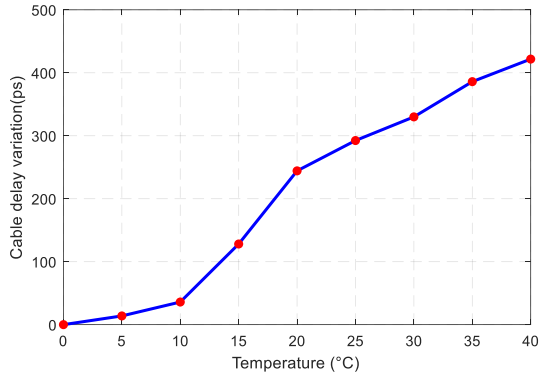

Fig. 10. Cable delay variation at different temperature

To evaluate the precision of single-channel delay variation calculation, the delay line method was adopted. A power divider was terminated at the end of the cable, splitting the signal equally to two channels of the data acquisition card. The difference between the delay variations calculated from the two channels was statistically analyzed. Fig. 11 shows the distribution of single-channel delay variation measurement at 25 °C, achieving a precision of 6.90 fs RMS.

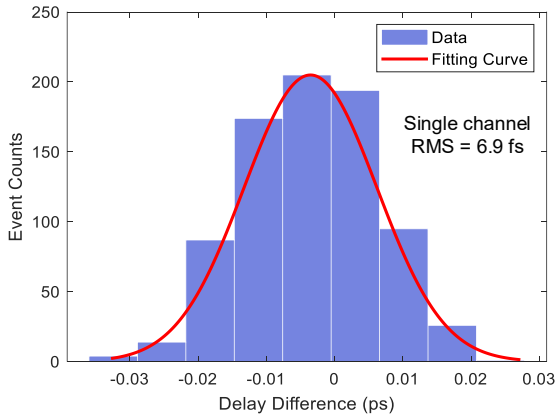

Fig. 11. Distribution of single-channel delay variation measurement at 25 °C

To further verify the performance of the proposed method under various accelerator environments, more tests were conducted at multiple temperatures based on the measurement scheme shown in Fig. 11. The time precision of single-channel

cable delay variation measurement was evaluated over a temperature range from 0 °C to 40 °C. As the test results shown in Fig. 12, the measurement precision is better than 10 fs RMS across the tested temperature range. Given that the current precision of bunch-by-bunch longitudinal phase measurement is approximately 0.2 ps [15], and the precision of the proposed method is significantly lower, the method fully meets the cable delay calibration requirements of the accelerator.

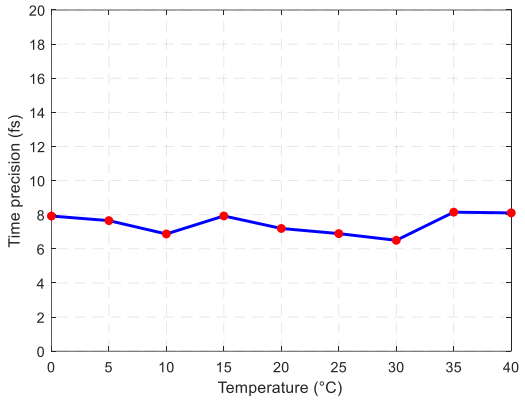

Fig. 12. Time precision of the delay variation measurement under different temperatures

V. Conclusion

This study developed a real-time cable delay calibration method designed to correct timing errors in bunch-by-bunch beam position measurements for large-scale electron accelerators. The proposed method employs a multi-frequency differential phase measurement model, which effectively suppresses common-mode interference. By converting time-domain delay variations into phase differences between multiple sinusoidal calibration signals, the method achieves high precision without requiring dedicated measurement channels. An FPGA-based digital signal processing architecture was implemented. The system supports real-time, continuous calibration during normal accelerator operation, enabling real-time correction of longitudinal phase measurement results.

Simulation results have demonstrated a cable delay measurement precision better than 10 fs RMS. Experimental validation using a dedicated test platform with temperature chamber showed that the method can continuously capture cable delay variations induced by temperature fluctuations. Over a 40°C temperature range, the cable delay variation exceeded 400 ps. The time precision of single-channel delay variation measurement was confirmed to be better than 10 fs RMS, which is well within the requirements for bunch-by-bunch longitudinal phase measurement.

The proposed method provides a real-time, non-invasive, and high-precision solution for cable delay variation calibration in large-scale accelerator facilities. It eliminates manual recalibration and dedicated measurement channels, reducing operational complexity and improving long-term system stability. Future work may explore extending the method to more application.

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