Design of Transmission Cable Delay Calibration Method for Large-Scale Electron Accelerators

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1. Introduction

For new-generation synchrotron radiation light sources and electron-positron colliders, precise measurement of individual bunch characteristics is essential to enable transient monitoring and real-time adjustment of varying beam parameters. In recent years, a series of research efforts have been conducted, leading to high-precision measurement of key parameters such as bunch charge, transverse position and longitudinal phase.

At the Shanghai Synchrotron Radiation Facility (SSRF), the time precision of bunch-by-bunch longitudinal position measurement has achieved better than 1 ps RMS. However, during long-term beam experiment operation, temperature fluctuations and mechanical instabilities along the signal transmission path can also introduce deviations in the bunch-by-bunch longitudinal phase measurement results. For example, in SSRF, with at least 50 meters of phase-stable cable (temperature drift ~30 ppm/℃) between BPMs and electronics, a 1℃ temperature variation induces ~6 ps signal delay change. This exceeds the measurement precision and necessitates correction. Since post-removal recalibration of cables would not only raise operational complexity and cost, but also risk introducing new uncertainties through mechanical reconnection. To address these problems, a dedicated real-time cable delay calibration method is presented for large-scale electron accelerators.

2. Technique and Instantiation

For a sinusoidal signal with frequency f, propagating through a cable of a certain length, a slight delay variation Δt results in a corresponding phase change $\delta\varphi = 2\pi f \cdot \Delta t$. By introducing multiple calibration signals at different frequencies(f_1, f_2, …f_n), a differential measurement model is constructed. The delay is calculated using two frequencies as:

$$\Delta t = \frac{\delta\varphi_1 - \delta\varphi_2}{2\pi(f_1 - f_2)}$$

Advantages:

- Effectively suppresses common-mode interference through differential calculation.
- Enables continuous calibration during normal system operation without a dedicated measurement channel.
- Calibration signals can be transmitted simultaneously with the original signal via frequency-division multiplexing (for narrowband signals) or time-division multiplexing (for broadband/intermittent signals), avoiding mutual interference.

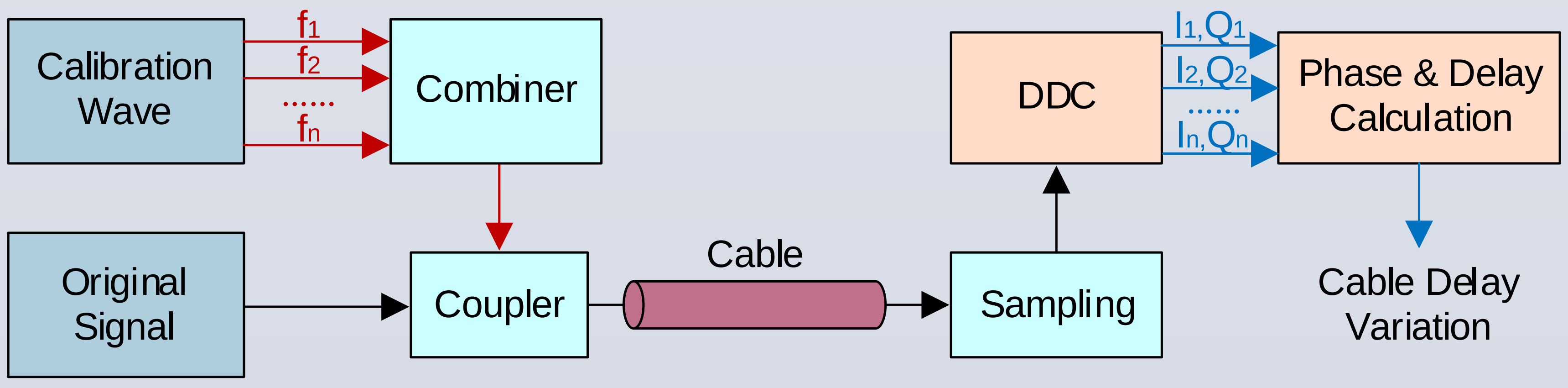

Fig. 1. The workflow of cable delay calibration method

A comprehensive workflow for the generation and processing of multi-frequency calibration signals is established, as depicted in Fig. 1. At the input of the transmission cable, multiple sinusoidal calibration signals are combined into a single composite signal via a combiner and then coupled onto the original signal transmission path. At the receiving end, a high-speed sampling circuit digitizes this composite signal, providing the data sequence for subsequent processing.

Digital signal processing stage is to extract the cable delay information from the mixed digital waveform sequence. Orthogonal digital reference sequences matching the calibration frequencies are generated. After mixing with the sampled data and low-pass filtering, the baseband I_k and Q_k components containing amplitude and phase information are obtained:

$$I_k = A_k cos(\varphi_k)$$
$$Q_k = A_k \sin(\varphi_k)$$

The phase $\varphi_k = arctan2(Q_k, I_k)$ is calculated to derive the delay variation.

A pipeline-structured FPGA logic, as depicted in Fig. 2, is designed for real-time phase calculation and delay calibration.

The block diagram of the phase calculation logic is shown in Fig. 3. The digital signal sequence of each channel is separately mixed with the local oscillator waveform sequence, followed by low-pass filtering and decimation to obtain the DC components I and Q. Phase information is then derived using the arctan function. To capture phase variations at different update rates while balancing stopband rejection and processing latency, a multi-stage digital filtering and decimation structure is utilized.

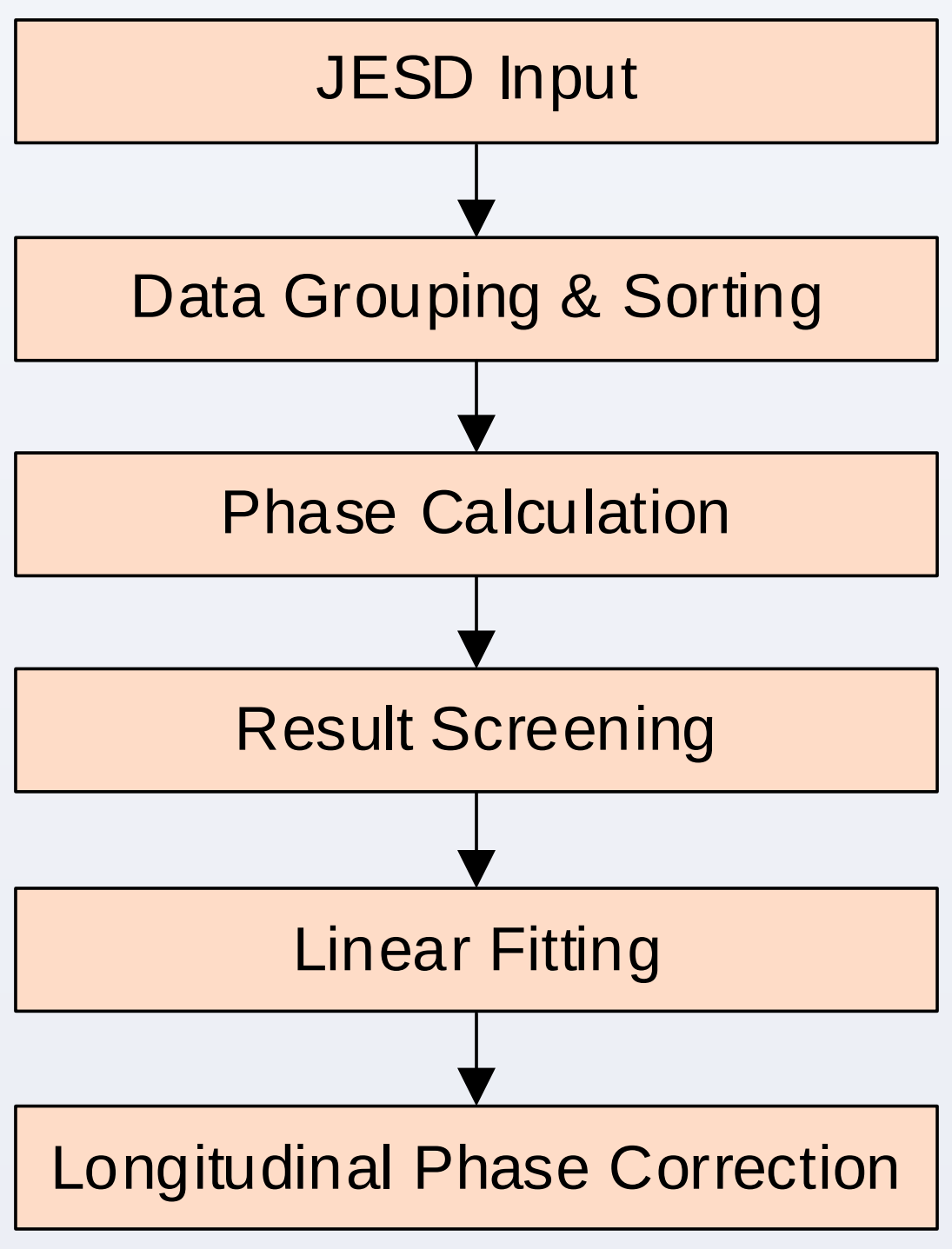

Fig. 2. Data processing logic architecture

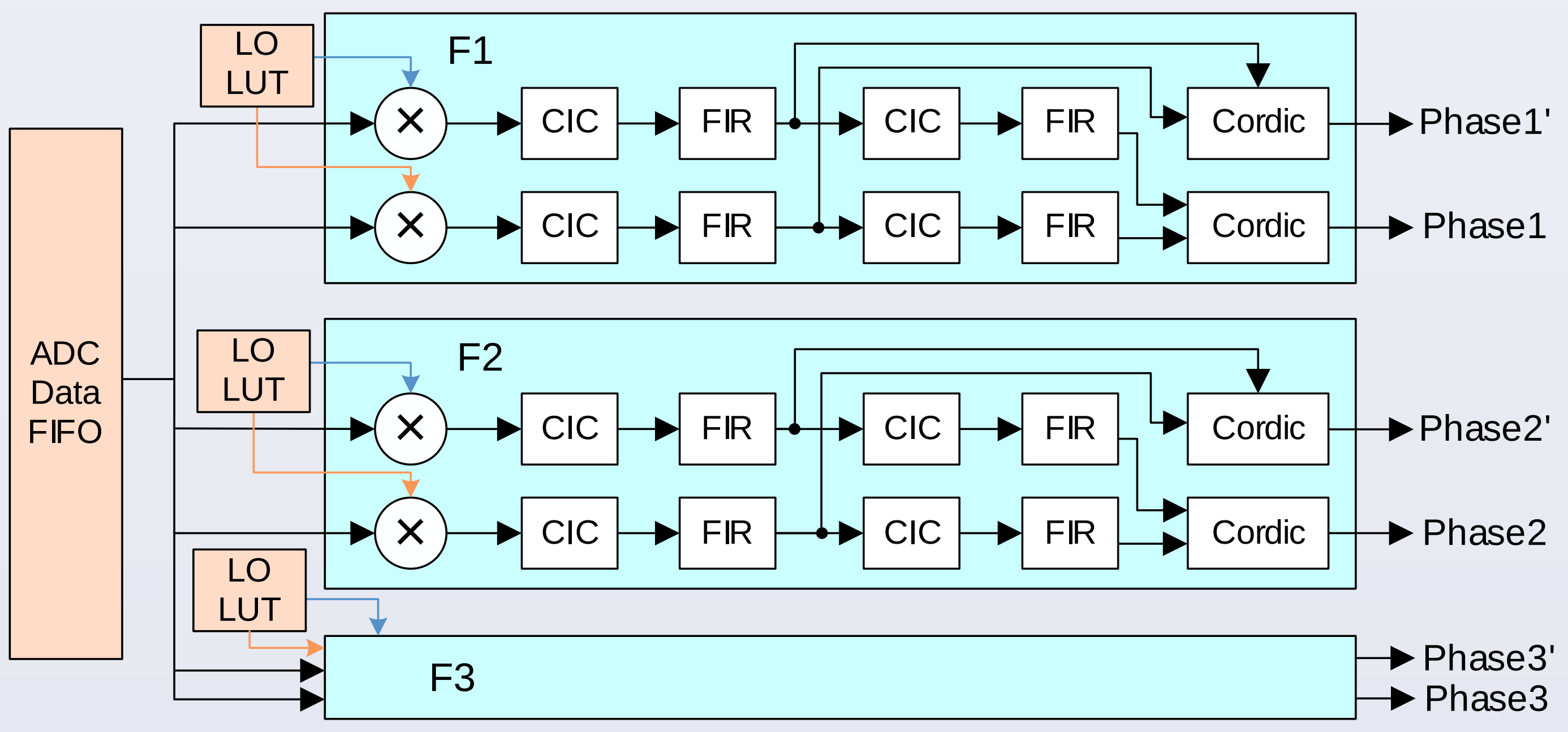

Fig. 3. Block diagram of the phase calculation logic

3. Experimental Implementation and Validation

A dedicated calibration signal module was developed, and the test platform shown in Fig. 4 was constructed based on data acquisition card. The calibration signal electronics generates corresponding waveforms using a phase-locked loop (PLL), followed by attenuation/amplification circuits and filtering before being combined. The combined signal is then power-divided into four channels, each coupled into a corresponding BPM signal path.

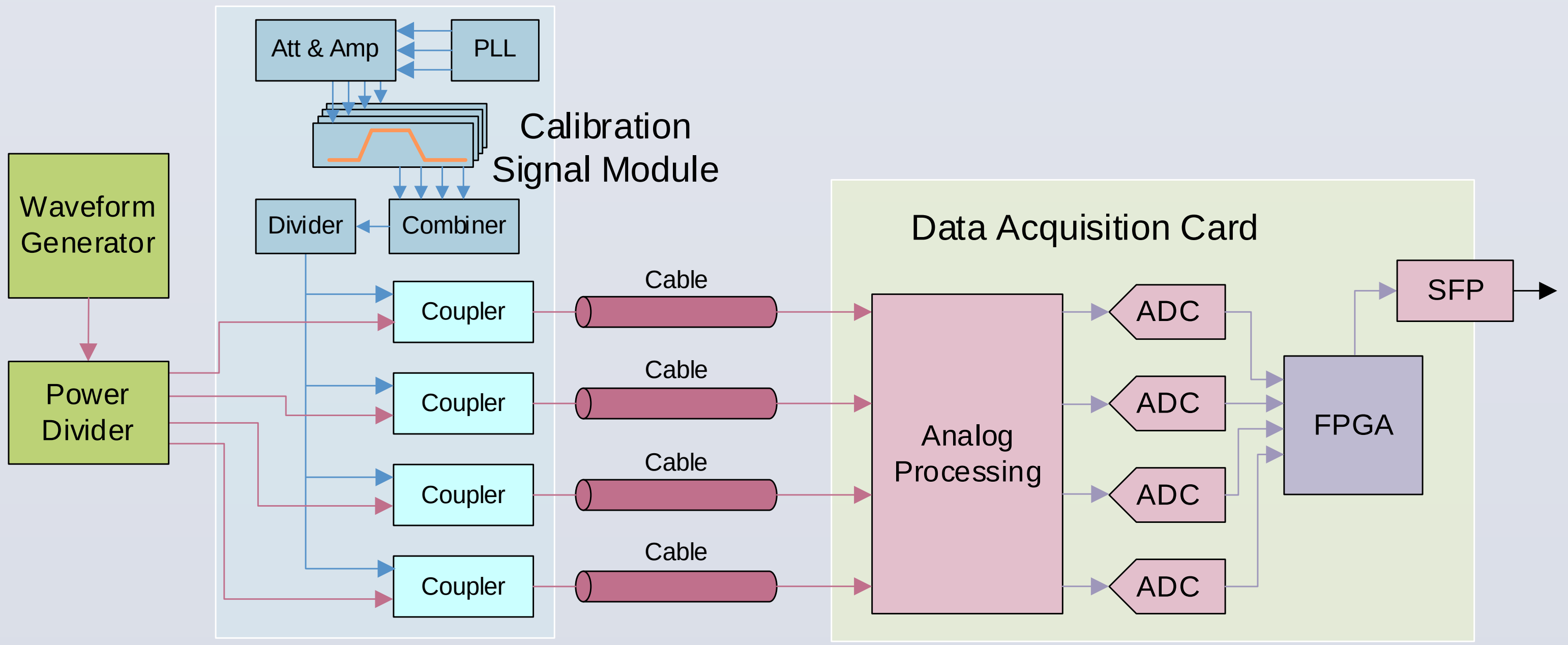

Fig. 4. Block diagram of test platform

A 20-meter cable was used and placed inside a temperature chamber. During testing, the delay variation was recorded as the temperature gradually increased. The cable delay variation results are shown in Fig. 5. A power divider was used at the end of the cable to split the signal into two channels, and the precision of single-channel delay calculation was evaluated. The test results, as shown in Fig. 6, indicate that the precision is better than 30 fs rms, meeting the requirements.

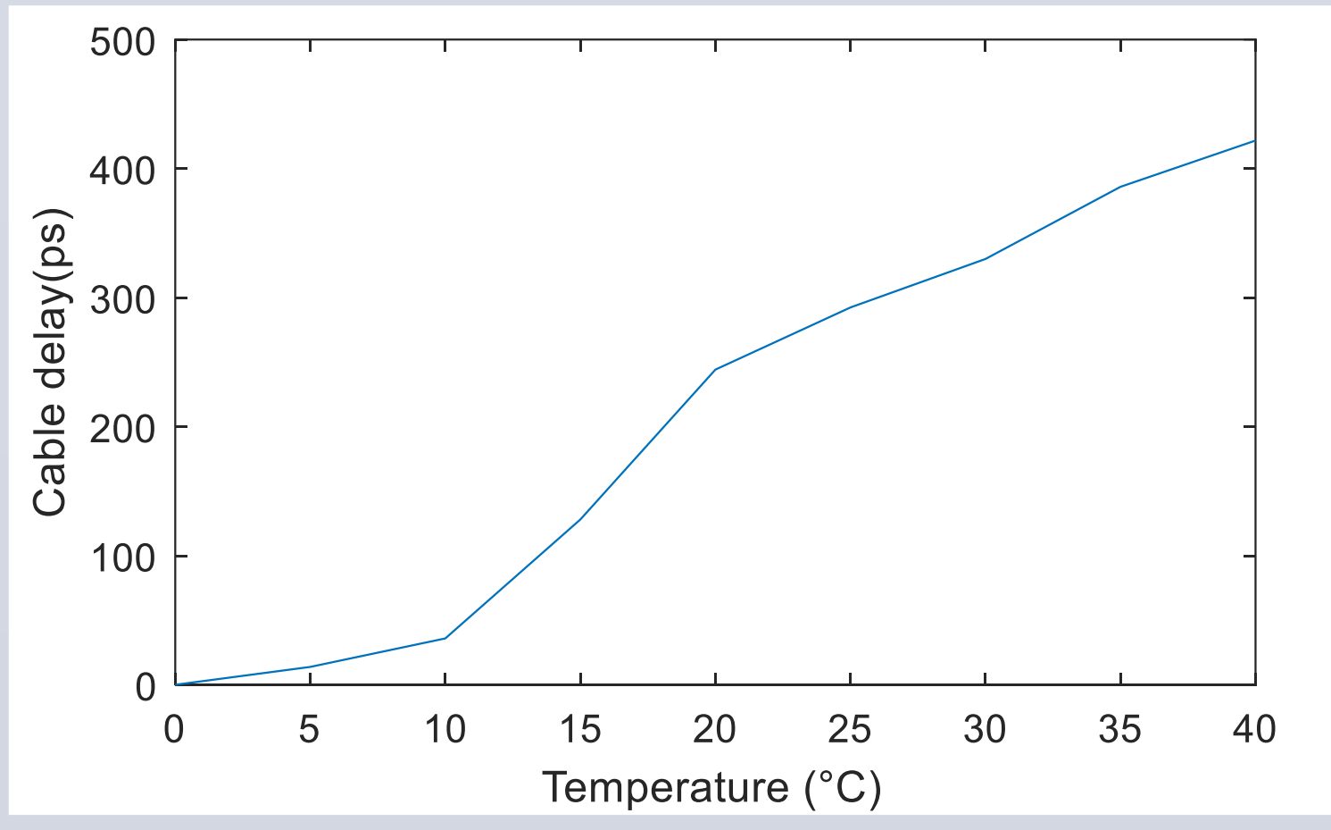

Fig. 5. The cable delay variation results

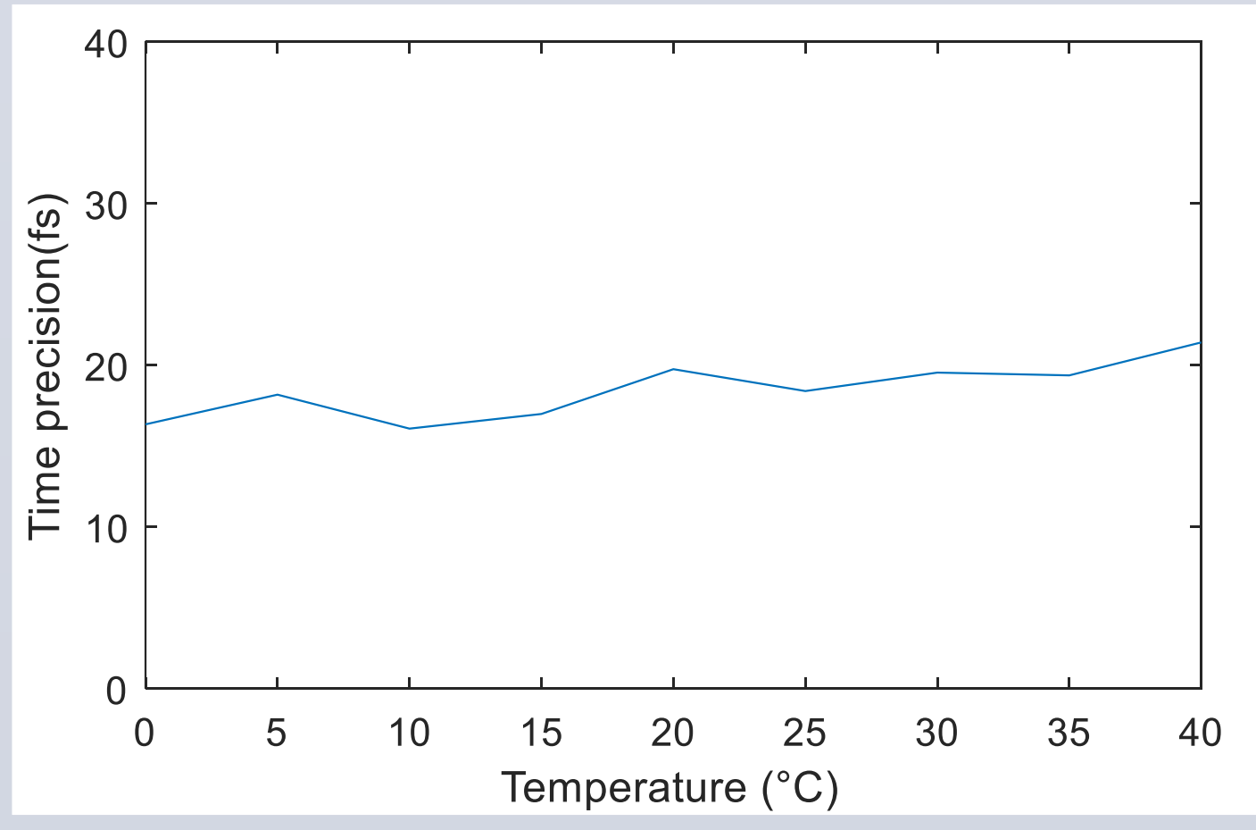

Fig. 6. The precision of delay calculation

4. SUMMARY

In conclusion, a real-time cable delay calibration method was developed to correct timing errors in bunch-by-bunch measurement results. Using multi-frequency differential phase measurement, this method achieves high time resolution without dedicated channels. FPGA-based implementation enables continuous calibration during operation. The test results indicate that cable delay measurement meets the time precision requirements.

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