Development of a Cost-Efficient 64-Channel Multi-Phase Clock TDC on an Artix-7 FPGA

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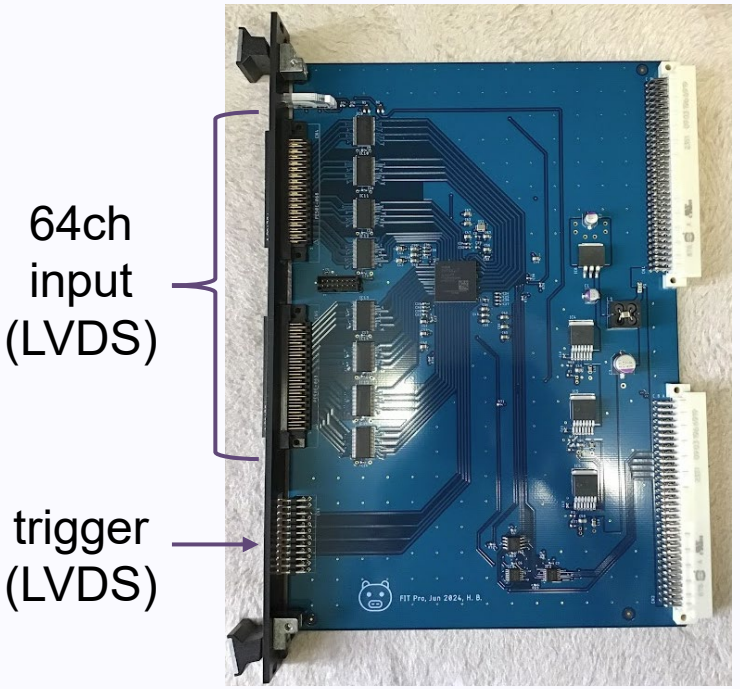
Japan

Overview

XC7A50T-2FGG484I

- Affordable PRICE
  - **64** channel TDC in **$100** FPGA
- Practical RESOLUTION
  - 312.5 ps LSB < 156.2 ps (RMS)
    - for both leading and trailing edges
  - 125 ps LSB < 72.4 ps (RMS)
    - for only leading edge
- READY to use
  - no calibration
  - data is relative to trigger timing

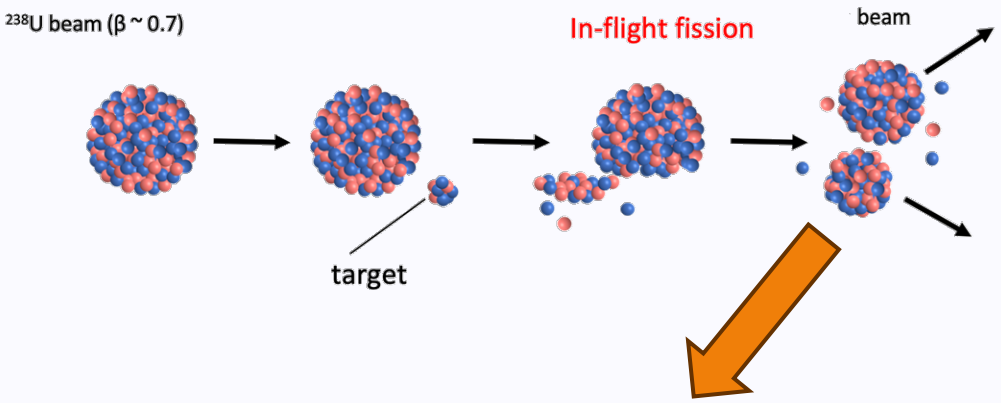
TDC board based on Artix-7

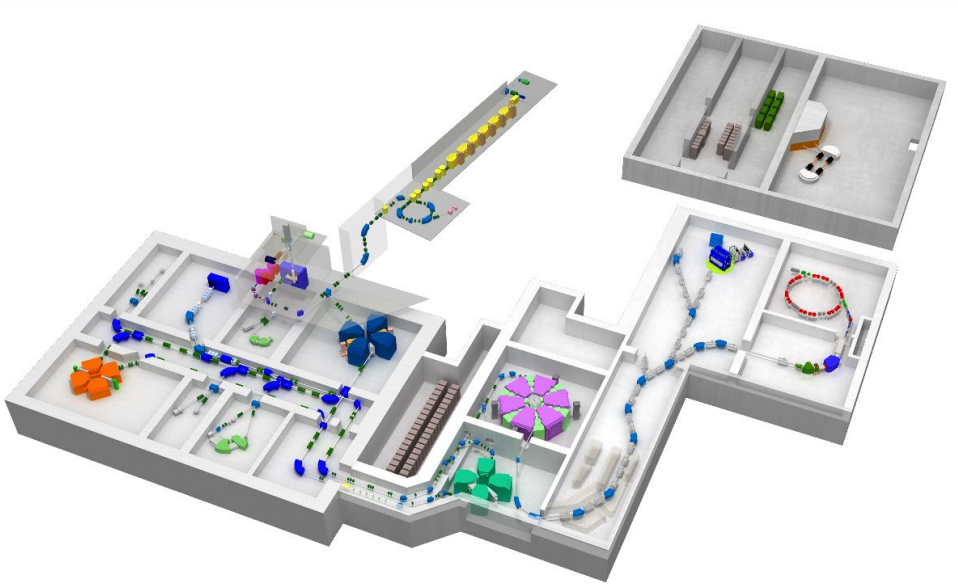


Physics

RIKEN RI Beam Factory (RIBF)

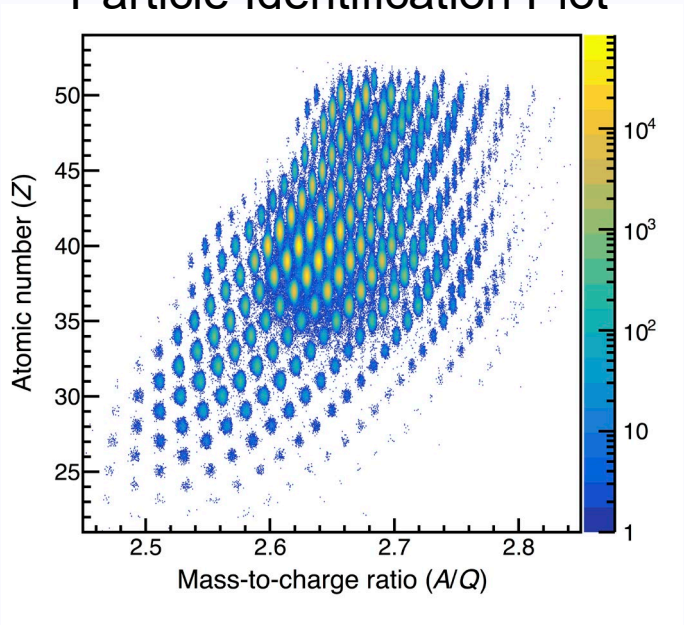
RIKEN NISHINA CENTER



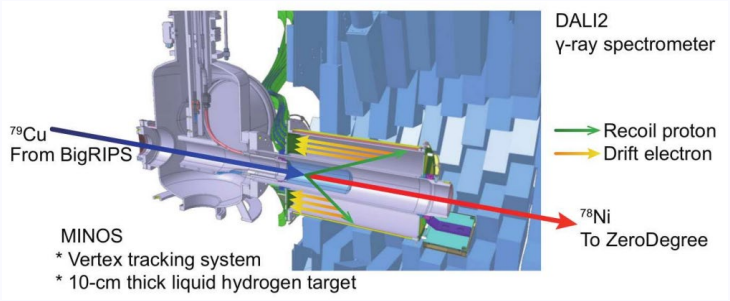


113
Nh
nihonium

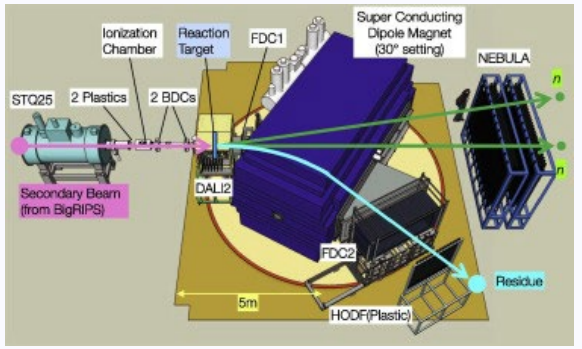
Particle Identification Plot



deliver RI beams
to experimental area



gamma-ray
spectroscopy



proton + neutron
+ heavy ion
coincidence
measurement

Target Detectors

Parallel Plate Avalanche Counter (PPAC)

https://doi.org/10.1016/j.nimb.2013.08.050

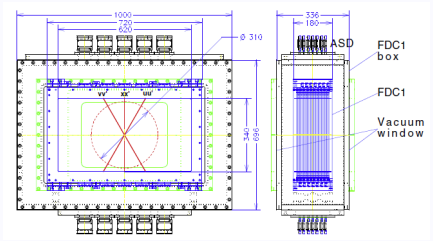
~ 100 ps (RMS)
~ 500 channel
multi-hit, leading edge timing

CAEN V1190 (HPTDC ASIC)
LSB 100ps, RMS <80ps

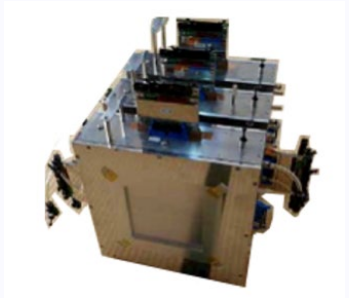
Crystal Scintillator

NaI(Tl), LaBr3(Ce), GAGG(Ce)
~ few hundred ps (RMS)
single-hit, leading edge timing

Drift Chamber



https://doi.org/10.1016/j.nimb.2013.05.089



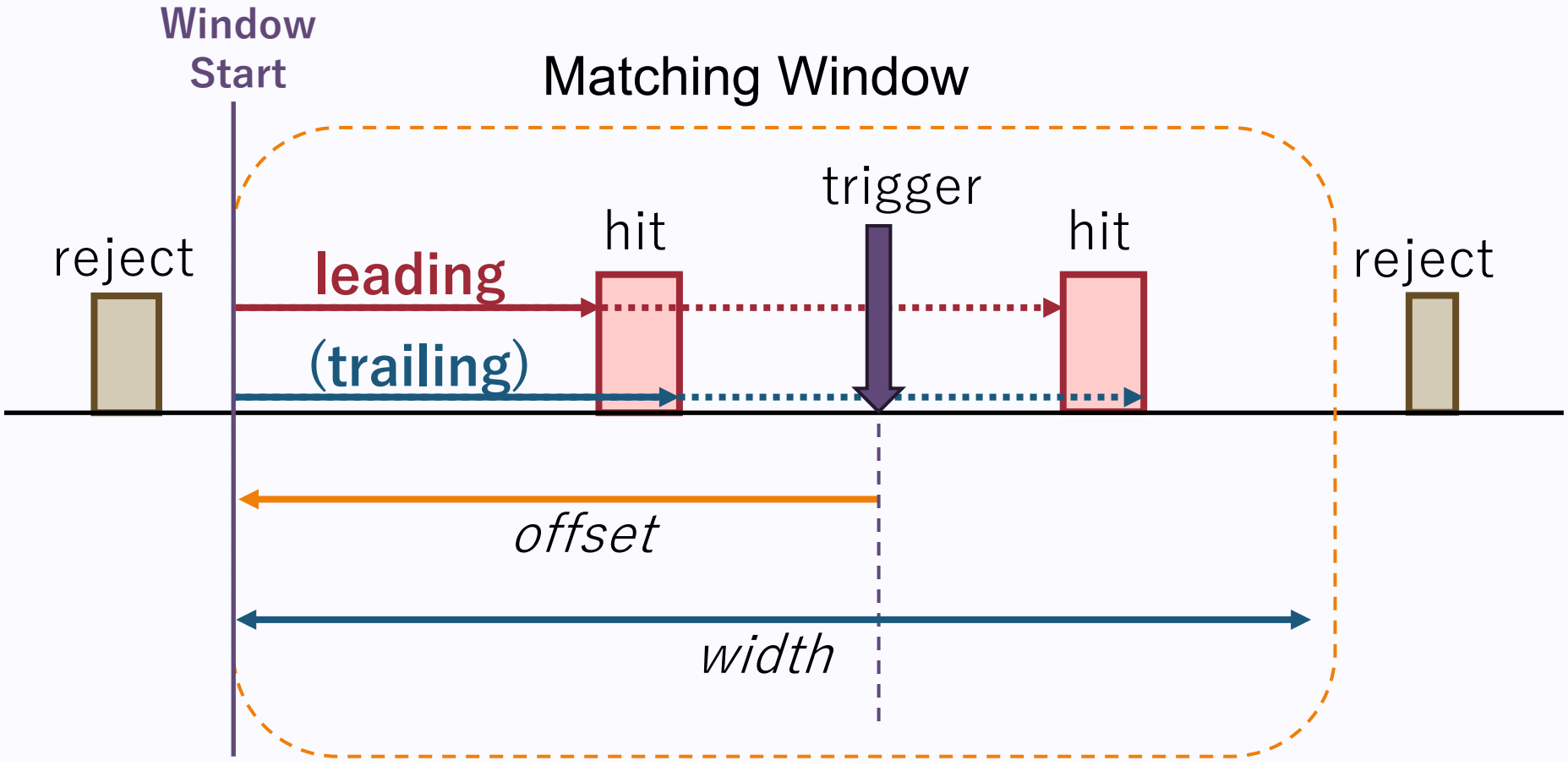
https://indico.ibs.re.kr/event/677/contributions/5957/attachments/4291/5671/New_Neutron_detector24_pub.pdf

~ 400 ps (RMS)
>> 5000 channel
multi-hit, leading and trailing edge

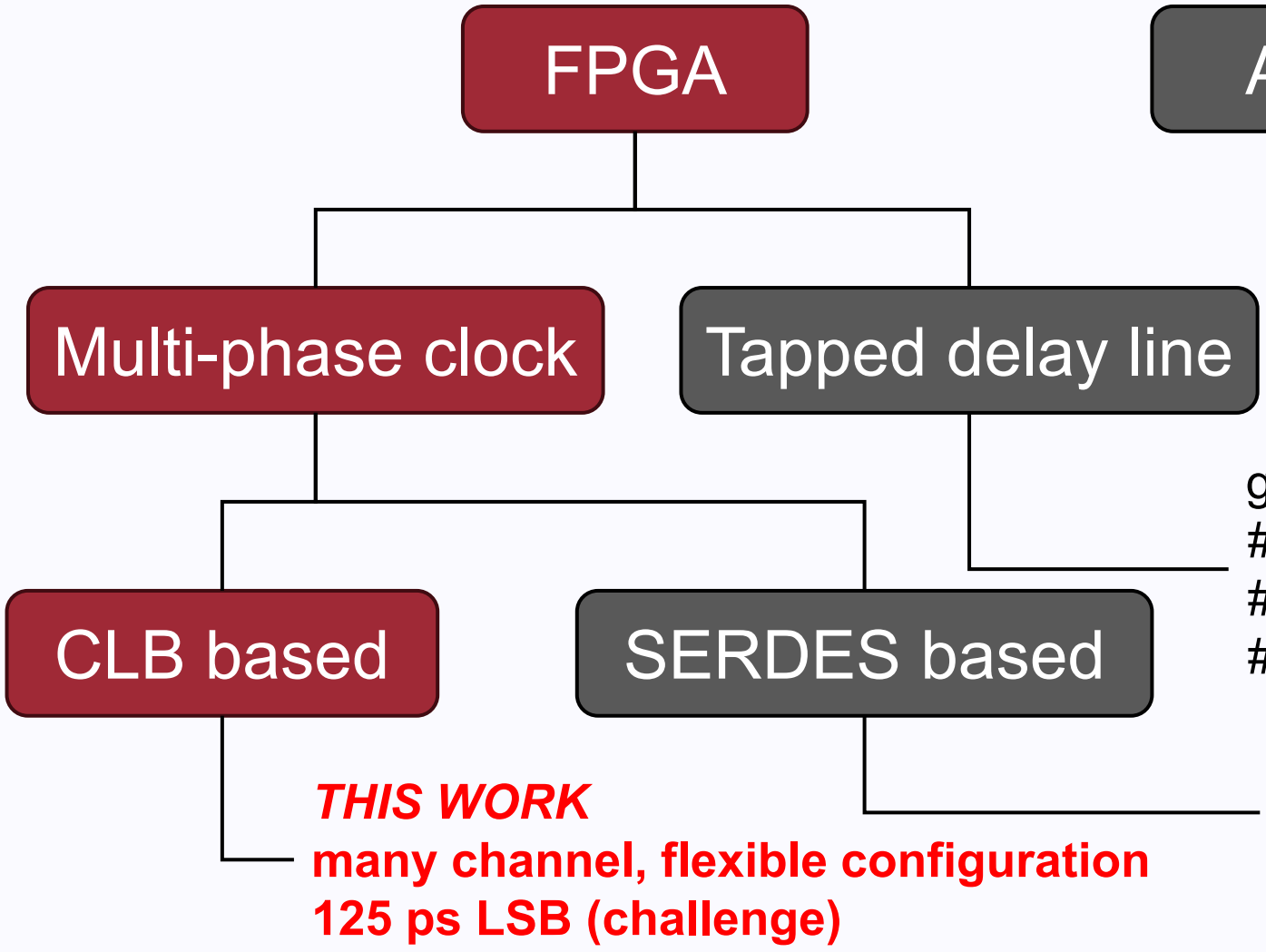
AMT-VME (AMT ASIC)
LSB 780ps / RMS 380ps

TDC Functionality

set “Matching Window” for hit selection (similar to HPTDC)
multi-hit detection capability within the matching window (similar to HPTDC)
leading (trailing) edge timing relative to the window start



Choice of Method



good **for mass production**
CERN **HPTDC**, **PicoTDC**
KEK AMT
#162 Xiongbo Yan
#177 Zhuang Li

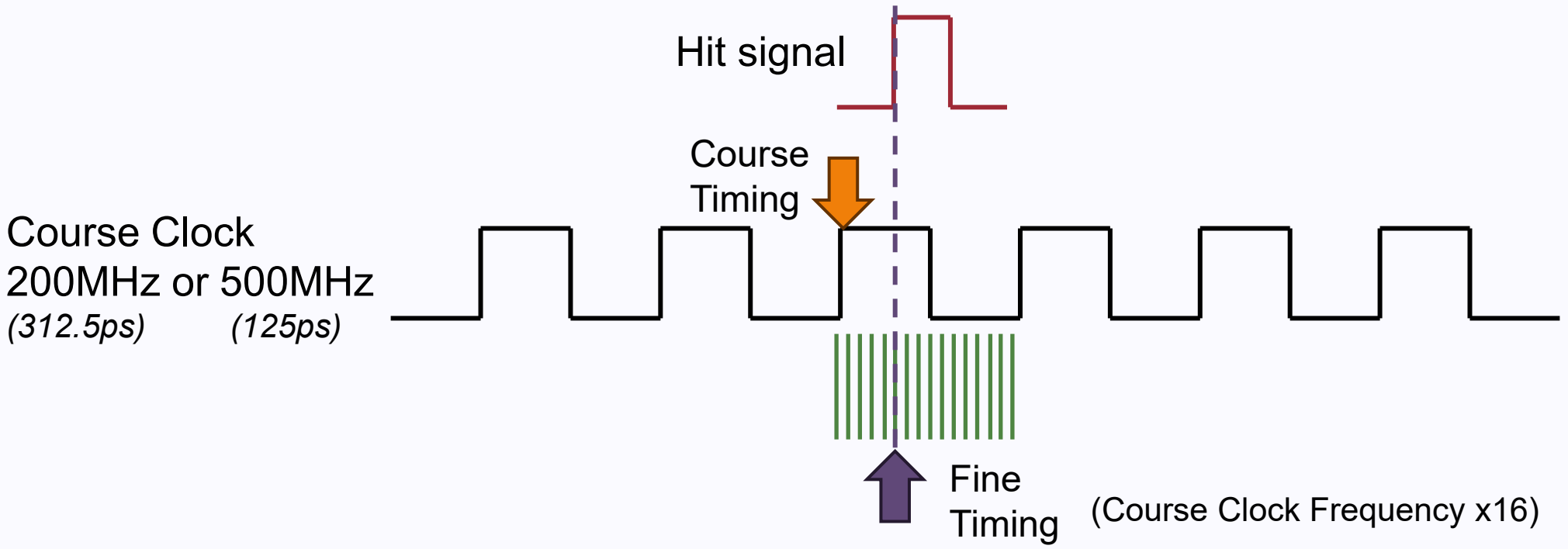
good **timing resolution**, high resource usage
#43 Julien Rossignol
#85 Yuchen Yang
#199 Giancarlo Sportelli

THIS WORK
many channel, flexible configuration
125 ps LSB (challenge)

many channel, resource optimized
applicable to 200 – 300 ps LSB
constrained by SERDES architecture

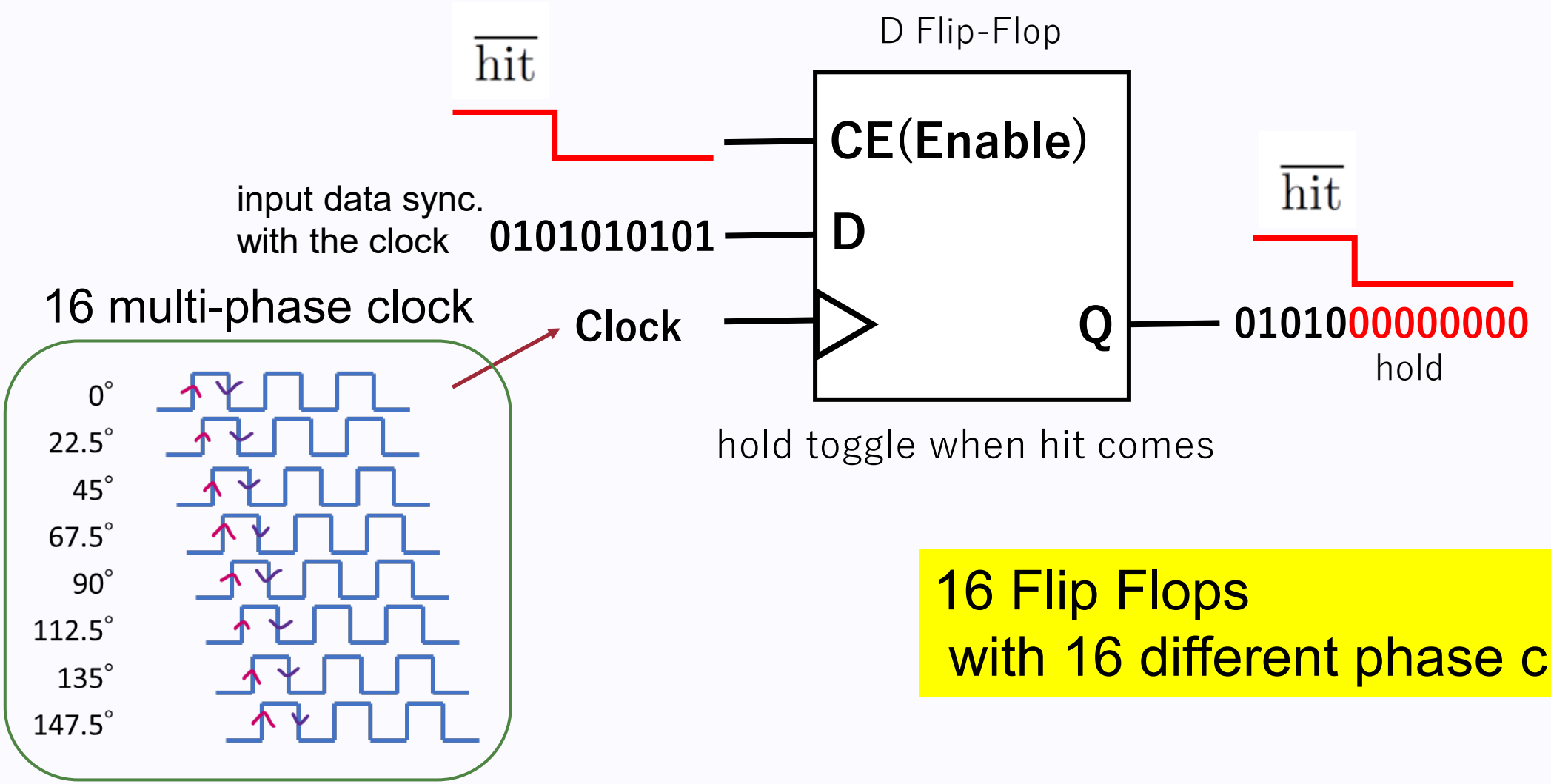
TDC Architecture

- Hit Timing = Course Timing + Fine Timing
  - Course Timing : Clock Counter
  - Fine Timing : 16 multi-phase clock TDC
    - 312.5 ps LSB or 125 ps LSB
- Output Data = Hit Timing – Trigger Timing + Offset
  - 64 TDC for hit + 1 TDC for trigger



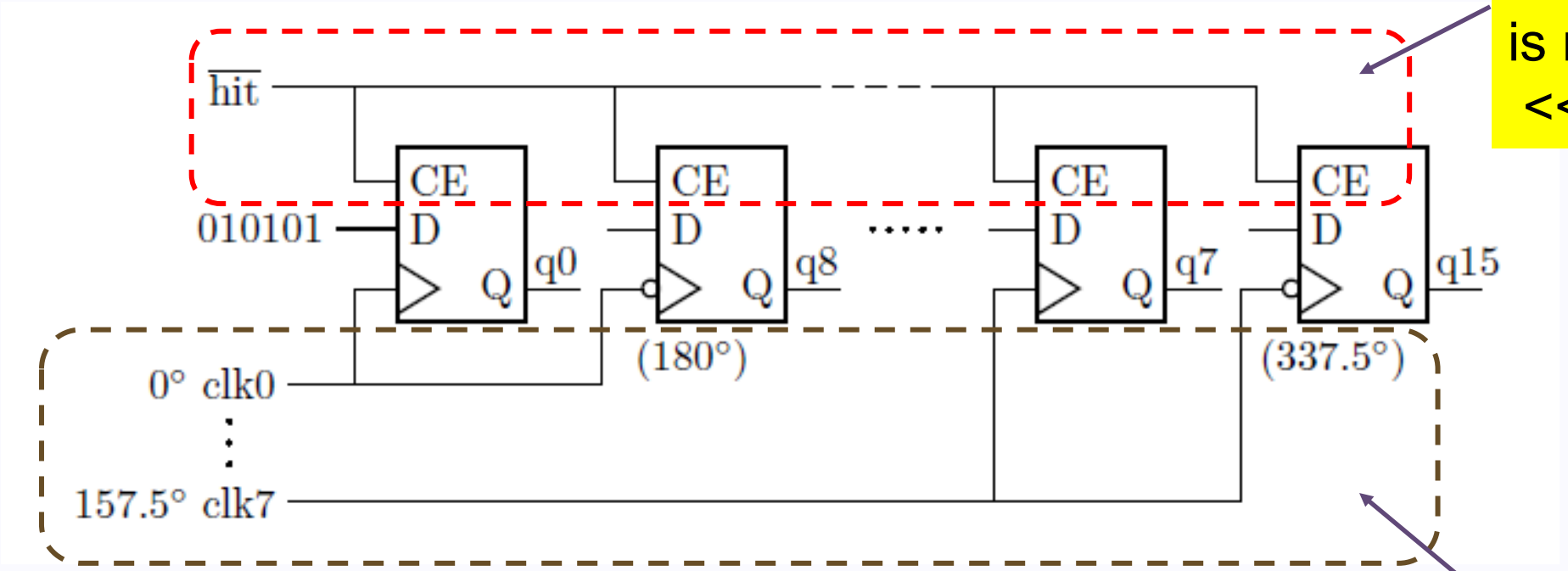
For Fine Timing

inverted hit signal for the leading-edge measurement



16 Flip Flops
with 16 different phase clocks

Fine Timing Unit

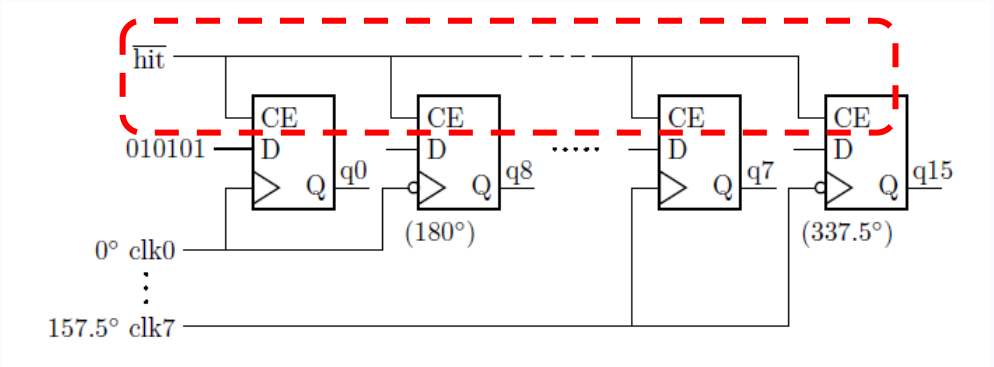


skew control is mandatory << ±125 ps

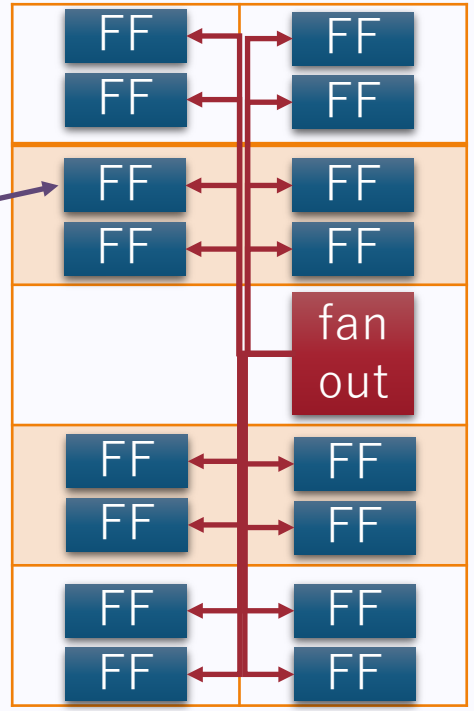
Use clock lines (should be small skew) in Artix-7

pattern will be 0000111111111111 1111000000000000 → both cases, value = “4”

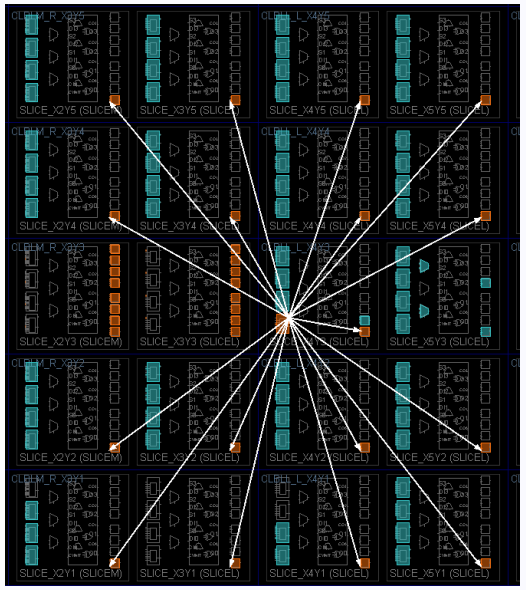
Routing by development tool (Vivado)



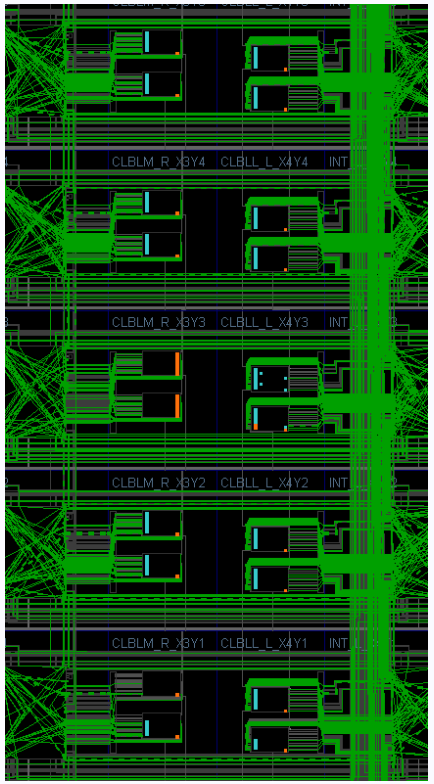
Manually fix
the placement
of the FFs



Block View

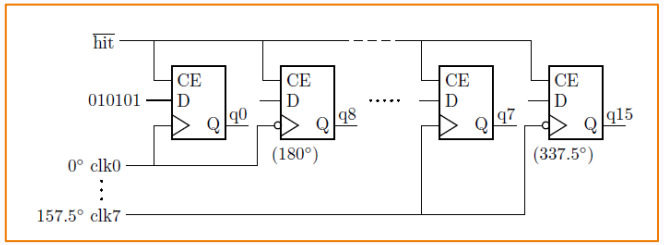


Routing View

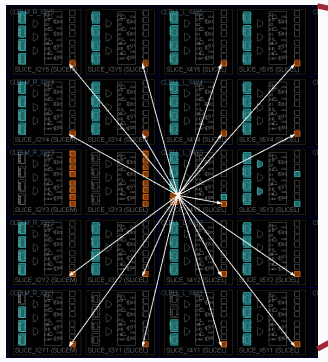


Layout

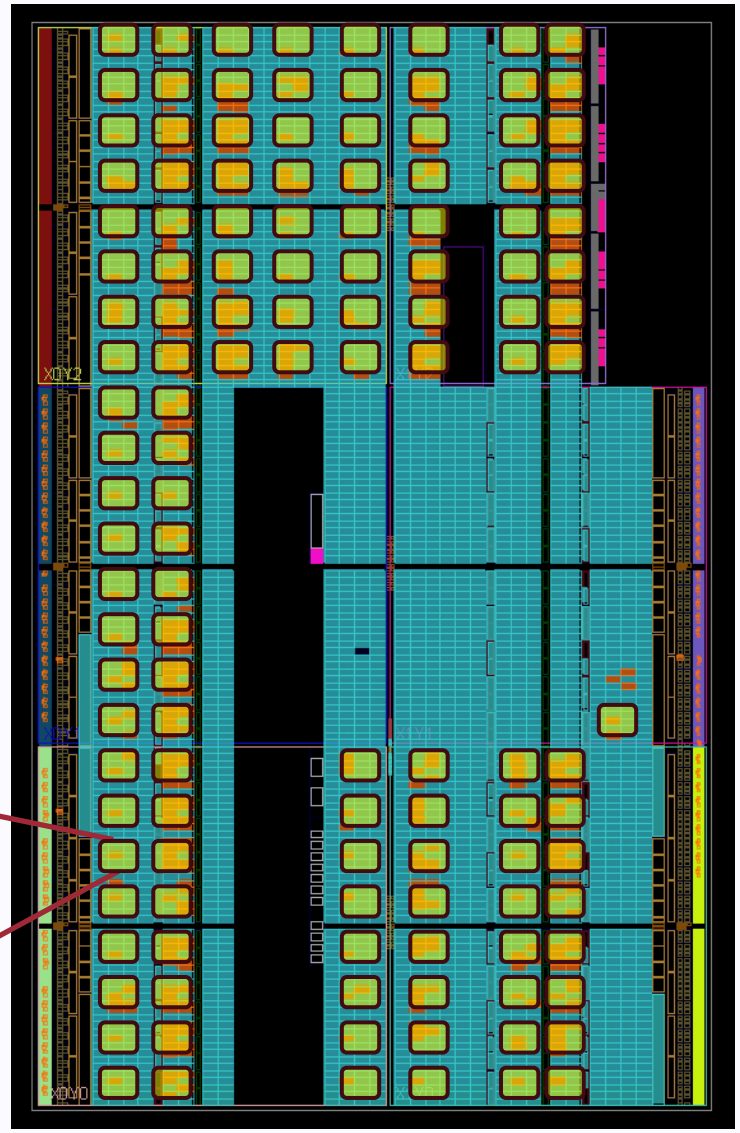
Trigger : 1 Unit
Leading edge : 64 Unit
Trailing edge : 64 Unit
(only for 312.5ps LSB version)



Fine Timing Unit



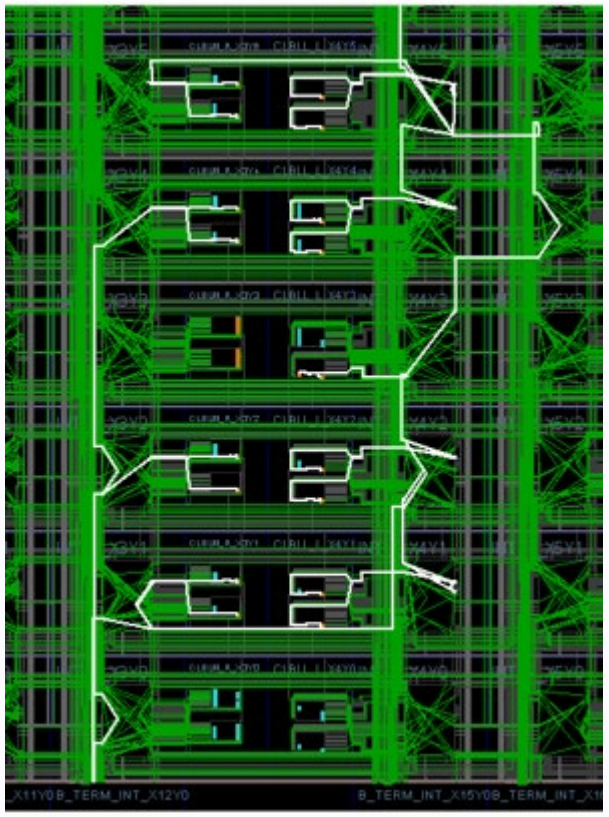
24 24 8 8 16 16 16 16 1



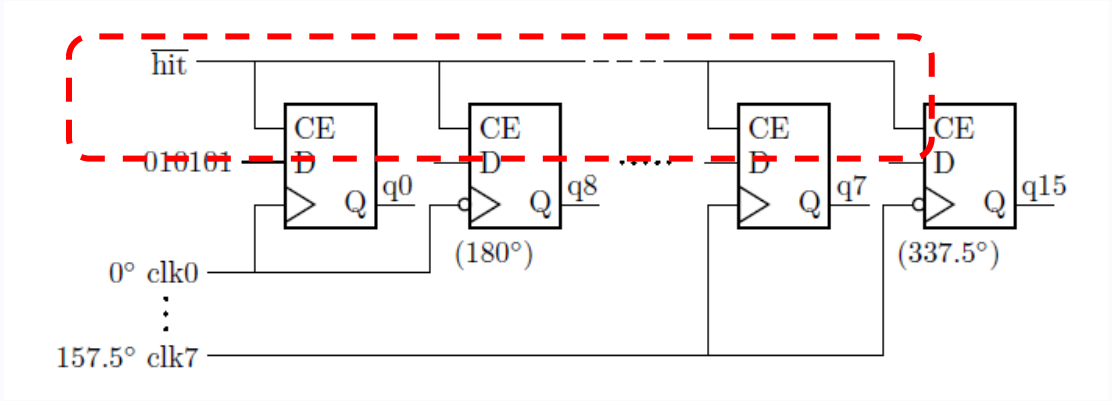
Routing by development tool (Vivado)

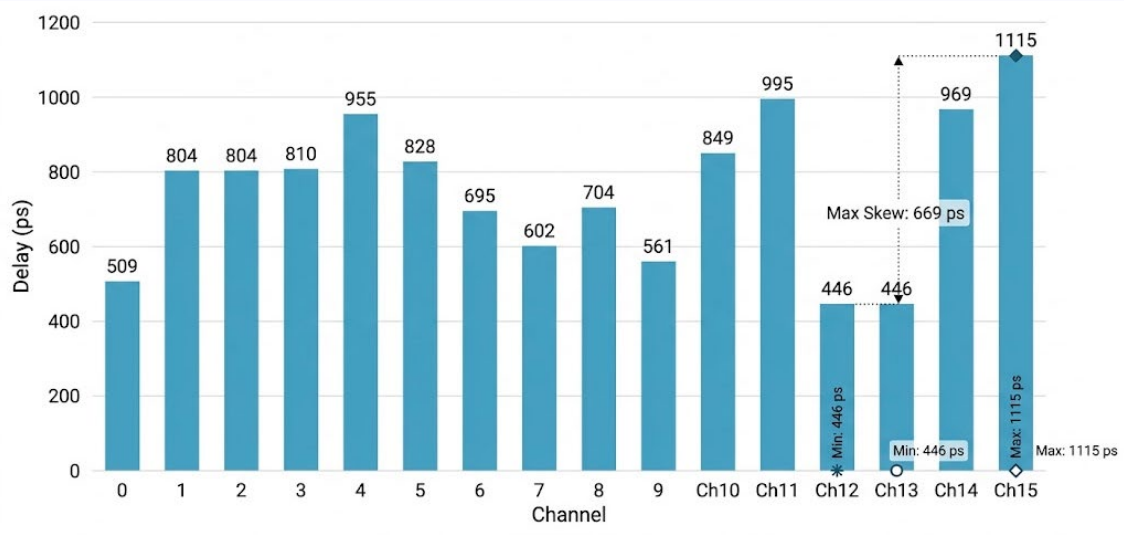
Estimated by Vivado

Auto Routing by Vivado



	Net Delay (ps)
)/U0/hgen[0].hitnfdce	599
)/U0/hgen[10].hitnfdce	804
)/U0/hgen[11].hitnfdce	804
)/U0/hgen[12].hitnfdce	810
)/U0/hgen[13].hitnfdce	955
)/U0/hgen[14].hitnfdce	828
)/U0/hgen[15].hitnfdce	685
)/U0/hgen[1].hitnfdce	602
)/U0/hgen[2].hitnfdce	704
)/U0/hgen[3].hitnfdce	561
)/U0/hgen[4].hitnfdce	849
)/U0/hgen[5].hitnfdce	995
)/U0/hgen[6].hitnfdce	446
)/U0/hgen[7].hitnfdce	446
)/U0/hgen[8].hitnfdce	969
)/U0/hgen[9].hitnfdce	1115

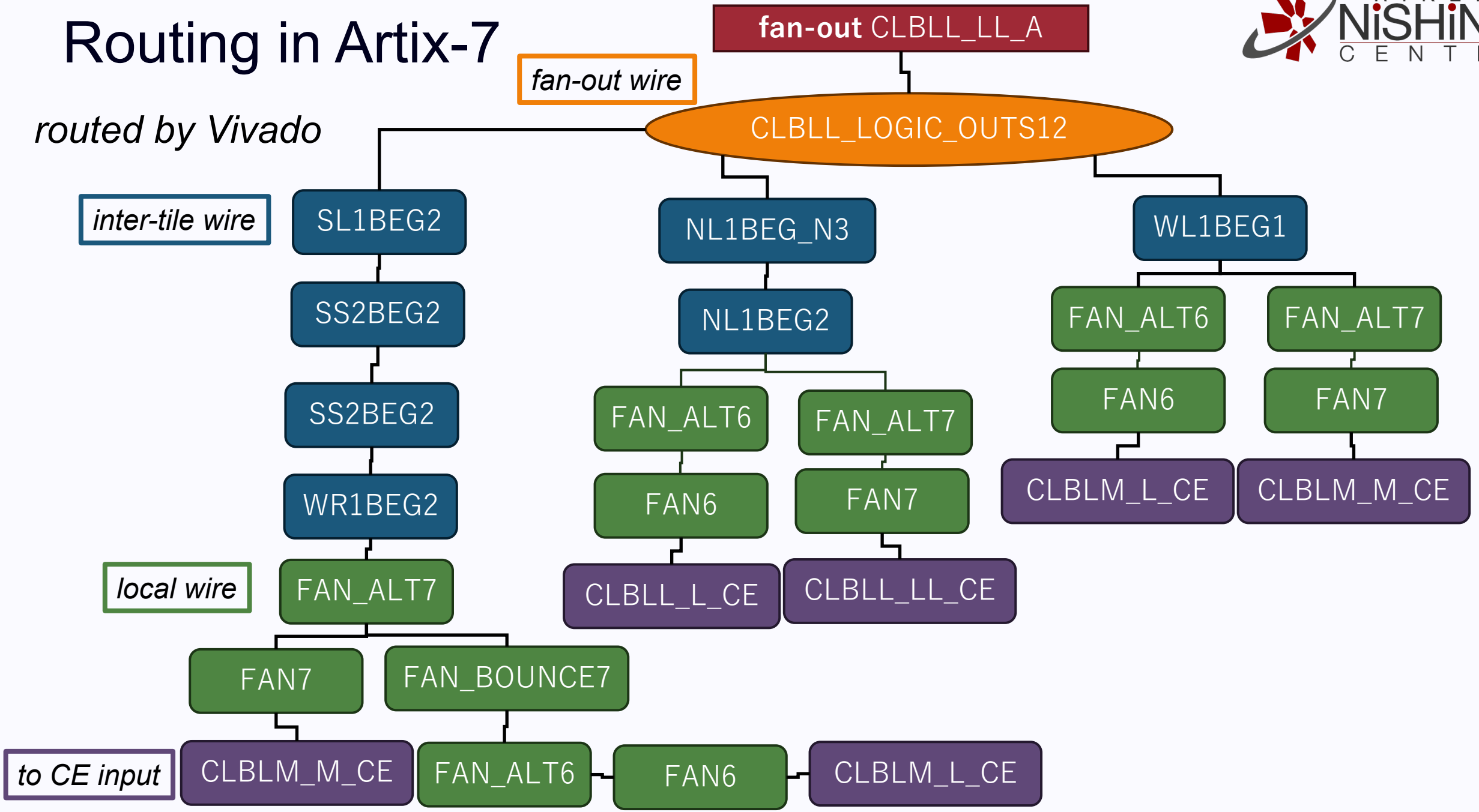




skew ±335 ps

Routing in Artix-7

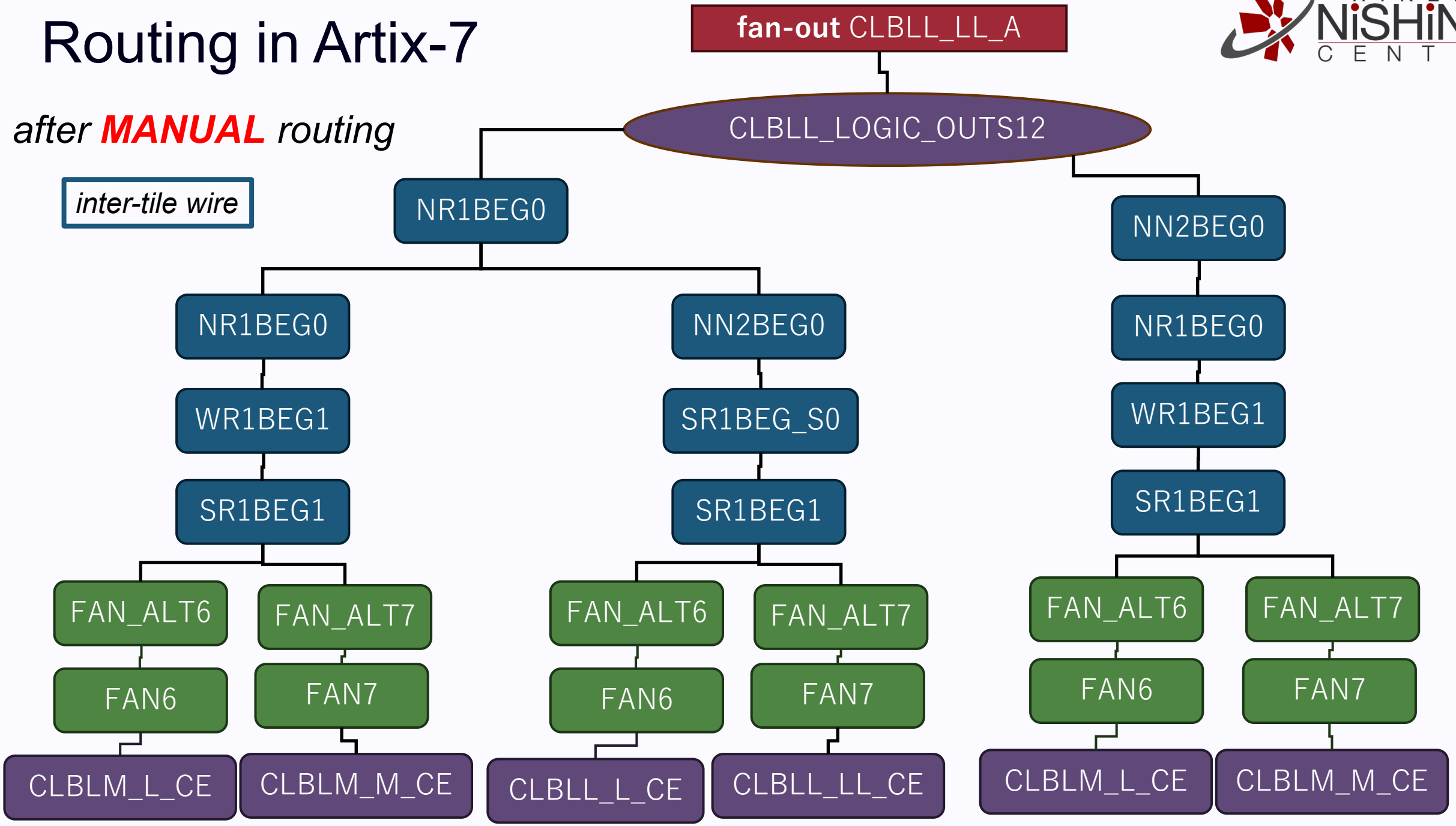
routed by Vivado



Routing in Artix-7

*after **MANUAL** routing*

inter-tile wire



Routing in Artix-7

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Vivado auto

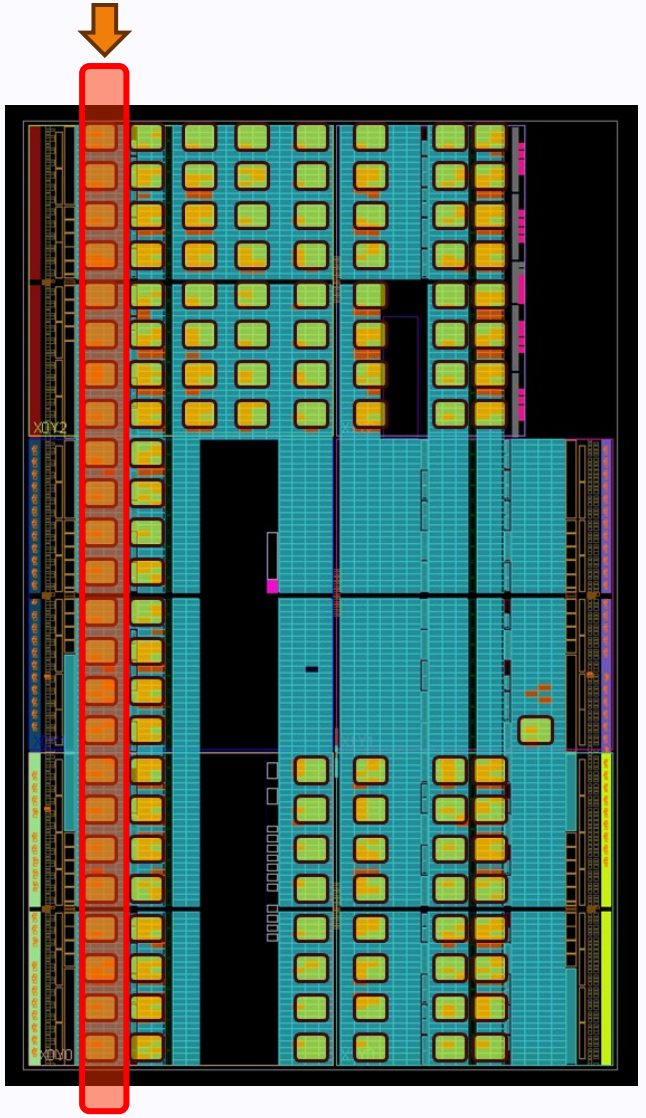
magic spell..

{ CLBLL_LL_A CLBLL_LOGIC_OUTS12 NL1BEG_N3 NL1BEG2 { FAN_ALT6 FAN_L6 CLBLL_L_CE } { FAN_ALT7 FAN_L7 CLBLL_LL_CE } NW2BEG2 { EL1BEG1 FAN_ALT6 FAN_L6 CLBLL_L_CE } { FAN_ALT6 FAN6 CLBLM_L_CE } { FAN_ALT7 FAN7 CLBLM_M_CE } NE2BEG2 { NL1BEG1 NR1BEG1 GFAN0 BYP_ALT0 BYP_L0 CLBLL_L_AX } SL1BEG2 { FAN_ALT7 FAN_L7 CLBLL_LL_CE } SL1BEG2 { SW2BEG2 { SL1BEG2 FAN_ALT7 { FAN_BOUNCE7 FAN_ALT6 FAN6 CLBLM_L_CE } FAN7 CLBLM_M_CE } SE2BEG2 { FAN_ALT7 { FAN_BOUNCE7 FAN_ALT6 FAN_L6 CLBLL_L_CE } FAN_L7 CLBLL_LL_CE } SS2BEG2 { SS2BEG2 WR1BEG2 FAN_ALT7 { FAN_BOUNCE7 FAN_ALT6 FAN6 CLBLM_L_CE } FAN7 CLBLM_M_CE } NR1BEG2 FAN_ALT7 { FAN_BOUNCE7 FAN_ALT6 FAN_L6 CLBLL_L_CE } FAN_L7 CLBLL_LL_CE } WL1BEG1 { FAN_ALT6 FAN6 CLBLM_L_CE } FAN_ALT7 FAN7 CLBLM_M_CE }

after tuning

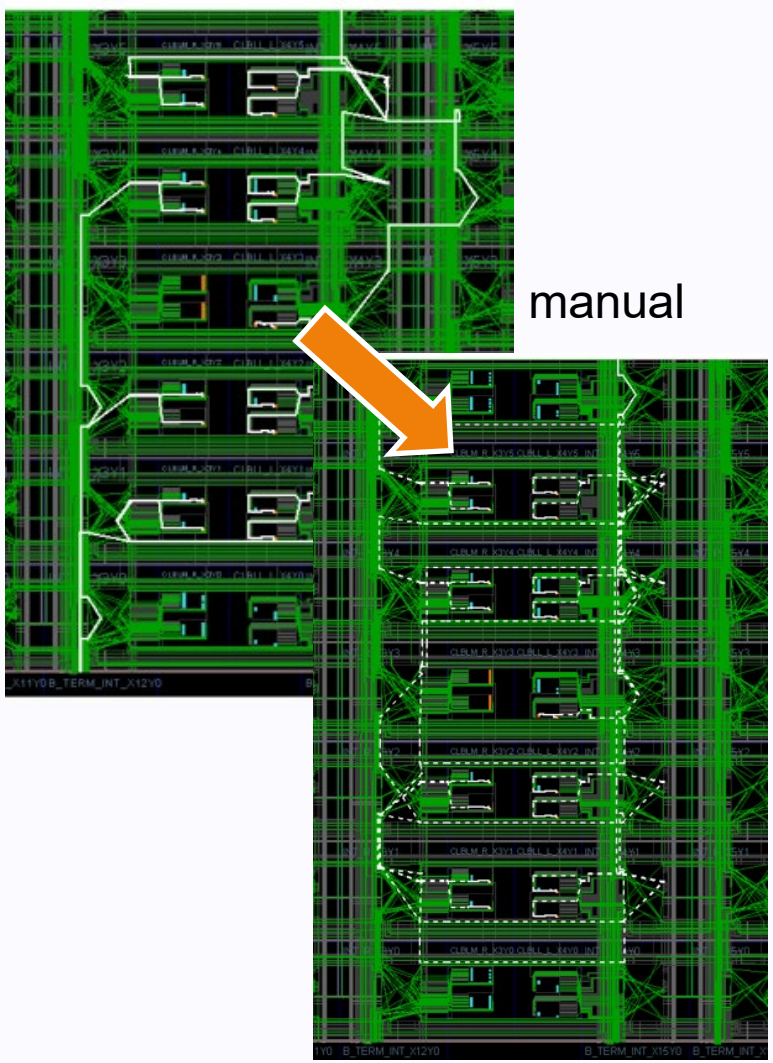
{ CLBLL_LL_A CLBLL_LOGIC_OUTS12 { NR1BEG0 { NR1BEG0 WR1BEG1 SR1BEG1 { FAN_ALT6 FAN6 CLBLM_L_CE } FAN_ALT7 FAN7 CLBLM_M_CE } NN2BEG0 SR1BEG_S0 SR1BEG1 { FAN_ALT6 FAN_L6 CLBLL_L_CE } FAN_ALT7 FAN_L7 CLBLL_LL_CE } { WL1BEG_N3 { SR1BEG_S0 SL1BEG0 ER1BEG1 { FAN_ALT6 FAN_L6 CLBLL_L_CE } FAN_ALT7 FAN_L7 CLBLL_LL_CE } NL1BEG_N3 NE2BEG3 NL1BEG2 { FAN_ALT6 FAN_L6 CLBLL_L_CE } FAN_ALT7 FAN_L7 CLBLL_LL_CE } { NN2BEG0 NR1BEG0 WR1BEG1 SR1BEG1 { FAN_ALT6 FAN6 CLBLM_L_CE } FAN_ALT7 FAN7 CLBLM_M_CE } { NW2BEG0 SR1BEG_S0 SL1BEG0 ER1BEG1 { FAN_ALT6 FAN_L6 CLBLL_L_CE } FAN_ALT7 FAN_L7 CLBLL_LL_CE } SS2BEG0 { NR1BEG0 WR1BEG1 SR1BEG1 { FAN_ALT6 FAN6 CLBLM_L_CE } FAN_ALT7 FAN7 CLBLM_M_CE } WL1BEG_N3 NL1BEG_N3 NL1BEG2 { FAN_ALT7 FAN7 CLBLM_M_CE } FAN_ALT6 FAN6 CLBLM_L_CE }

use the same routing for the same column,
finally, 9 different routing patterns were prepared



Result of Manual routing

auto



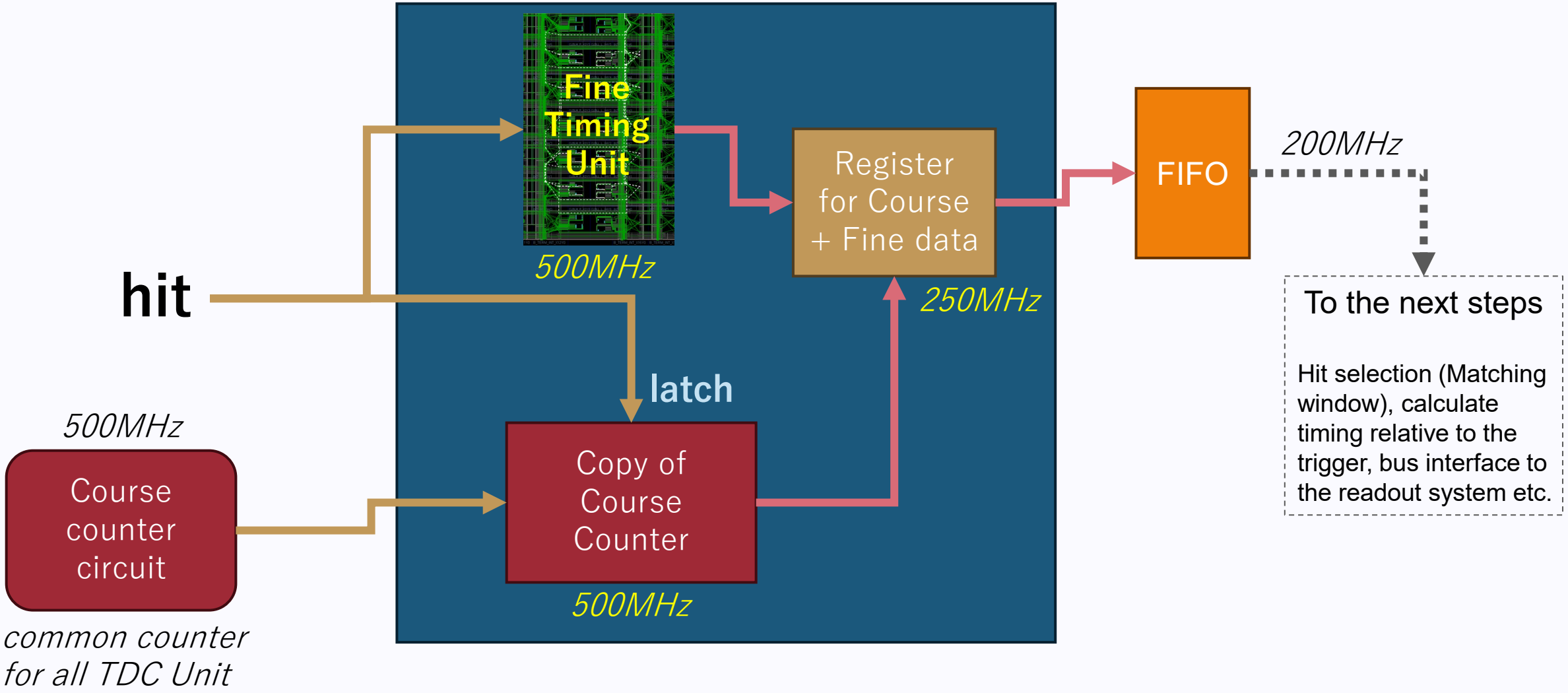
manual

Estimated by Vivado

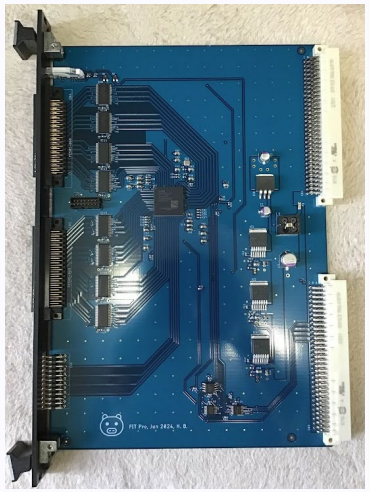
	Net Delay (ps)
)/U0/hgen[0].hitnfdce	827
)/U0/hgen[10].hitnfdce	820
)/U0/hgen[11].hitnfdce	820
)/U0/hgen[12].hitnfdce	817
)/U0/hgen[13].hitnfdce	820
)/U0/hgen[14].hitnfdce	843
)/U0/hgen[15].hitnfdce	843
)/U0/hgen[1].hitnfdce	830
)/U0/hgen[2].hitnfdce	833
)/U0/hgen[3].hitnfdce	833
)/U0/hgen[4].hitnfdce	820
)/U0/hgen[5].hitnfdce	823
)/U0/hgen[6].hitnfdce	835
)/U0/hgen[7].hitnfdce	835
)/U0/hgen[8].hitnfdce	817
)/U0/hgen[9].hitnfdce	820

Skew 669 ps → ±13 ps

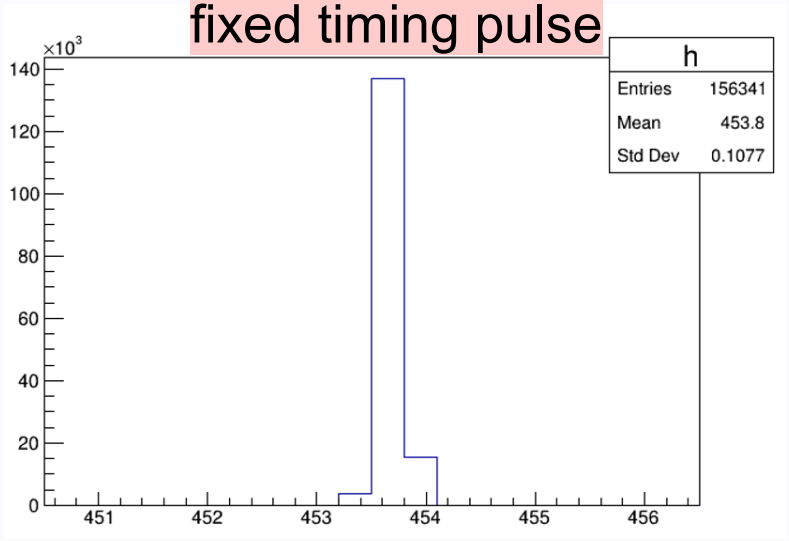
TDC Unit for 125 ps LSB TDC



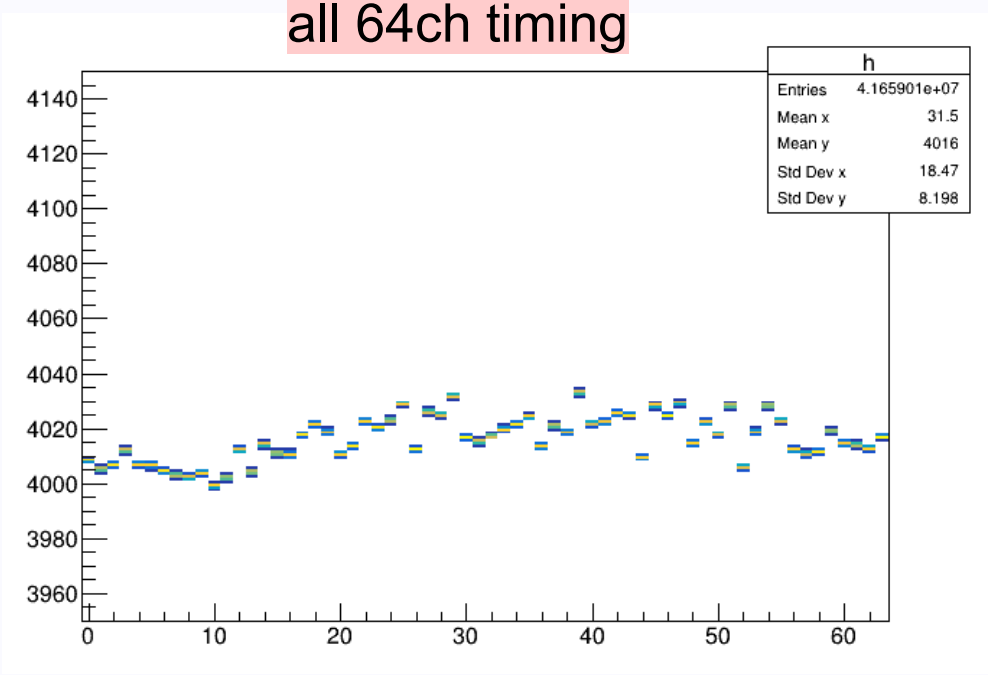
It works



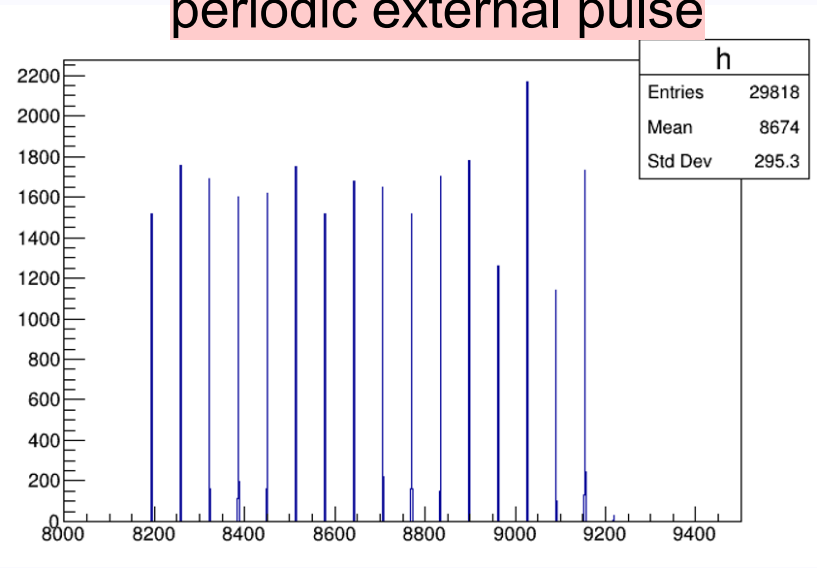
fixed timing pulse



all 64ch timing

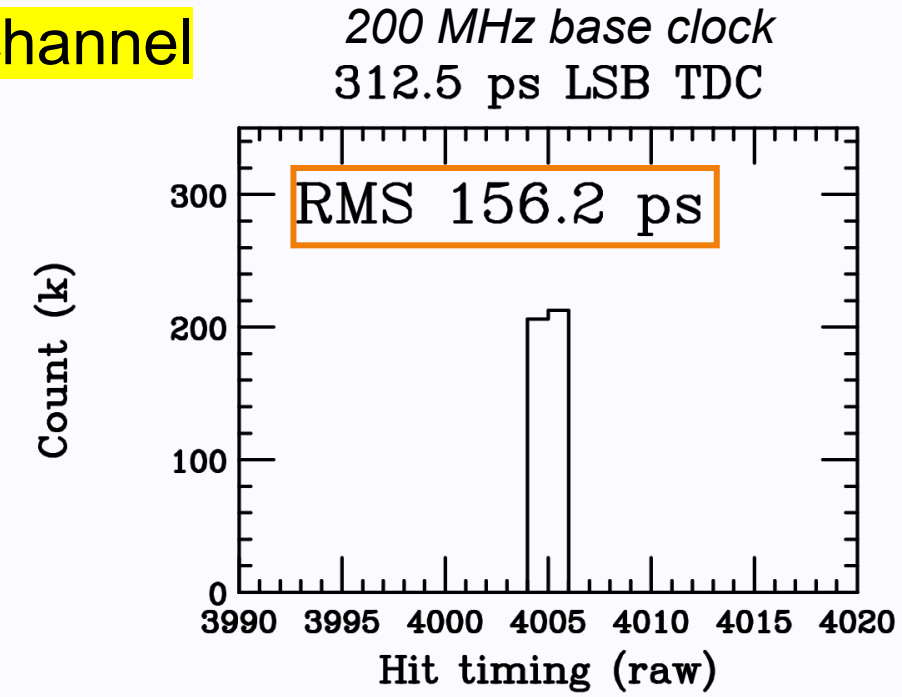


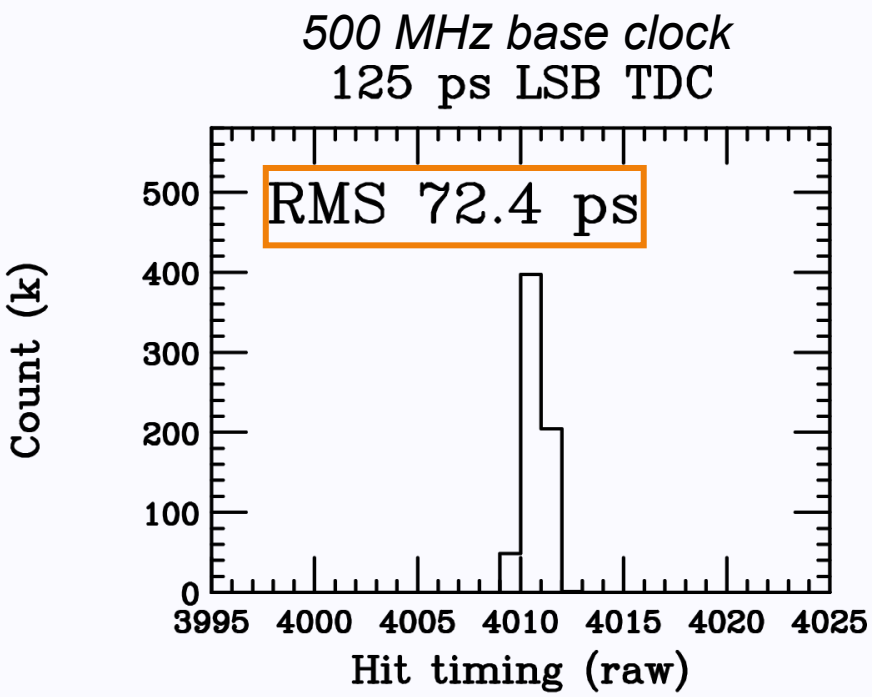
periodic external pulse

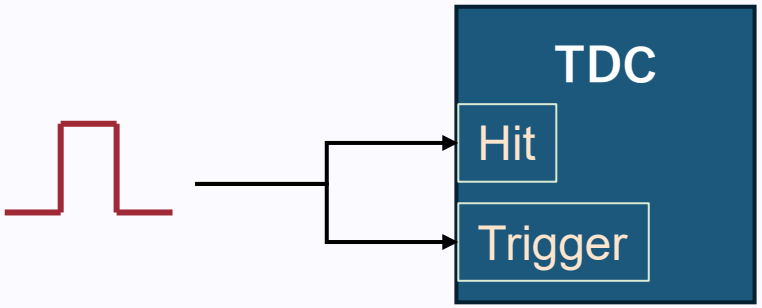


Resolution (or Precision)

worst channel





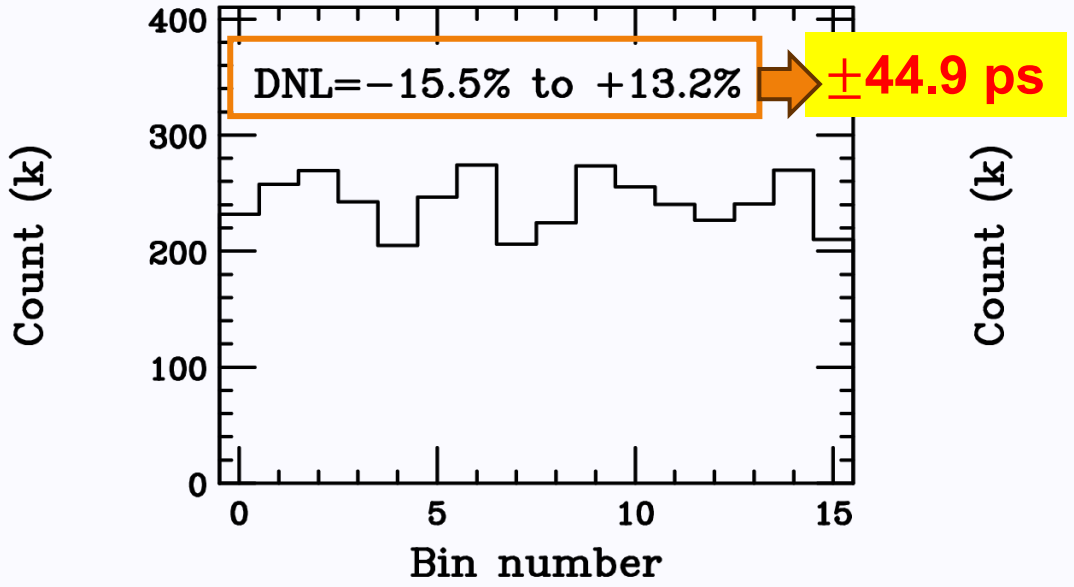


RMS(hit – trigger) = 72.4 ps
as a single TDC, RMS = 51.2 ps

DNL for Fine Timing (16 bin units)

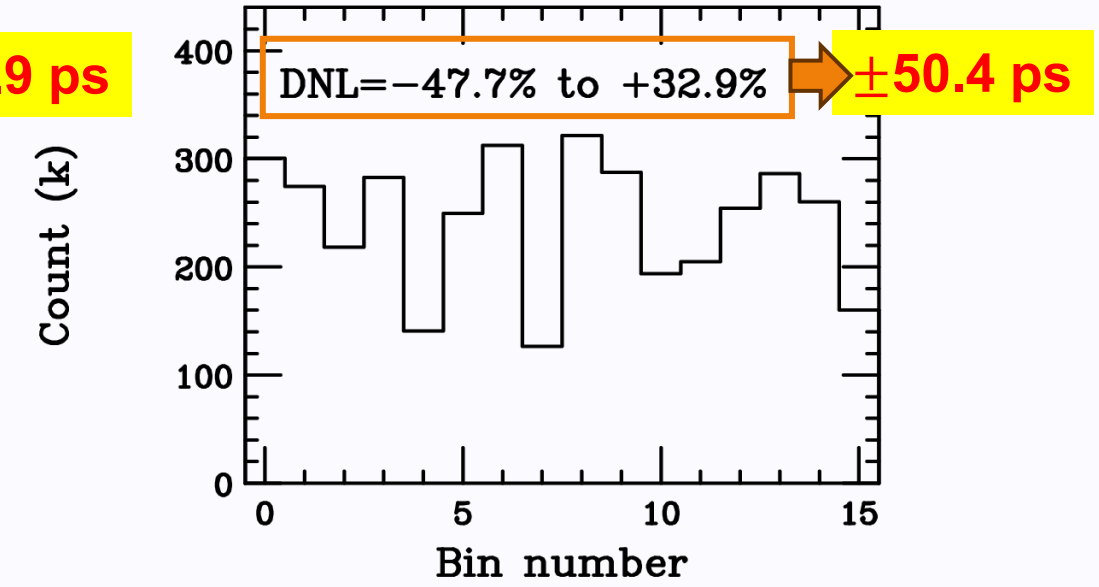
200 MHz base clock

312.5 ps TDC

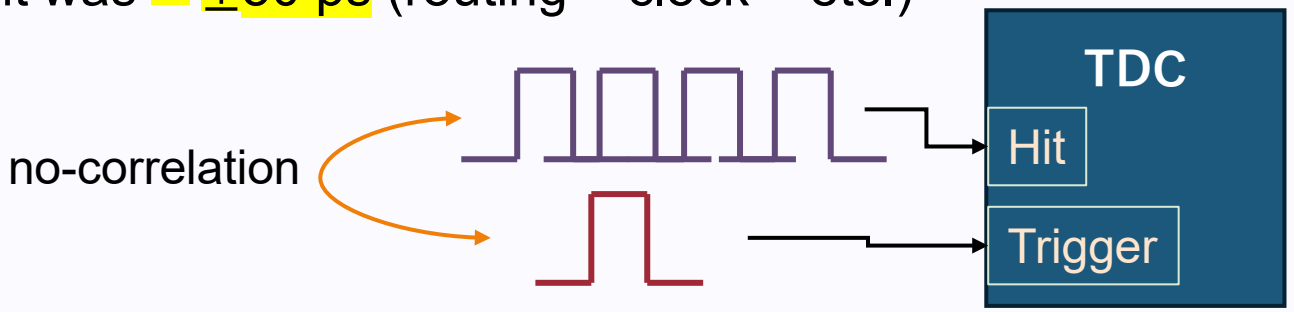


500 MHz base clock

125 ps TDC

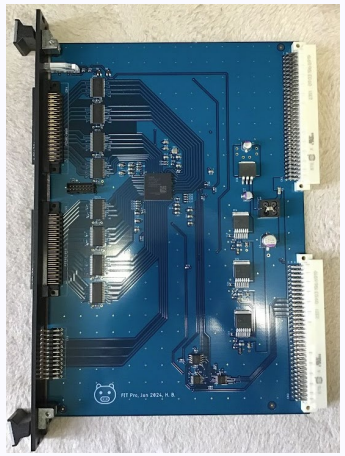


Vivado's estimation was ±13 ps (only routing skew)
measurement was ~ ±50 ps (routing + clock + etc.)

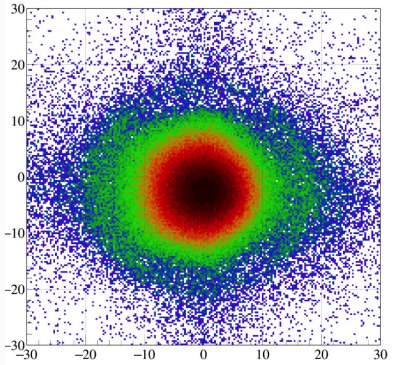


Summary

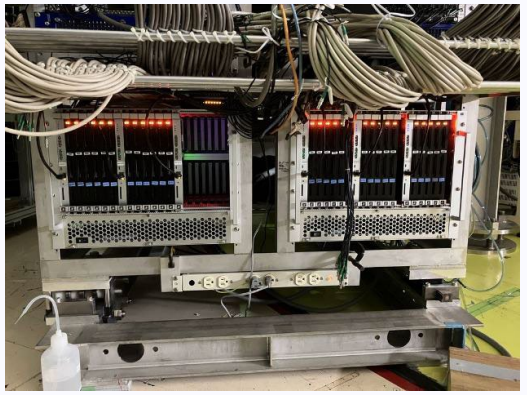
- 64 channel TDC in Artix-7 ($100)
  - 312.5 ps LSB for leading / trailing edge
    - < 156 ps (RMS)
  - 125 ps LSB for leading edge
    - < 72.4 ps (RMS)



Real experiment :
Beam tracking image
using DriftChamber

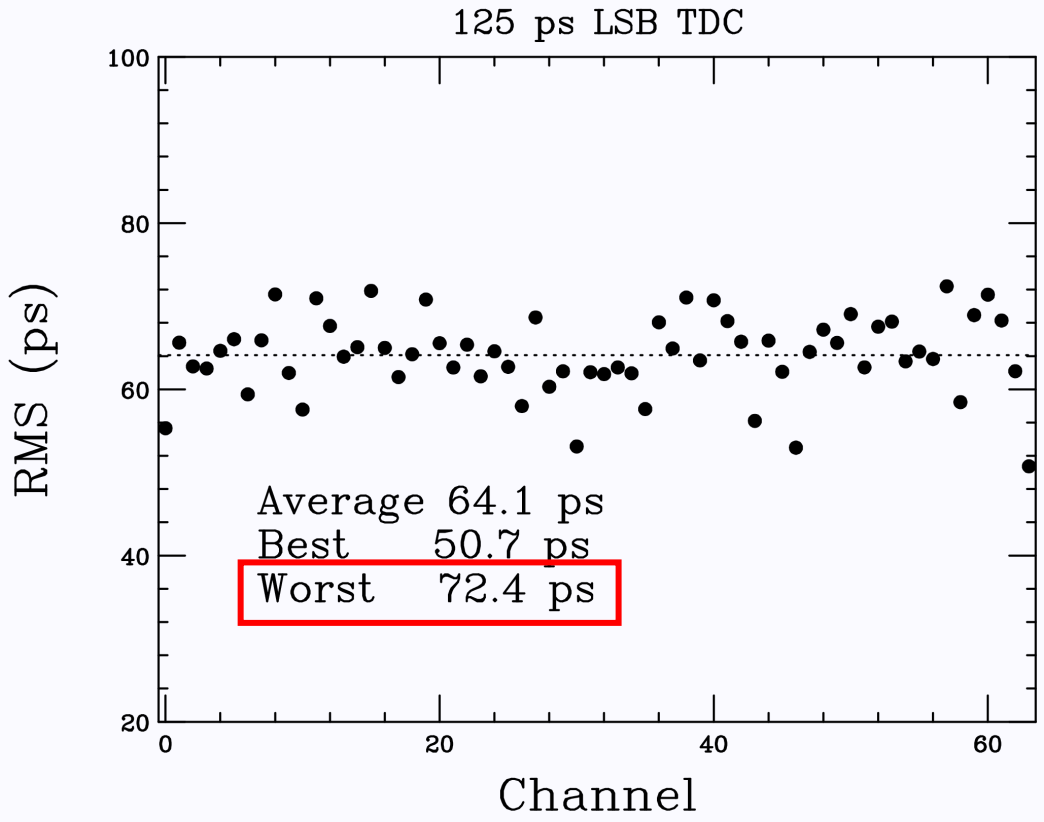


- Manual routing in FPGA
  - Can control the propagation delay
- Already successfully introduced experiments in RIBF, Japan
  - > 50 TDC modules are stably working now

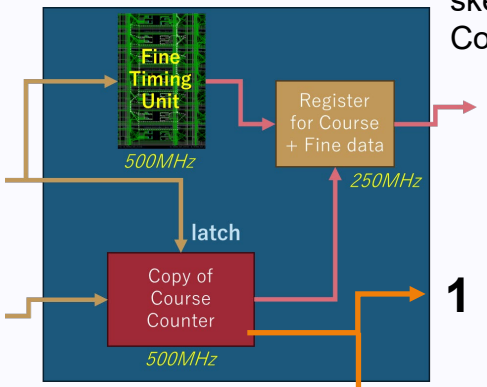


Backup

Resolution : Channel Variations

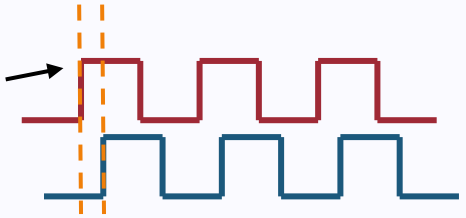


Aliment of Course clock and Fine timing



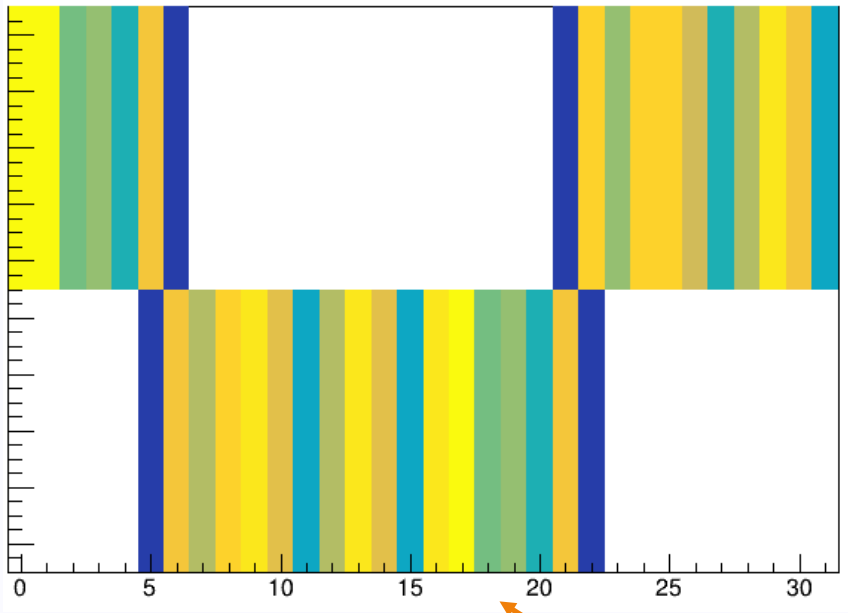
LSB of Course Counter

skew between Course and Fine



Clock for Course

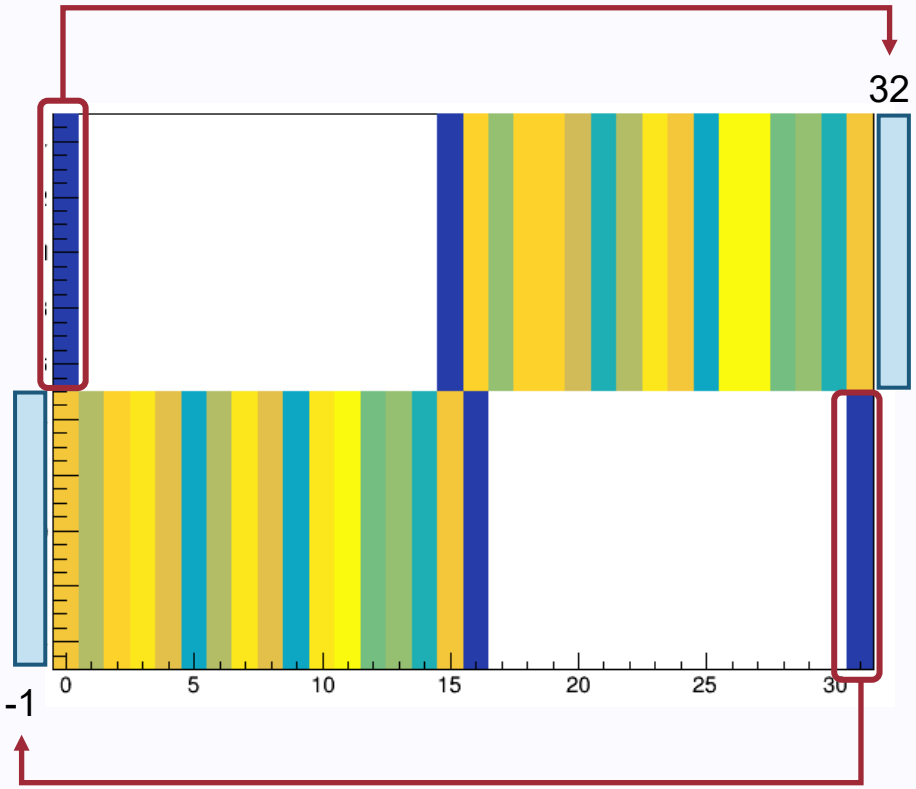
Clock for Fine



for tuning purpose

Aliment in FPGA

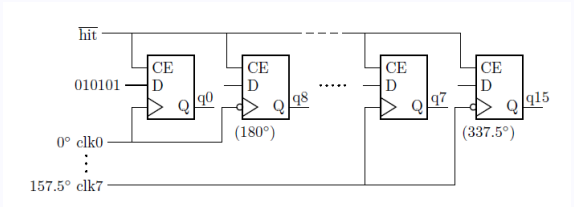
add “26”



value=“4”

000011111111111 → 20

111100000000000 → 4

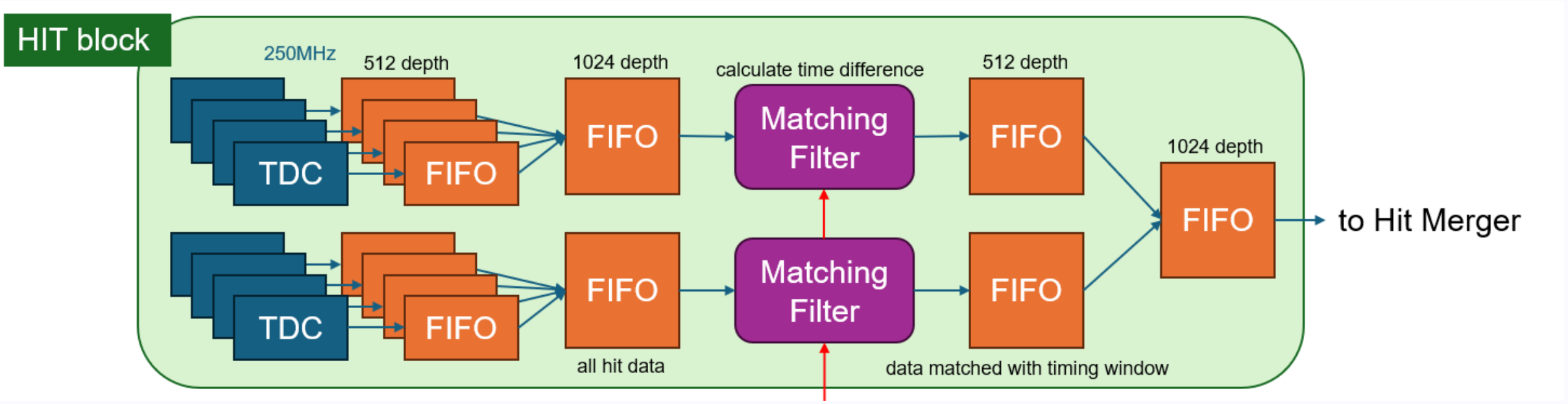


Due to small independent jitter, additional correction is required for specific combinations.

hit input limitation

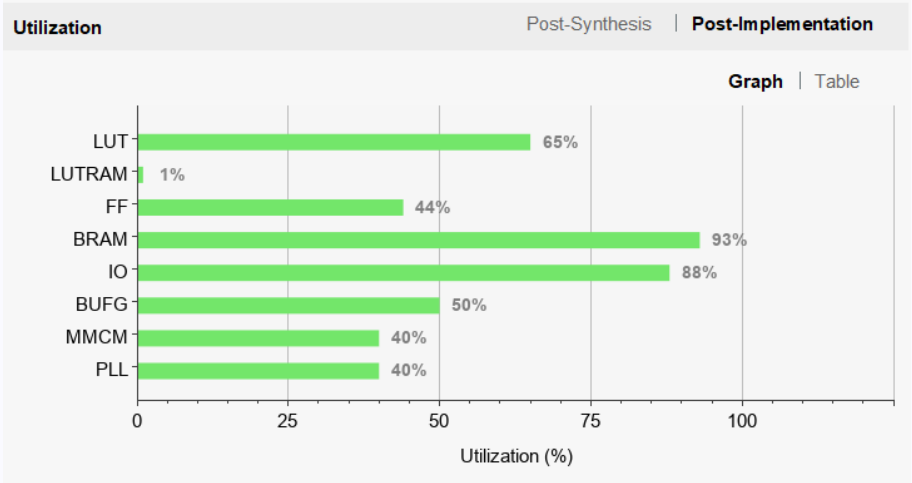
- 25MHz hit / 4 channel
  - merge 4xFIFO to one FIFO
  - procedure in the matching filter

  - leading + trailing edge case, 12.5MHz hit / 4 channel



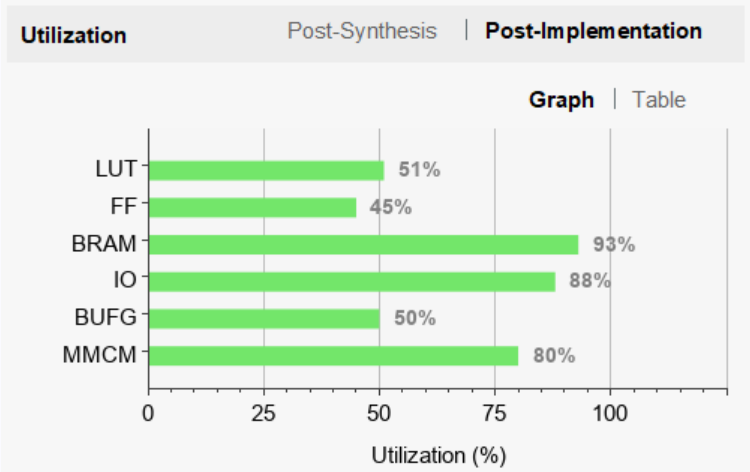
Vivado Resource Usage

312.5 ps LSB TDC



Name	Slice LUTs	Slice Registers (65200)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (32600)	LUT as Memory (9600)	Block RAM Tile (75)
FITMOCO_wrapper	21187	28569	1015	2	8132	21186	1	69.5
FITMOCO_i (FITMOCO)	21187	28569	1015	2	8132	21186	1	69.5
HITGRL_3 (HITGRL_ins	2525	3371	120	0	1090	2525	0	8
HITMatch_1 (HITGRI	182	150	0	0	92	182	0	0
HITMatch_0 (HITGRI	182	150	0	0	99	182	0	0
HITBIT_5 (HITGRL_i	180	215	15	0	138	180	0	0
U0 (HITBIT_1526)	180	215	15	0	138	180	0	0
HITBIT_4 (HITGRL_i	180	215	15	0	105	180	0	0
HITBIT_3 (HITGRL_i	180	215	15	0	132	180	0	0
HITBIT_1 (HITGRL_i	180	215	15	0	133	180	0	0
HITBIT_0 (HITGRL_i	180	215	15	0	109	180	0	0
HITBIT_7 (HITGRL_i	179	215	15	0	129	179	0	0
HITBIT_6 (HITGRL_i	179	215	15	0	128	179	0	0
HITBIT_2 (HITGRL_i	179	215	15	0	119	179	0	0

125 ps LSB TDC

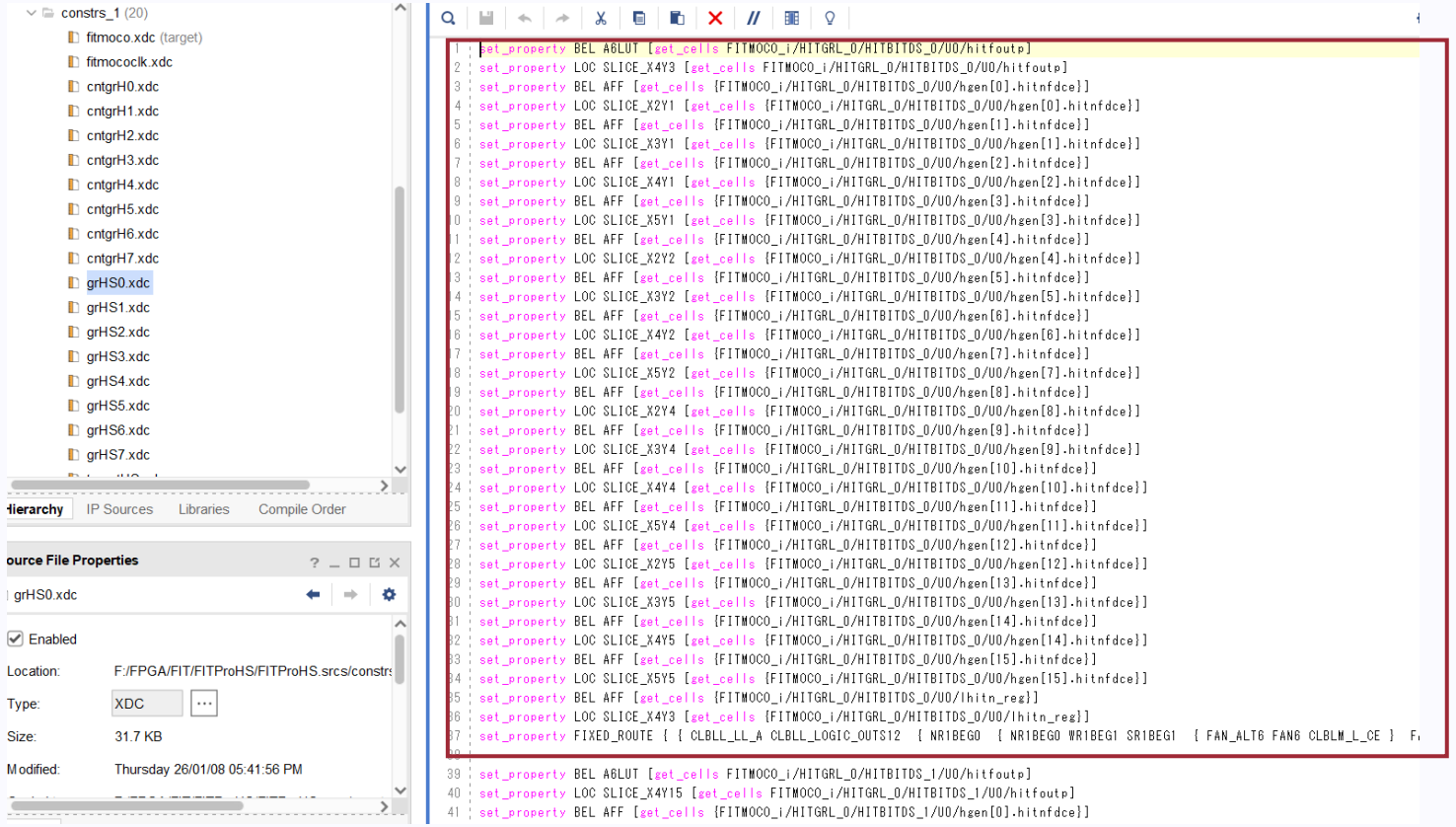


Name	Slice LUTs	Slice Registers (65200)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (32600)	Block RAM Tile (75)
FITMOCO_wrapper	16658	29215	33	2	7981	16658	69.5
FITMOCO_i (FITMOCO)	16658	29215	33	2	7981	16658	69.5
HITGRL_2 (HITGRL_ins	1914	3462	0	0	1015	1914	8
HITMatchD_0 (HITGI	180	148	0	0	76	180	0
HITMatchD_1 (HITGI	179	148	0	0	90	179	0
fifo_generator_h3 (HI	81	183	0	0	51	81	0.5
fifo_generator_h1 (HI	81	183	0	0	55	81	0.5
fifo_generator_h5 (HI	80	183	0	0	51	80	0.5
fifo_generator_h7 (HI	79	183	0	0	51	79	0.5
fifo_generator_h4 (HI	79	183	0	0	52	79	0.5
fifo_generator_h0 (HI	79	183	0	0	48	79	0.5
fifo_generator_h6 (HI	78	183	0	0	53	78	0.5
fifo_generator_h2 (HI	78	183	0	0	48	78	0.5
HITBITDS_4 (HITGR	74	144	0	0	75	74	0
U0 (HITBITDS_20	74	144	0	0	75	74	0
HITBITDS_0 (HITGR	74	144	0	0	74	74	0
HITBITDS_7 (HITGR	73	144	0	0	76	73	0
HITBITDS_6 (HITGR	73	144	0	0	76	73	0
HITBITDS_5 (HITGR	73	144	0	0	60	73	0
HITBITDS_3 (HITGR	73	144	0	0	66	73	0
HITBITDS_2 (HITGR	73	144	0	0	64	73	0
HITBITDS_1 (HITGR	73	144	0	0	75	73	0

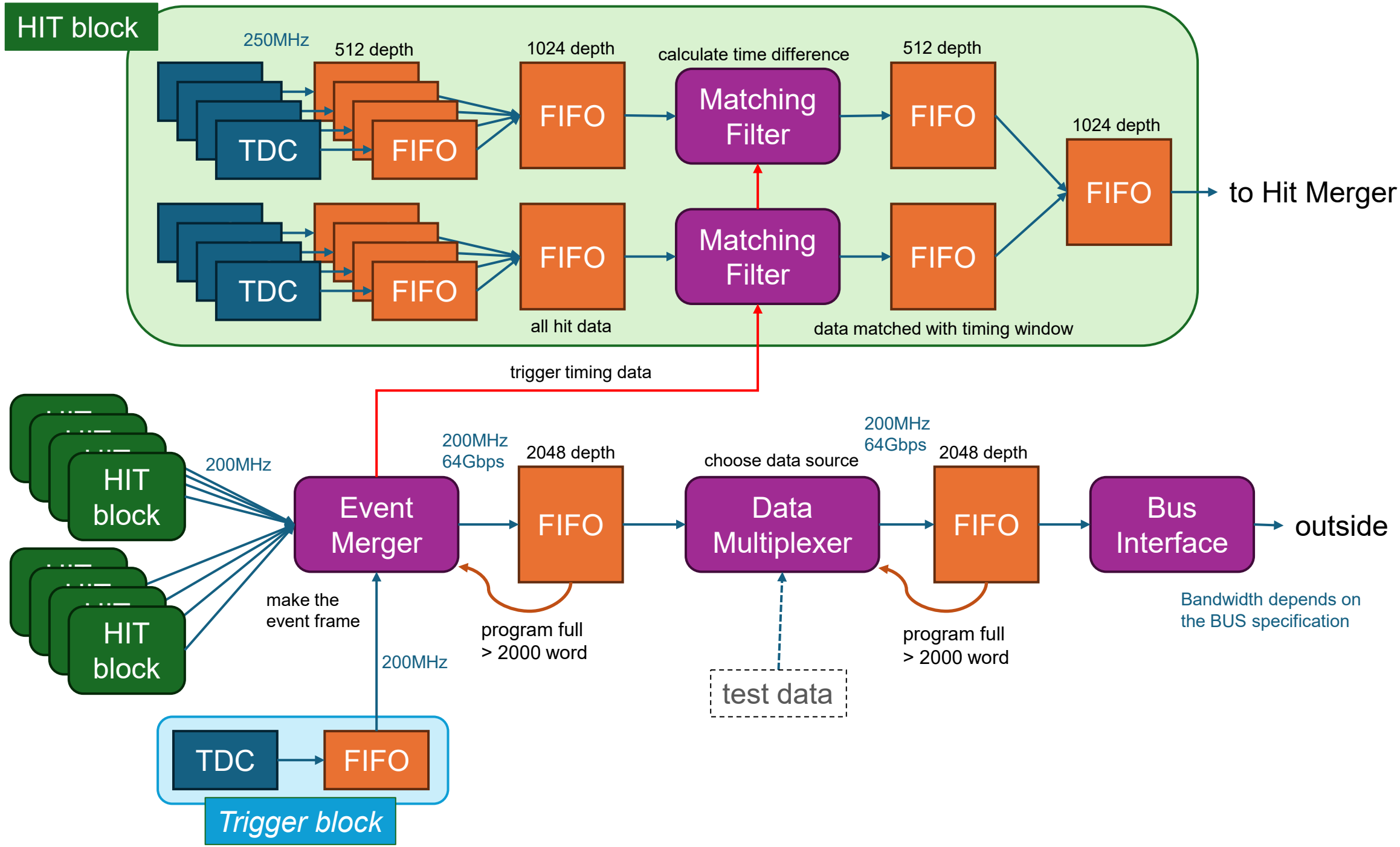
Constraint for Vivado

For routing, the same constraint is applied for both 312.5 and 125 ps LSB TDC

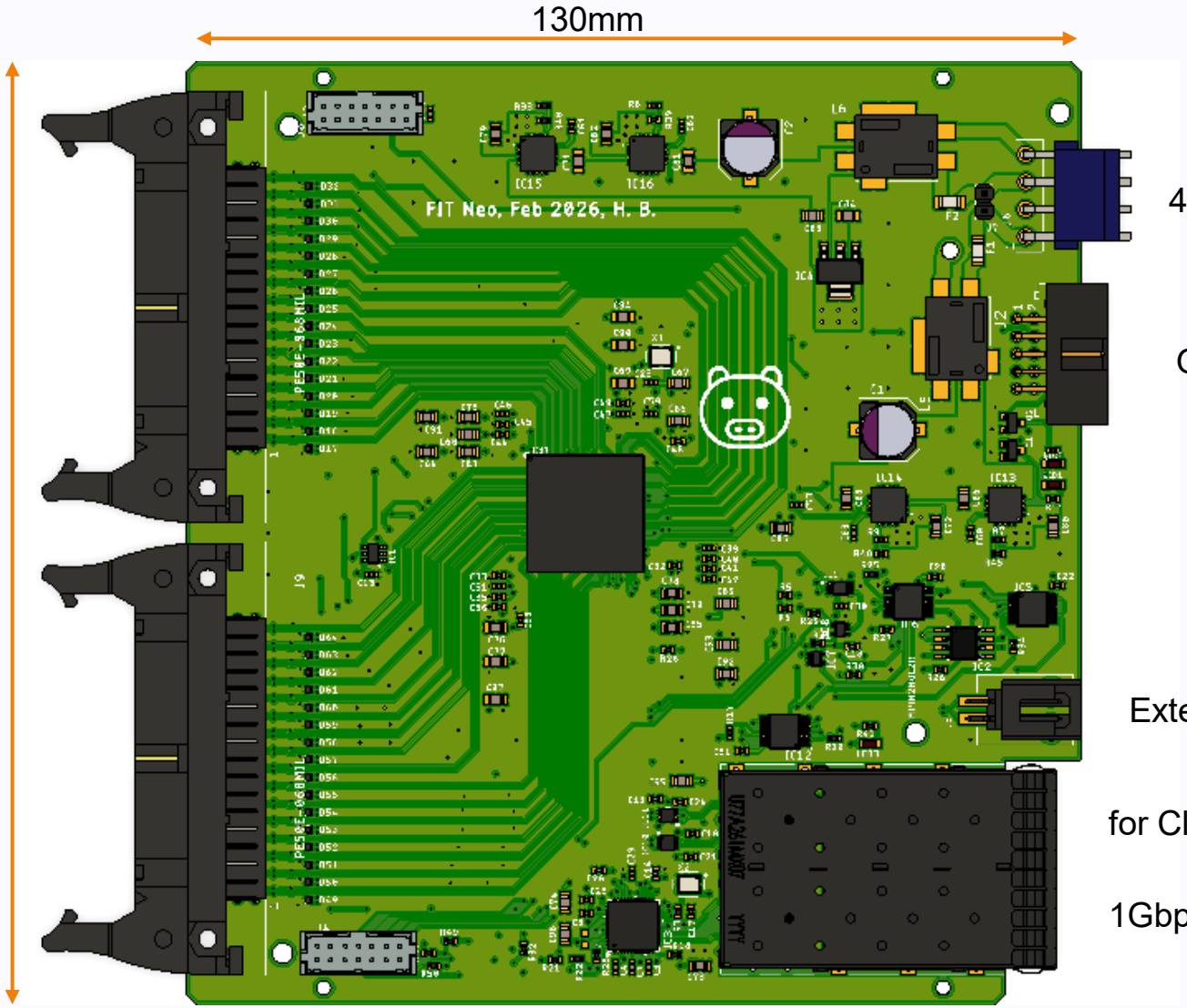
1 Fine Block



- 312.5 ps LSB TDC
  - 9166 lines
  - 64ch leading + 64ch trailing + 1ch trigger
- 125 ps LSB TDC
  - 6826 lines
  - 64ch leading + 1ch trigger


HIT block
250MHz
512 depth
1024 depth
calculate time difference
512 depth
1024 depth
TDC
FIFO
FIFO
Matching Filter
FIFO
FIFO
to Hit Merger
TDC
FIFO
FIFO
Matching Filter
FIFO
all hit data
data matched with timing window
trigger timing data
HIT block
200MHz
200MHz 64Gbps
2048 depth
choose data source
200MHz 64Gbps
2048 depth
Event Merger
FIFO
Data Multiplexer
FIFO
Bus Interface
outside
HIT block
make the event frame
program full > 2000 word
program full > 2000 word
Bandwidth depends on the BUS specification
200MHz
test data
TDC
FIFO
Trigger block

Ethernet version
of the TDC



32ch
LVDS
input

32ch
LVDS
input

4V & 2V (or 5V only)

GPIO

External trigger

for Clock synchronization / Serial link

1Gbps Ethernet