25th IEEE Real Time Conference | Oral presentation

Cost-effective and competitive alternative to the ITER time communication network for accurate time synchronization

From the validated MITICA TCN to a compact Kria-based all-in-one prototype

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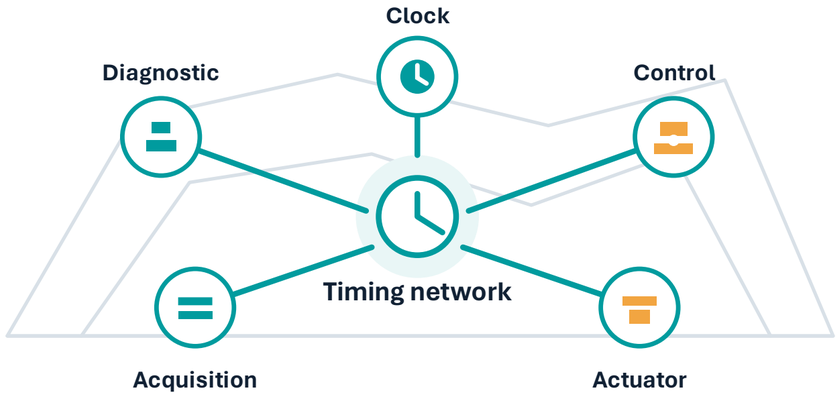
La Biodola, Isola d'Elba | May 25-29, 2026

Why timing matters in ITER/NBTF

Distributed control and acquisition only work if every node agrees on time.

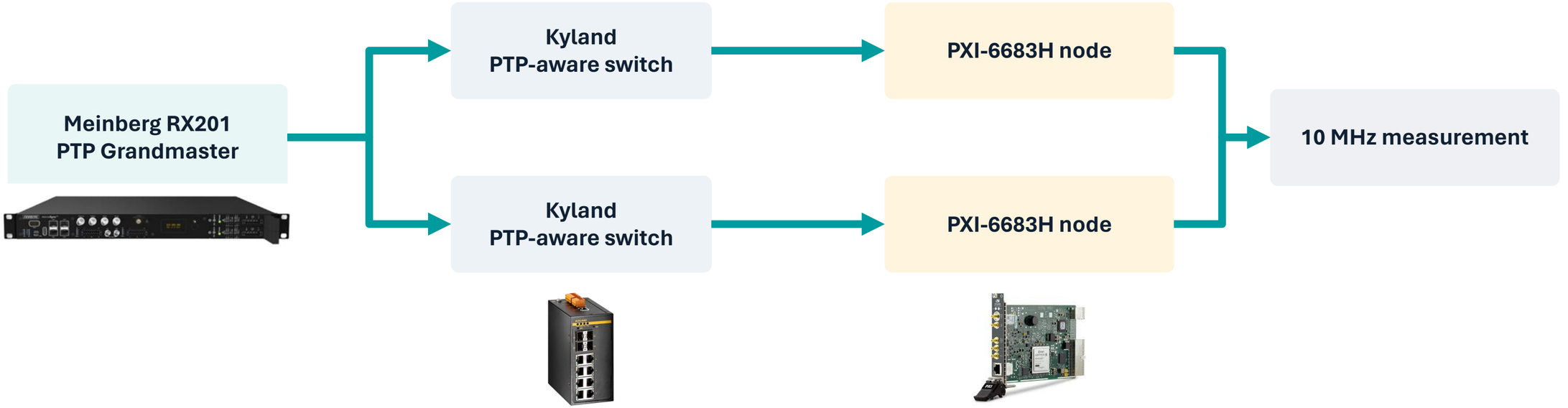
- Diagnostics and controls are geographically distributed across the facility.
- Clock and trigger coherence are required for reproducible acquisition and event timing.
- IEEE 1588/PTPv2 lets timing travel through the same network class used by the control system.



The Timing Communication Network (TCN) is not infrastructure decoration, it is a crucial part of the measurement chain.

Baseline: the MITICA TCN has been already validated

The new prototype starts from a trusted reference, not from a blank page.

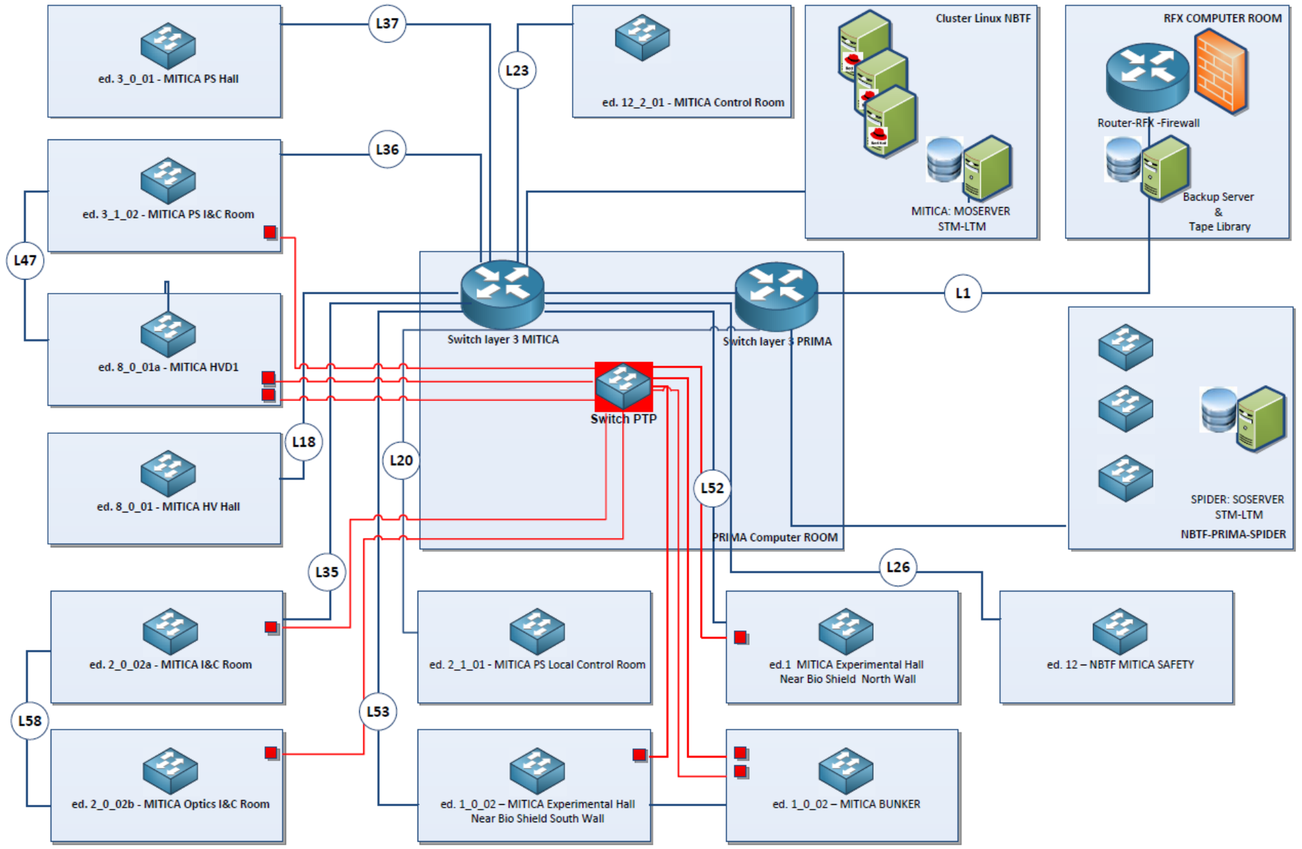


Previous MITICA campaigns showed that the ITER architecture based on PTP-aware network equipment and NI timing modules satisfies the ITER RMS requirement. (< 50ns)

https://doi.org/10.1109/TNS.2023.3237003

MITICA TCN Topology

- Distributed over 6 different buildings
- Core layer: PTP Grand Master Clock connected via Ethernet TCP to 2 PTP switches
- 9 PTP boundary clock switches connected va fiber optics to guarantee the synchronization to the connected leaves
- Segregated traffic though different VLANs
- No redundancy



The reference node works, but it is challenging to scale

The question is whether the timing function can be compressed into one embedded platform.

Standard ITER-like node

CODAC server

NI chassis

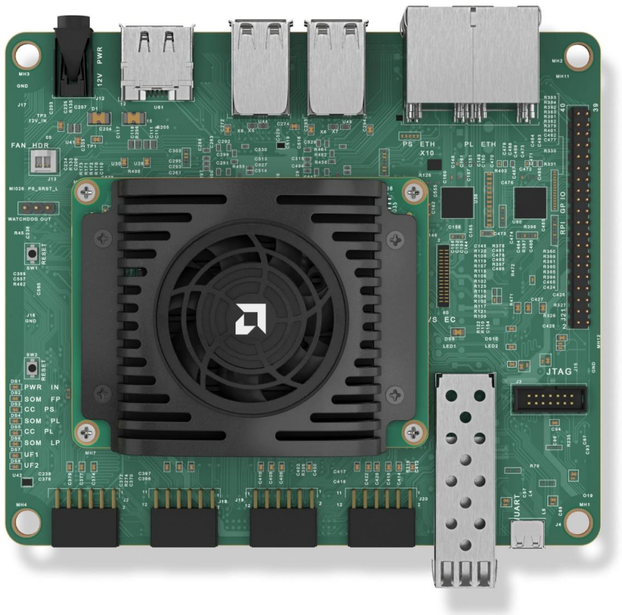
PXI-6683H module

High-end hardware, custom integration, high per-node cost

Can one FPGA-based board generate synchronized clocks and triggers while staying inside ITER-like PTP constraints?

This is the design target for the Kria prototype.

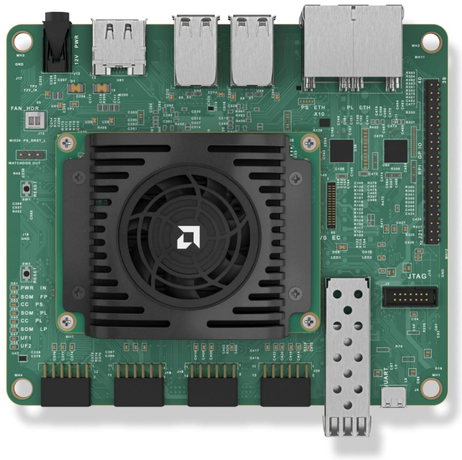
Kria KR260 all-in-one timing node



- Zynq™ UltraScale+™ MPSoC EV (XCK26)
- 256K logic cells, 1.2K DSP slices, 144 Block RAM, 64 UltraRAM
- 4 GB DDR4 non-ECC + 512 Mb QSPI boot memory
- 4× Gigabit Ethernet + 1× 10G SFP+ for deterministic industrial networking
- 4× USB 3.0, DisplayPort 1.2a, SLVS-EC vision interface

Kria KR260 all-in-one timing node

ARM/Linux handles PTP; FPGA fabric generates deterministic timing outputs.



PTP network → **ARM / Linux LinuxPTP** → **FPGA fabric Clock synchronization logic** → **Synchronized clocks + triggers outputs**

PetaLinux environment tailored to the board

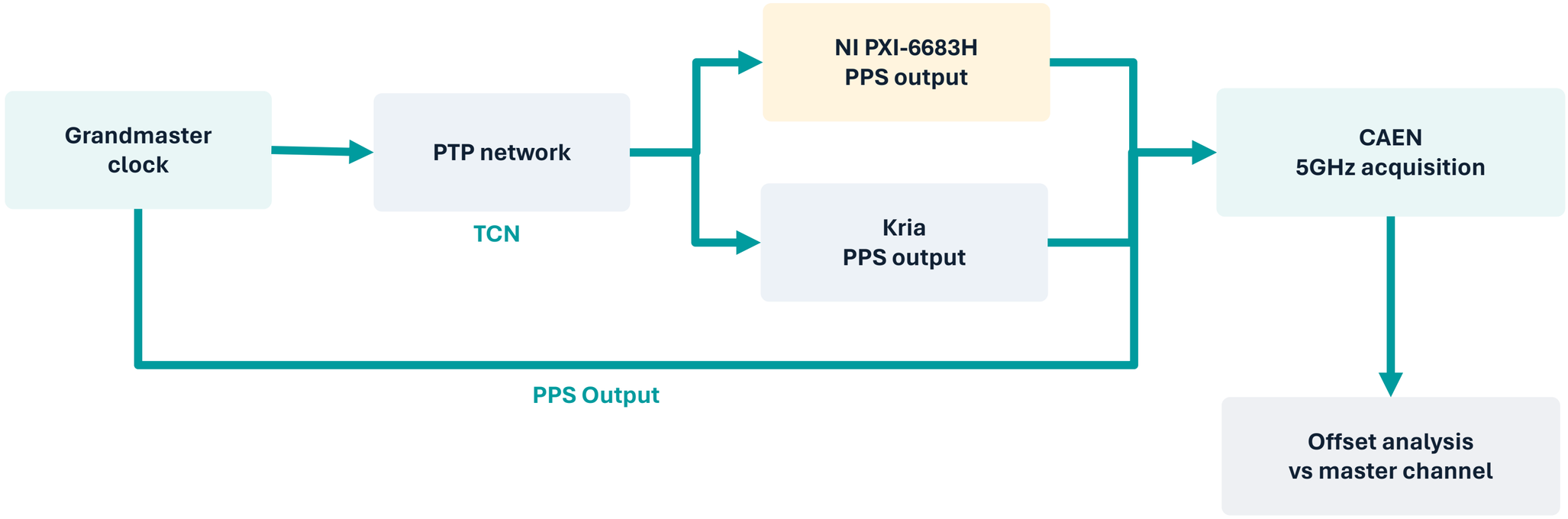
External clock lock and configurable FPGA outputs

Open software stack keeps the prototype tunable

Goal: one compact node instead of server + chassis + timing module.

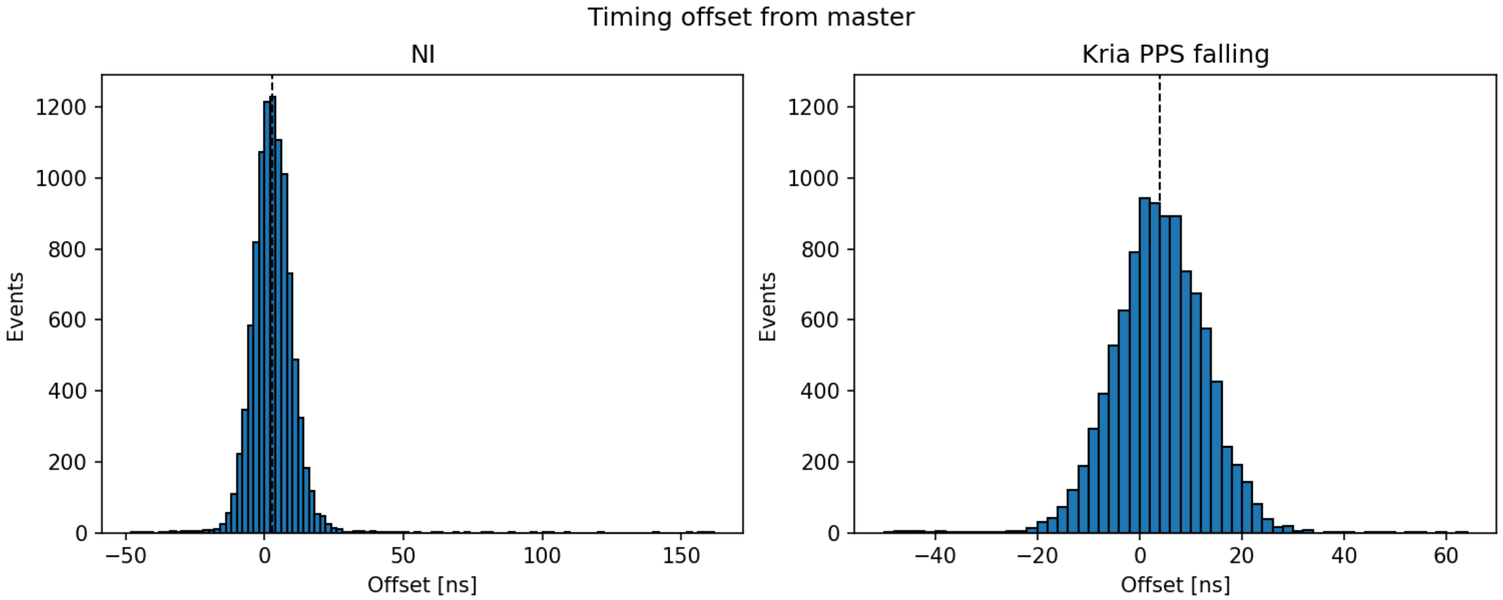
Test setup: PTP synchronization, PPS acquisition

The Grandmaster Clock synchronizes both timing boards; CAEN measures their generated PPS outputs.



Test A: PPS from the PTP-synchronized internal clock, raw data

Kria generates the PPS directly from its clock synchronized via PTP.



9.189 ns
NI Filtered RMS

9.738 ns
Kria RMS

161 ns
MAX delay

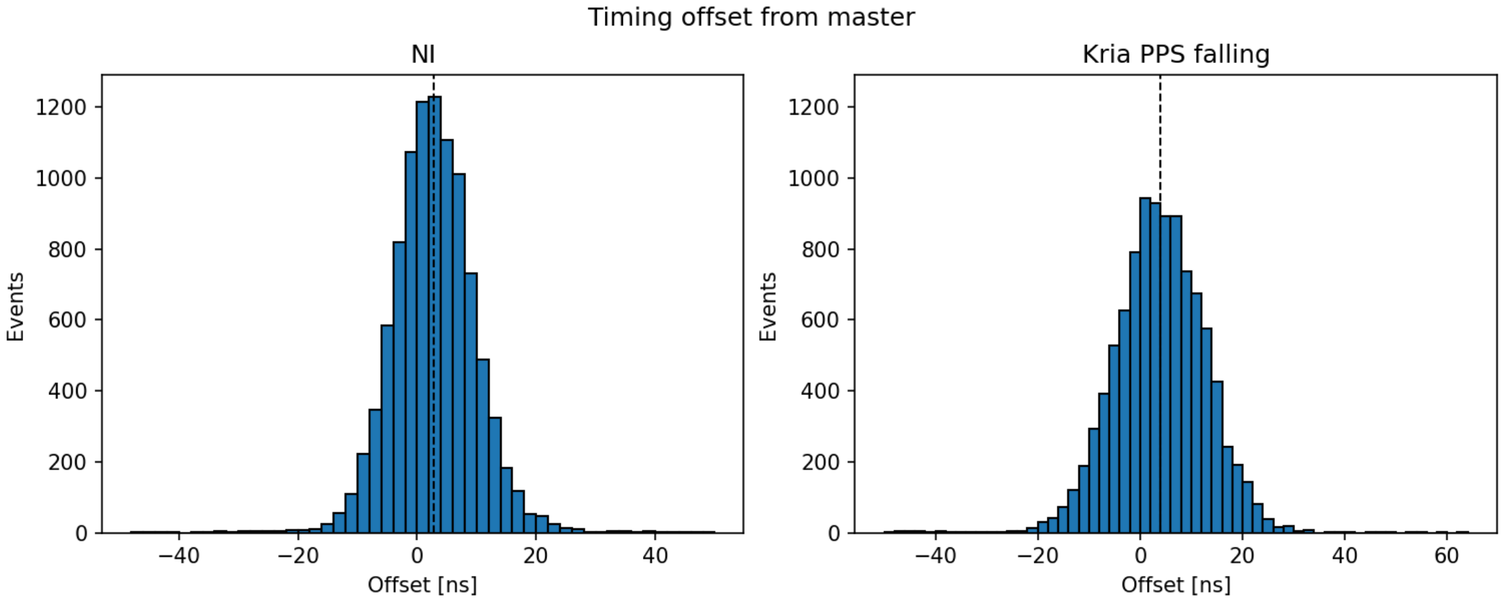
62 ns
MAX Delay

ITER requirement: RMS < 50 ns

PXI6683H synchronization presents groups of outliers that affect the statistics

Test A: PPS from the PTP-synchronized internal clock, filtered data

Kria generates the PPS directly from its clock synchronized via PTP.



7.726 ns

NI Filtered RMS

9.738 ns

Kria RMS

ITER requirement: RMS < 50 ns

The direct PPS path is already compliant, but it leaves room for jitter reduction.

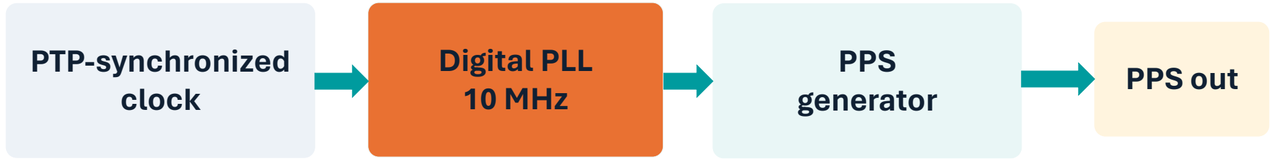
Two Kria PPS generation paths

Both tests start from PTP synchronization; the difference is where the PPS is derived.

Test A: direct PPS path

- The KRIA generates the PPS directly from the PTP Hardware Clock (PHC)

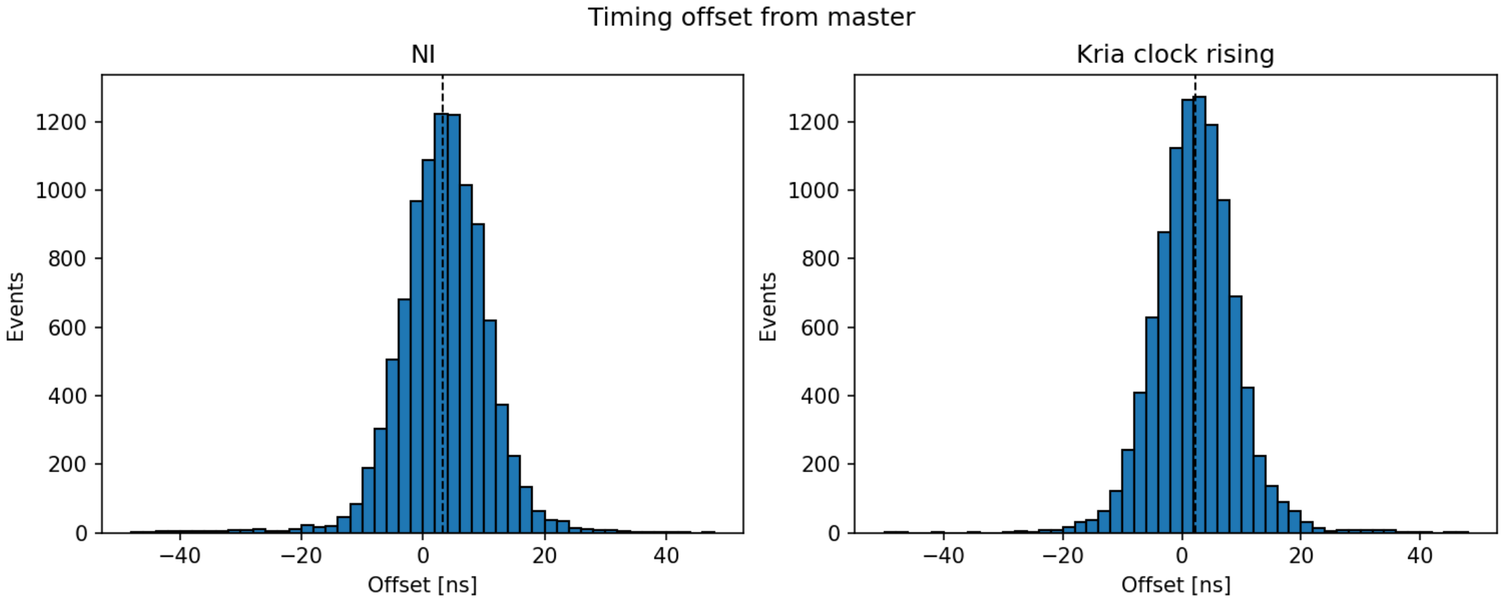
Test B: 10 MHz digital PLL path



- The KRIA links a 10MHz clock to the PTP Hardware Clock (PHC)
- The PPS is generated from the 10MHz clock
- The output triggers and clock are generated by the 10MHz clock

Test B: digital PLL to 10 MHz, then PPS generation

The PTP-synchronized clock feeds a digital PLL; the resulting 10 MHz clock generates the PPS.



8.167 ns

NI filtered RMS

7.177 ns

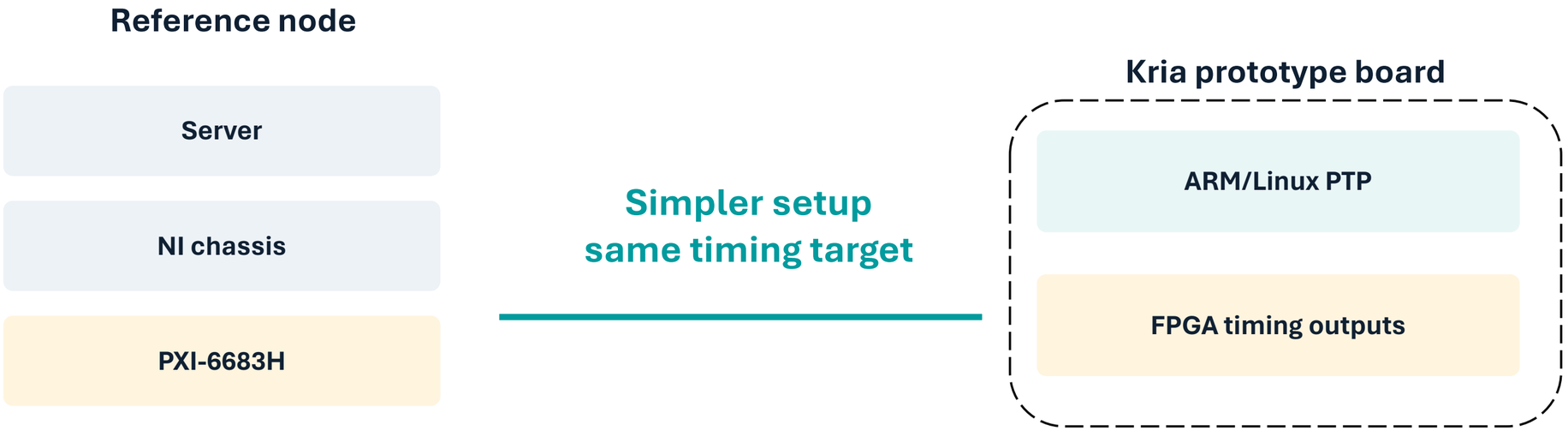
KriaRMS

ITER requirement: RMS < 50 ns

The 10 MHz digital PLL path reduces variance and gives the best Kria result.

Cost and integration impact

The Kria prototype statistics are comparable with the ITER timing nodes.



Conclusions and next steps

MITICA validated the ITER TCN path.

The 10 MHz digital PLL path gives the best Kria result.

The next validation is API-level compatibility.

ELAD will produce the final timing module with appropriate service contracts.

Future work: expose the prototype through behavior compatible with ITER TCN APIs and extend test duration.

7.177 ns	9.738 ns
Kria PLL path RMS	Kria direct PPS RMS