Fast Beam Position Calculation Implemented in FPGA

Wei Peng, Miao Wang, Yuchen Yang, Letian Huang and Shichuan Ding

***Abstract*—This paper presents the design of electron beam position processor with a fast beam position calculation implemented in FPGA. The digital beam position processor will be adopted to the free electron laser and high magnetic field (FEL-HMF) facility constructed by Anhui University in Hefei, China. The digital beam position processor consists of a RF front-end board, an ADC and FPGA board and an AC/DC power supply module, which is able to process 476 MHz RF signal from beam position pick-ups in sampling rate of 250 Msps. The RF front-end board cascading two low-pass filters, two bandpass filters, two low-noise amplifiers and a digital attenuator, achieving performance of out-of-band suppression >60 dB over the 466–495 MHz frequency range. Its total gain is 40 dB and controllable gain is 31 dB with 1 dB step. The ADC and FPGA board have two dual-channel ADC chips and an Zynq SoC XC7Z045. We have implemented all digital signal process and data calculation at floating-point format in FPGA to improve precision and reduce latency. We test the digital beam position processor and compare the results of x and y with CPU calculation. The results show that the total processing latency is 122 cycles, the position precision STD for x-axis direction is 0.37 μm and for y-axis direction is 0.62 μm, and the differences between CPU and FPGA are 0.28 nm and 0.26 nm respectively.**

***Index Terms*—Field-programmable gate array (FPGA), Real time process, Beam position monitor, Beam diagnostics, LINAC, Free electron laser and high magnetic field (FEL-HMF)**

I. Introduction

THE experimental facility of free electron laser and high magnetic field (FEL-HMF) is been building by Anhui University in Hefei, China. Fig. 1 is the 3D model of FEL-HMF facility in campus of Anhui University. It is a unique integration of Infrared free-electron laser, high magnetic field, and low-temperature environment. The linear accelerator system in FEL-HMF will accelerate the electron beam to 15-60 MeV. The light wavelength of this facility cover middle and far-infrared，and is able to be continuously adjusted from 2.5 to 200 μm. It is primarily concerned with the investigation of quantum materials, with a particular emphasis on low power electronic materials. However, it also serves as a crucial experimental platform for a diverse range of multidisciplinary frontiers, including energy materials, biomaterials, medicine, and health materials. To facilitate the advancement of multidisciplinary research on low-power electronic materials, the facility is equipped with five experimental stations: (1) The Ultrafast Infrared Spectroscopy Experimental Station, (2) The Scanning Probe Microscopy Station, (3) The Magneto-Optical Experimental Station, (4) The Multi-field Control Experimental Station, (5) The Integrated Characterization Station and The Energy Materials Experimental Station [1].

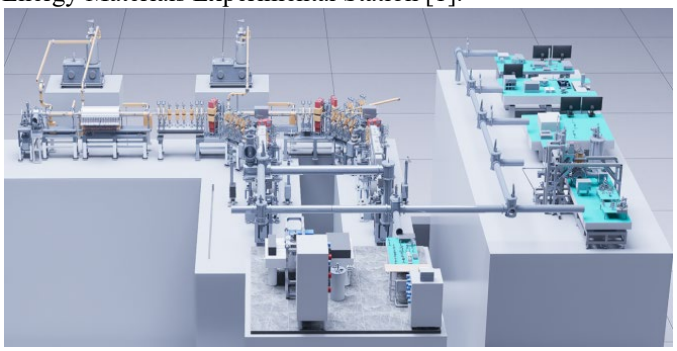

Fig. 1. 3D model of FEL-HMF facility in campus of Anhui University.

Its electron linac operates in 2-10 Hz repetition rate mode and micro-pulse repetition rate can be set to 476 MHz, 238 MHz, 119 MHz, 59.5 MHz and 29.75 MHz. It serves as a primary source of electron beams to generate high quality mid- or far-infrared laser. Under such operating conditions, even small beam position deviations may lead to beam losses, radiation damage, or degradation of laser light source quality. Consequently, the beam position monitor (BPM) system must provide accurate beam position measurements with deterministic and ultra-low latency [2], [3].

Conventional BPM signal processing systems are often based on digital signal processors, embedded systems or industrial computers. While these solutions offer flexibility, their sequential processing architecture and reliance on operating systems introduce non-deterministic latency, making them less suitable for MHz-level repetition rates. In contrast, field-programmable gate array (FPGA) provides massive parallelism, deterministic timing, as well as low-power and high-speed interfaces, making them an ideal platform for real-time beam diagnostics [4]. The Digital down conversion (DDC) and Coordinate Rotational Digital Computer (CORDIC) were

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employed to calculate phase and amplitude[5], [6], [7]. The Discrete Fourier Transform (DFT) algorithm was evaluated and implemented in FPGA to resolve the signal phase and amplitude which reached better than 1 MHz rate beam signal processing [8].

This paper reports consideration, design, implementation, and experimental validation of an FPGA-based real-time beam position computation system. The system performs all critical signal processing tasks in hardware, including digital filter, digital down-conversion and beam position calculation at floating-point format, ensuring low latency and high precision. Accordingly, the digital beam position processor discussed in this paper is not only applicable to the FEL-HMF, but also to MHz-level repetition rates electron linacs [9].

II. System Requirements and Design Considerations

A. Operating Conditions of the Electron Linac

Button-type BPMs are employed in the linac beamline. The length of the BPMs are 25 mm and two inner diameter specifications: 33 mm and 39 mm. It is a diagonal orientation pickup, so coordinate system convention for diagonal is used when calculates beam position. The BPM system must process electron beam-induced RF signals for each pulse without dead time. Key system requirements are summarized in Table I.

TABLE I
KEY SYSTEM REQUIREMENTS

Parameters	Values
Micro-pulse repletion rate	476 MHz, 238 MHz, 119 MHz, 59.5 MHz or 29.75 MHz
Micro-pulse width	~10 ps
repetition rate	2-10 Hz
Macro-pulse width	10 μs
beam position resolution	＜30 μm
long-term stability	continuous operation over several hours without recalibration

B. Beam position measurement principle

When the electron beam passes through the button-type BPM, image currents are induced on four symmetrically arranged electrodes. The amplitudes of these signals are proportional to the beam displacement relative to the electrical center. The beam position in the horizontal and vertical directions can be expressed as [10], [11]:

$$\begin{cases} x = K_x \dfrac{(V_A+V_D)-(V_B+V_C)}{V_A+V_B+V_C+V_D} \\ y = K_y \dfrac{(V_A+V_B)-(V_C+V_D)}{V_A+V_B+V_C+V_D} \end{cases}, \quad (1)$$

where V_A, V_B, V_C, and V_D denote the amplitudes of the left-upper, right-upper, right-lower, and left-lower electrode signals and K_x and K_y are calibration coefficients. Fig. 2 shows button-type BPM electrodes naming and orientation. Here, beam direction into paper.

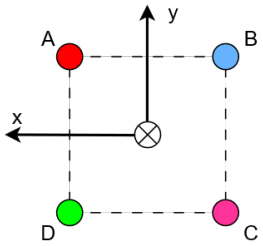

Fig. 2. Button-type BPM electrodes naming and orientation.

C. Motivation for FPGA-Based Implementation

Except for meet the requirements in Table I, we hope our system can be applied to MHz-level repetition rates electron linacs. So the signal processing chain must be high throughput, deterministic, low latency and so on. FPGAs are well suited to these demands due to their inherent parallelism, pipeline-friendly architecture, and hardware-level timing determinism.

In order to meet the aforementioned technical requirements and accommodate the operational range of electronic equipment, this paper proposes setting the operating frequency of the electron beam position processor to 476 MHz and the ADC sampling rate to 250 Msps. The sampling data are transmitted via an LVDS interface to the FPGA for processing. The FPGA operates at a clock frequency of 250 MHz. EDA software tools, such as AMD's Vivado, provide numerous IP cores that can be invoked and functionally combined to implement specific applications. This paper uses an AMD Zynq SoC processor and IP cores such as the FIR Compiler and Floating-point LogiCORE during real-time position computation. The FPGA signal acquisition and processing workflow is illustrated in Fig. 3.

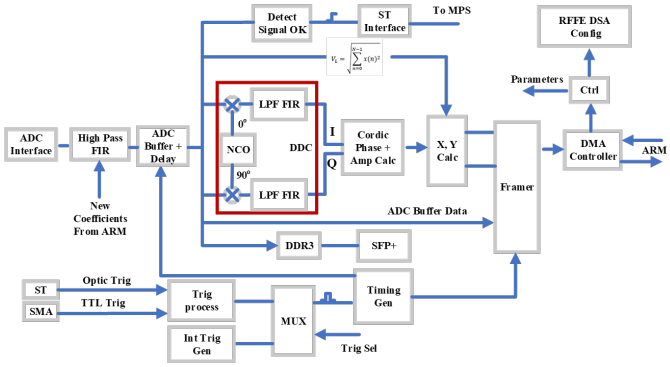

Fig. 3. Signal sampling and processing flow implemented in FPGA.

III. System Architecture

A. Hardware Overview

Fig. 4 shows the FEL-HMF digital beam position processor. It consists of three main parts: the RF front-end (RFFE) board, the ADC and FPGA board, and the AC/DC power supply module.

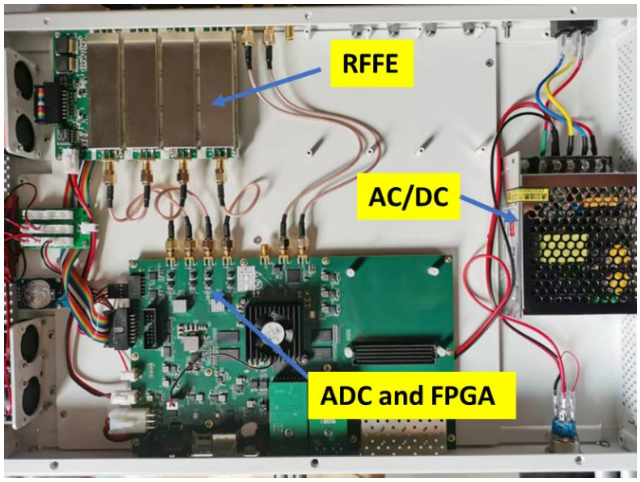

Fig. 4. Digital beam position processor of the FEL-HMF.

B. RFFE design

The RFFE has been designed and optimised for a center frequency of 476 MHz. It cascades two low-pass filters, two bandpass filters, two low-noise amplifiers and a digital attenuator. The low-pass filter is LFCN-530+ with a cut-off frequency of 530 MHz and insertion loss of 0.7 dB. The bandpass filter is a surface acoustic wave (SAW), model TA0555A, with an insertion loss of 1.9 dB and a ripple of 0.4 dB within the 476– 484 MHz band. Low-noise amplifier (LNA) TQP3M9036 operates across 50–2000 MHz with a noise figure of 0.4 dB and 20 dB gain. Combining the two LNAs with a DAT-31A-SP+, achieves 40 dB total gain and 31 dB controllable gain in 1 dB step. The control is a 5-bit serial interface, it is convenient for our system integration. The gains are linear with respect to the digital controlled attenuator (DSA) setting. As shown in Fig. 5, the RFFE exhibits out-of-band suppression >60 dB over 466–495 MHz frequency range. However, noticeable gain ripples occur within the operating band which will be corrected via gain calibration and compensation. Based on the sampling theorem, the post-sampling signal frequency range falls into the 5-34 MHz range in the digital domain.

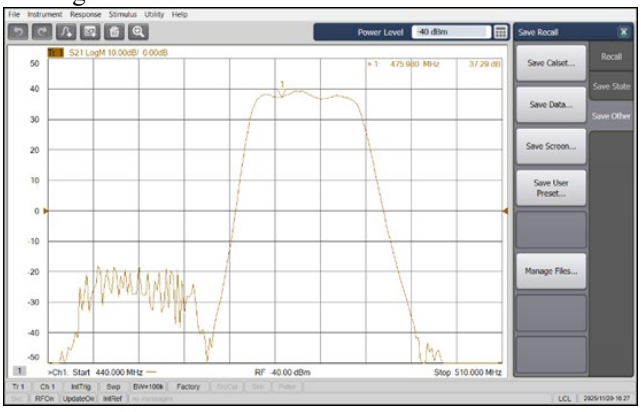

Fig. 5. Test of the RFFE.

C. ADC and FPGA Board Design

On the board, there have two dual-channel ADC chips which have sampling rate of 250Msps, -3dB analogue bandwidth of 900MHz and resolution of 16-bit. In order to achieve optimal performance from the ADC, we connect two identical RF baluns back-to-back and add termination resistor pair between the two baluns. This design helps minimize mismatch and good performance is obtained for 476MHz input signals. The maximum amplitude of the differential input signal permitted by the ADC is defined as the differential full-scale input, which is $2V_{pp}$. An AD9516 integrates a phase-locked loop (PLL)/voltage-controlled oscillator (VCO) capable of locking to an external reference clock and outputting a 250 MHz sampling clock and FPGA reference clock. The board includes a 10 MHz TCXO crystal oscillator (NT0503EH3I507EN10) with a phase noise of -140 dBc/Hz@1 kHz.

The board is designed with an Zynq SoC XC7Z045 as the digital process unit. This chip incorporates a dual-core ARM Cortex-A9 and FPGA within a single chip. The ARM dual-core Cortex-A9 application processor is based on the ARMv7 architecture and operates at a main frequency of 800 MHz. It features two SPI interfaces, two I2C, and is capable of supporting up to a 2-way Gigabit network, as well as a 32-bit DDR3 specific memory interface. A Debian operating system and EPICS-based application run on the ARM. The FPGA have plenty of logic cells, look-up tables, digital signal units, and sixteen-way 10 Gbps high-speed transceivers. It is suit for the implementation of logic operations and diverse interfaces. The board integrates 1 GB of 32-bit DDR3 memory for the real-time storage of raw ADC data. Four SFP+ ports provide a maximum speed of 10 Gbps for data transmission and communication. Two universal I/O slots can accommodate either HFBR-2412Z/1414Z optocouplers or SMA interface universal I/O modules. The board installed with one pair of transmit/receive optocoupler I/O module and one pair of transmit/receive SMA interface I/O module. These I/O channels are used to receive external triggers and output beam loss indicators. A standard mezzanine-connector (FMC) high-pin count (HPC) male connector is designed to expand functionality of the board.

D. Performance Test

A test platform had been built in laboratory, as show in Fig. 6. There is a G2 Analog signal generator model AP5012A output 476MHz RF signal to the digital BPM processor. Raw ADC data is stored on a PC, then a 1024 points Fast Fourier Transform (FFT) is used to analyze the RFFE and the ADC performance. Fig. 7 shows that with signal power is 0 dBm, the digital BPM processor performances: signal-to-noise ratio (SNR) is 58.1 to 58.9 dB and spurious free dynamic range (SFDR) is 71.6 to 74.1 dBFS, then induces the effective number of bits (ENOB) is 9.3 to 9.5 bits.

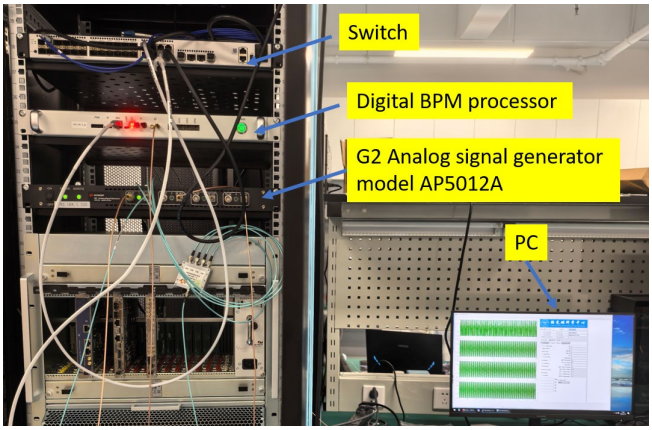

Fig. 6. Digital BPM processor tested in laboratory.

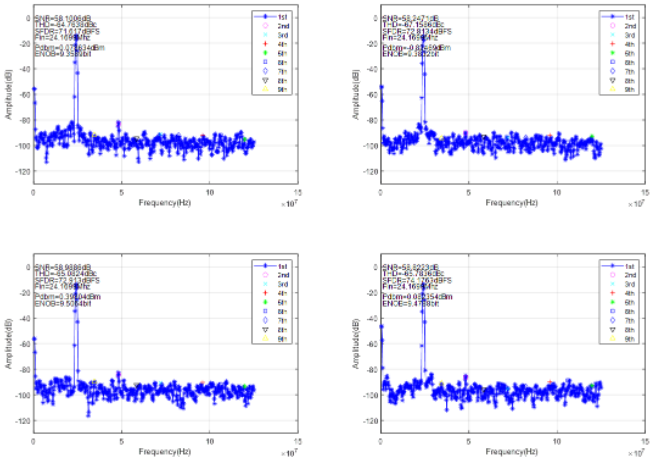

Fig. 7. A 1024 points FFT for the 4 channels of the digital beam position processor.

IV. Signal Processing in FPGA

The macro-pulse width of the electron beam is 10 μs. At a sampling rate of 250 Msps, a single-channel ADC will generate approximately 2500 data points. To reduce latency and enhance throughout, all digital signal processing is performed by the FPGA. As shown in Fig. 3, the processing flow primarily includes: FIR filtering, integer multiply-accumulate operations, integer-to-floating-point conversion, and calculating position x and y at floating-point format.

A. Reloadable High-pass FIR Filter

The FFT analysis results shown in Fig. 7 reveal the presence of a DC component in the raw ADC data. To enhance the system's measurement accuracy and stability, an FIR high-pass filter is first applied to remove the DC portion. The FIR filter computes the convolution sum defined in (2), where N is the number of filter coefficients.

$$y(k) = \sum_{n=0}^{N-1} a(n)x(k-n) \quad k = 0, 1, \ldots \quad (2)$$

Using a filter design tool, we generated filter coefficients that balanced resource consumption and performance in order to design a 57th-order high-pass filter. The resulting filter has a cutoff frequency of 1 MHz, 50 dB out-of-band suppression, and 0.1 dB in-band ripple. We instantiated the FIR IP core in the FPGA and loaded it with the generated filter coefficients. Fig. 8 shows the amplitude-frequency response of the high-pass FIR filter. We enabled the Use Reloadable Coefficients feature of this IP core [12]. This feature allows for the dynamic reconfiguration of the FIR coefficients, thereby updating the FIR filter's response characteristics. As previously mentioned, this feature will be used to compensate gain and phase unbalances between channels.

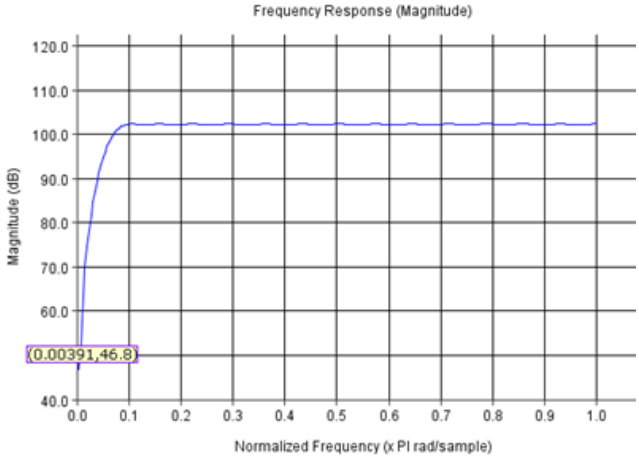

Fig. 8. High pass filter magnitude vs frequency response.

B. Amplitude Calculation

Generally, there are two main methods for calculating signal amplitude in the area of beam position diagnostics. The first one involves processing on the signal to obtain pairs of I/Q data chains, such as DDC and Hilbert Transform (HT) [8]. Then the signal amplitude is estimated using operation $\sqrt{I^2 + Q^2}$ or the CORDIC algorithm [13], [14], or the fast approximate digital I/Q amplitude algorithm [15]. The second method uses time-domain processing (TDP) to calculate V_A, V_B, V_C, and V_D using the following formula [16]:

$$V_A = \sqrt{\sum_{n=0}^{N-1} x(n)^2} \quad (3)$$

Where V_A is amplitude from electrode A, $x(n)$ is the n-th ADC sample.

The system requires one set of x and y values per macro-pulse. Approximately 2,500 samples are acquired and processed during each macro-pulse. The FPGA implements amplitude calculation for I/Q data generated via DDC and TDP simultaneously.

For DDC method as show in Fig. 9a, the fast approximate digital I/Q amplitude algorithm has been implemented in FPGA to get amplitudes. This calculating process is pipelined and latency is 7 cycles. For 2,500 I/Q pairs, there are 2,500 amplitude values. We accumulate these 2,500 amplitudes to produce a single value before being sent to the fixed-to-float operation which converts the 47-bit unsigned format data to a 32-bit floating-point format (latency is 8 cycles). Then, 4 amplitudes are sent to position (x, y) calculation module. The outputs are final results of beam position (x, y).

The TDP method incorporates a square accumulation process and outputs only one amplitude value per macro-pulse. For our design, the square accumulation process output result is at 47-bit unsigned format. To obtain the final amplitude value, it requires a square root operation. Before performing this operation, the 47-bit unsigned format data is converted to a 32-

bit floating-point format. Fig. 9b illustrates the TDP processing flows. This FIR and square accumulation process are pipelined, resulting no blocking. Latency of the fixed-to-float has been set to be 8 cycles. The square root operation takes 29 cycles.

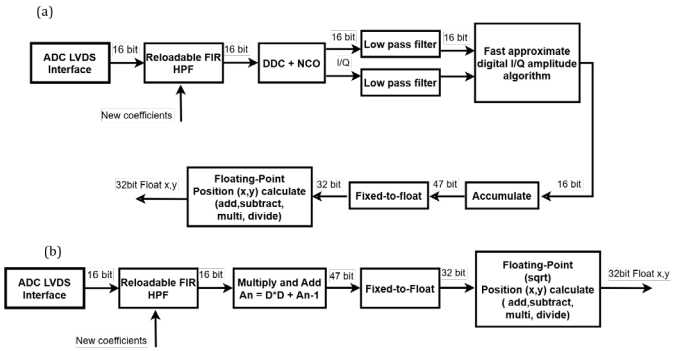

Fig. 9. FPGA implements real time beam position calculation, (a) digital down-conversion processing method, (b) time-domain processing method.

C. Process of Calculating Position x and y

Generally, beam position x and y processing is done in CPU. For our design, it is able to be calculated on the ARM core of the Zynq SoC XC7Z045. Intensive mathematical operations (float-point square root, multiply, divide, add/subtraction etc.) take up to several hundreds of ms processing time for the whole ADC buffer [16]. In this paper, we use the Floating-Point Operator IP Core in Vivado software to implement fully FPGA-based logic computation for position x and y. This reduces computation time, lowers the computational intensity of CPU and keeps calculating precision. Based on this advantage, we can use the digital BPM processor in the condition of high repetition rate mode. And also, it benefits the digital BPM processor in the processing of two or more beam position pick-ups simultaneously. For the digital BPM processor, we can add-on an FMC ADC sub-board and another RFFE module to connect with two button-type BPM pick-ups.

The Floating-Point Operator core provides simplified means to perform floating-point arithmetic on an FPGA. The core can be customized for different operation, word-length, latency and interface. It supports numbers of floating-point operators including: Multiply, Divide, Add/subtract, Square-root, fixed-to-float conversion and so on. These operators are compliance with IEEE-754 Standard [17].

According to equation (1), four stages have been designed to calculate position (x, y) as shown in Fig. 10. First stage calculates v1=V_A-V_C, v2=V_B-V_D, v3=V_A+V_C and v4=V_B+V_D. At second stage, using the results coming from stage 1 to calculate s1=v1-v2, s2=v1+v2 and sum=v3+v4. At third stage, xn=(s1-s2)/sum and yn=(s1+s2)/sum have been implemented. Finally, operating xn*kx and yn*ky to get position (x, y). A pulse signal is accompanying with the position (x, y) to show a valid result is ready.

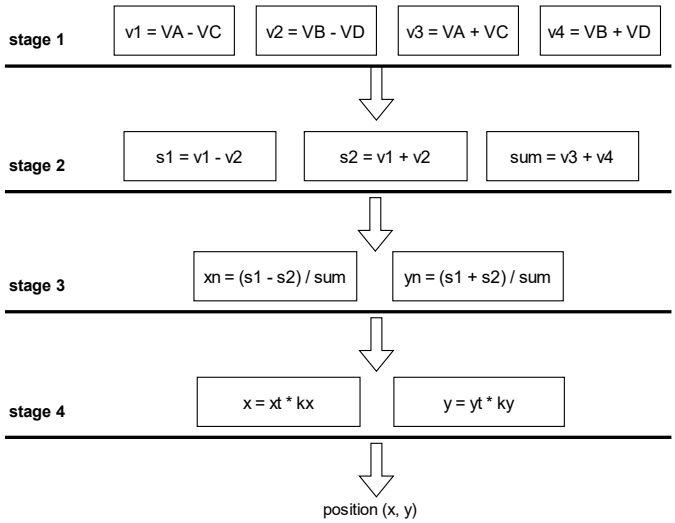

Fig. 10. Implementation of calculating position (x, y) in FPGA.

D. FPGA Implementation

Fig. 3 illustrates the FPGA signal acquisition and processing flow described in this paper. The flow comprises an ADC LVDS interface module, a high-pass FIR filter with reloadable coefficients, an amplitude calculation module based on DDC, a time-domain amplitude calculation module, a position (x, y) calculation module, an ADC data storage module, a data transmission module and a timing and control module. Table II shows resource utilization summary after synthesis and implementation in Vivado software, where DSP and I/O both exceed 45%, and MMCM and BUFG both exceed 60%.

TABLE III
RESOURCE UTILIZATION SUMMARY OF THE DESIGN

Resource	Utilization	Available	Utilization %
LUT	52023	218600	23.80
LUTRAM	13035	70400	18.52
FF	83194	437200	19.03
BRAM	85.50	545	15.69
DSP	423	900	47.00
IO	166	362	45.86
GT	1	16	6.25
BUFG	20	32	62.50
MMCM	6	8	75.00
PLL	1	8	12.50

We set the latency of all Floating-Point Operator cores on the FPGA implementation to be maximum. Four amplitudes V_A, V_B, V_C, and V_D are feed into the position (x, y) calculation module. The module output values of x and y at floating-point format after 75 cycles, as shows in Fig. 11. The fixed-to-float module latency is 8 cycles and the square root (sqrt) process latency is 29 cycles. For TDP method, the total latency including x and y calculation module latency, the square root (sqrt) process latency and the fixed-to-float module latency, which is 122 cycles. The total latency is much less than the period of one macro-pulse and meets the requirements of the FEL-HMF. We can conclude that the digital BPM processor with sampling rate of 250 Msps, is able to handle pulse-to-pulse beam position measurement above repetition rate of 2 MHz。

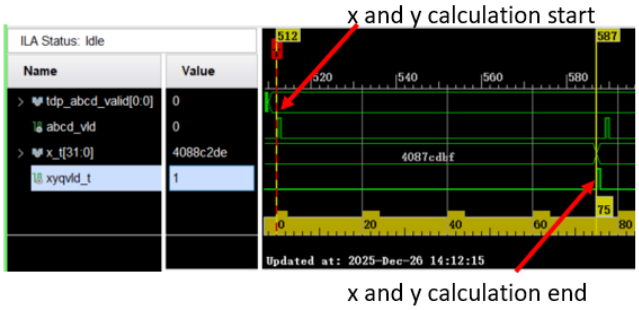

Fig. 11. FPGA implements x and y calculation latency.

E. Simulated Beam Position Test

Test platform is constructed to evaluate the performance of the digital BPM processor. A Keysight G2 signal source generates a 476 MHz sine wave signal which is divided into 4 signals by a 1:4 splitter. These signals simulate the RF signals coupled from the four electrodes of a BPM pick-up. A trigger signal is set to be 10 Hz, the same as FEL-HMF macro-pulse rate. Each macro-pulse acquires and processes ADC data in duration of 10 μs, triggering an output and saving a position (x, y) value each time.

Fig. 3 illustrates the flow of FPGA signal acquisition and processing, which includes real-time packet framing of ADC buffer data prior to transferring it to the ARM processor via DMA. The system runs a Linux operating system and two user processes. Process 1 acquires the data transferred from the FPGA via DMA and sends it to process 2. Process 1 receives control commands and filter coefficients from Process 2, then transmit these data to the FPGA. Process 2 implements Process Value (PV) distribution and reception based on the Experimental Physics and Industrial Control System (EPICS). The two processes communicate with each other via the socket mechanism [18]. During testing, we saved the ADC raw data and position (x, y) calculated on the FPGA corresponding to each valid macro-pulse in real time. We then calculated x and y on the CPU using time-domain processing methods. The test results are shown in Fig. 12 in the condition of K_x and K_y are 19.5 mm. In Fig. 12a, the blue cycles represent results calculated on CPU and red diamonds represent results calculated on the FPGA. We can find both results are very close and their standard deviation (STD) values are same. The STD for x-axis direction is 0.37 μm and for y-axis direction is 0.62 μm. Fig. 12b shows the deviation between the FPGA and CPU calculations which are in excellent agreement. The deviation (RMS) in the x-axis direction is 0.28 nm and in the y-axis direction is 0.26 nm.

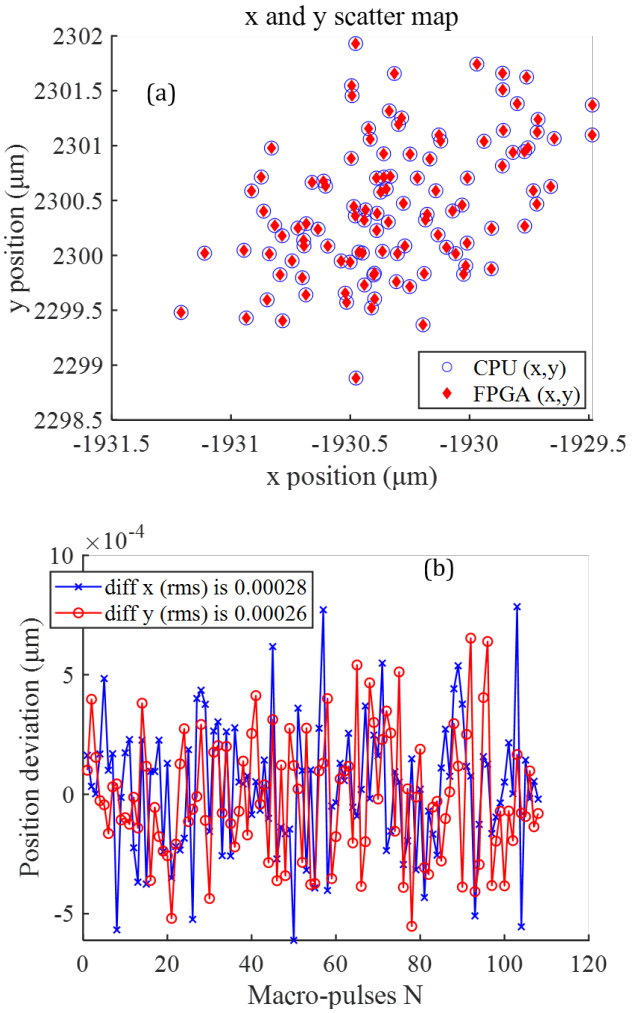

Fig. 12. Scatter map (a) shows the distribution along x-axis and y-axis for CPU calculation and FPGA calculation. (b) is the position deviation between the CPU calculations and FPGA calculations.

V. Conclusion

In this article, we have described the design of digital beam position processor with fast position calculation implemented in FPGA. The processor consists of a RFFE board, an ADC and FPGA board and an AC/DC power supply module, which is able to process 476 MHz RF signal from BPM pick-ups in sampling rate of 250 Msps. We have implemented all digital signal process and position (x, y) calculation at floating-point format in FPGA to reduce latency and enhance precision. The test result of total processing latency is 122 cycles, which is much less than the period of one macro pulse and meets the requirements of the FEL-HMF. Accordingly, we concluded that the digital beam position processor with sampling rate of 250 Msps, is able to handle pulse-to-pulse beam position measurement above repetition rate of 2 MHz. The deviations (RMS) between CPU calculations and FPGA calculations have been evaluated. The differences in the x-axis direction and y-axis direction are as follows: 0.28 nm and 0.26 nm.

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