安徽大學

Fast Beam Position Calculation Implemented in FPGA

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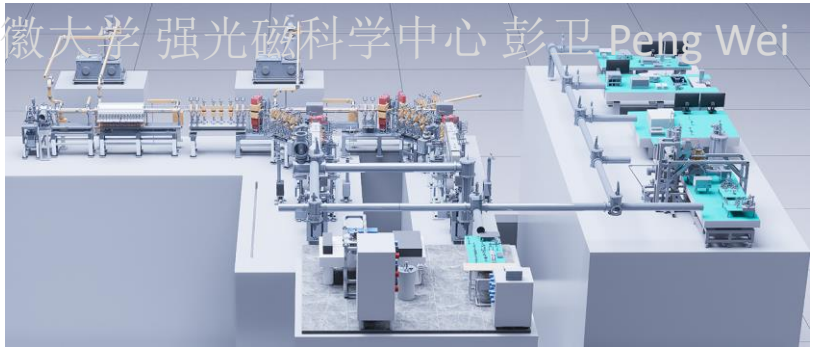
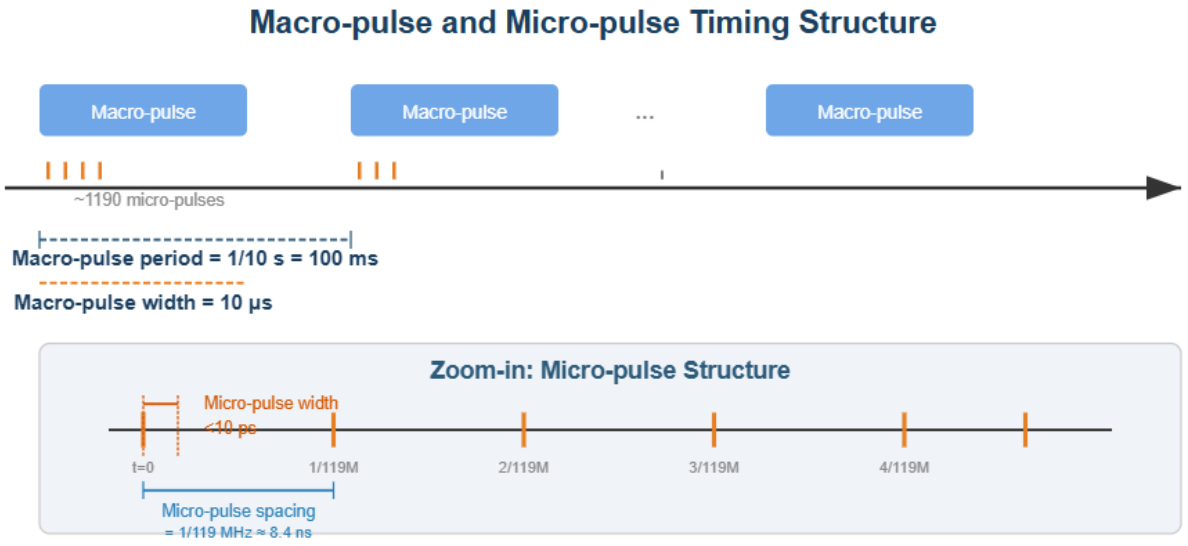
The Experimental Facility of Free Electron Laser and High Magnetic Field (FEL-HMF)

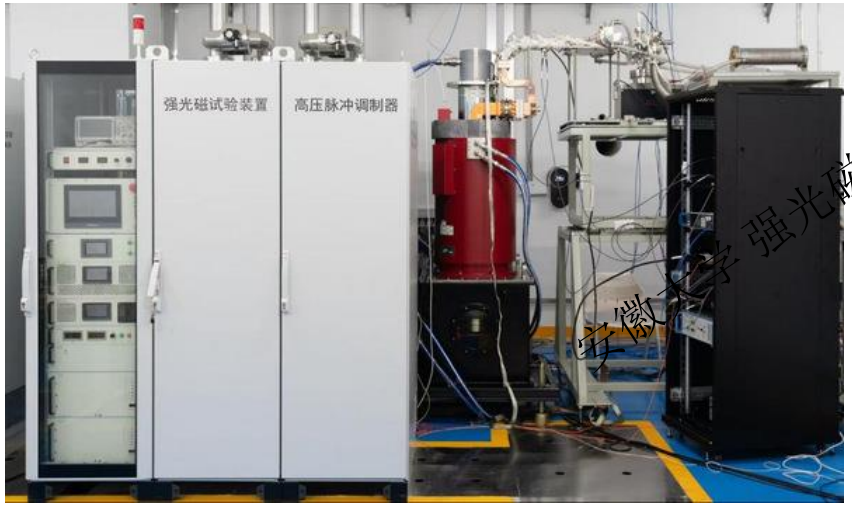
- **FEL-HMF is being built at Anhui University**
  - It concerns with the investigation of low power electronic materials, energy materials, biomaterials, medicine, and health materials
- **It integrates an Infrared free-electron laser (IR-FEL), high magnetic field, and low-temperature environment**

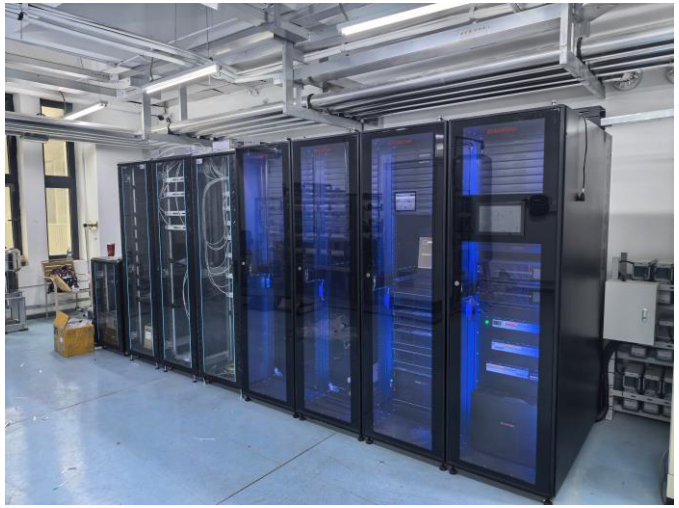




Parameter	Design Value
Wavelength	2.5 – 200 μm
Frequency	120 – 1.5 THz
Macro-pulse average power (typical)	0.6 W (@119 MHz)
Micro-pulse peak power (typical)	5 MW
Micro-pulse energy (typical)	10 – 100 mJ
Micro-pulse width	<10 ps
Bandwidth Δλ/λ	0.5 – 2%
Macro-pulse repetition rate	2 – 10 Hz
Micro-pulse repetition rate	476, 119, 59.5, 29.75 MHz
Electron energy	12 – 60 MeV
Electron beam energy spread	<5%
Micro-pulse peak current	>95 A
Emittance (typical)	<40 mm·mrad

FEL-HMF Current Status

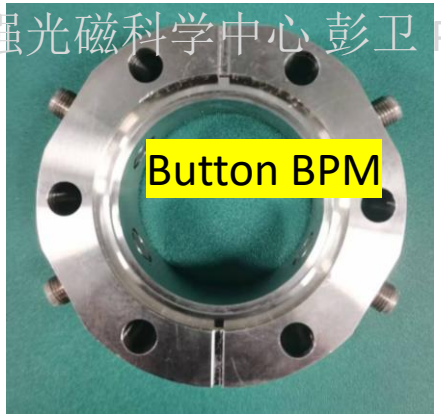


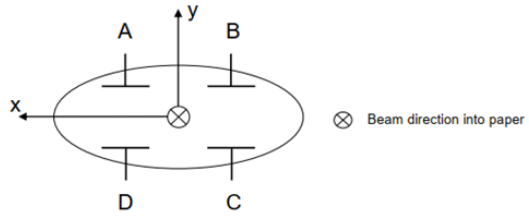


Beam Position Requirements for FEL-HMF

- Position resolution: 30 um
- Support repetition rate: 10 Hz
- Button BPM pick-ups:
  - 9 for LINAC (33 mm diameters)
  - 4 for undulator (39 mm diameters)
- RF frequency: 476 MHz, maximum power: 0 dBm, dynamic range: 40 dB
- Industrial standard 1U 19” rack-mount enclosure

- **Additive capabilities**
  - Support repetition rate up to 1 MHz
  - Support 2 BPM pick-ups in one digital BPM proccesor
  - ADC raw data can be stored and transmitted





$$SUM = V_A + V_B + V_C + V_D$$

$$X = K_x \frac{(V_A + V_D) - (V_B + V_C)}{SUM} + X_{OFFSET}$$

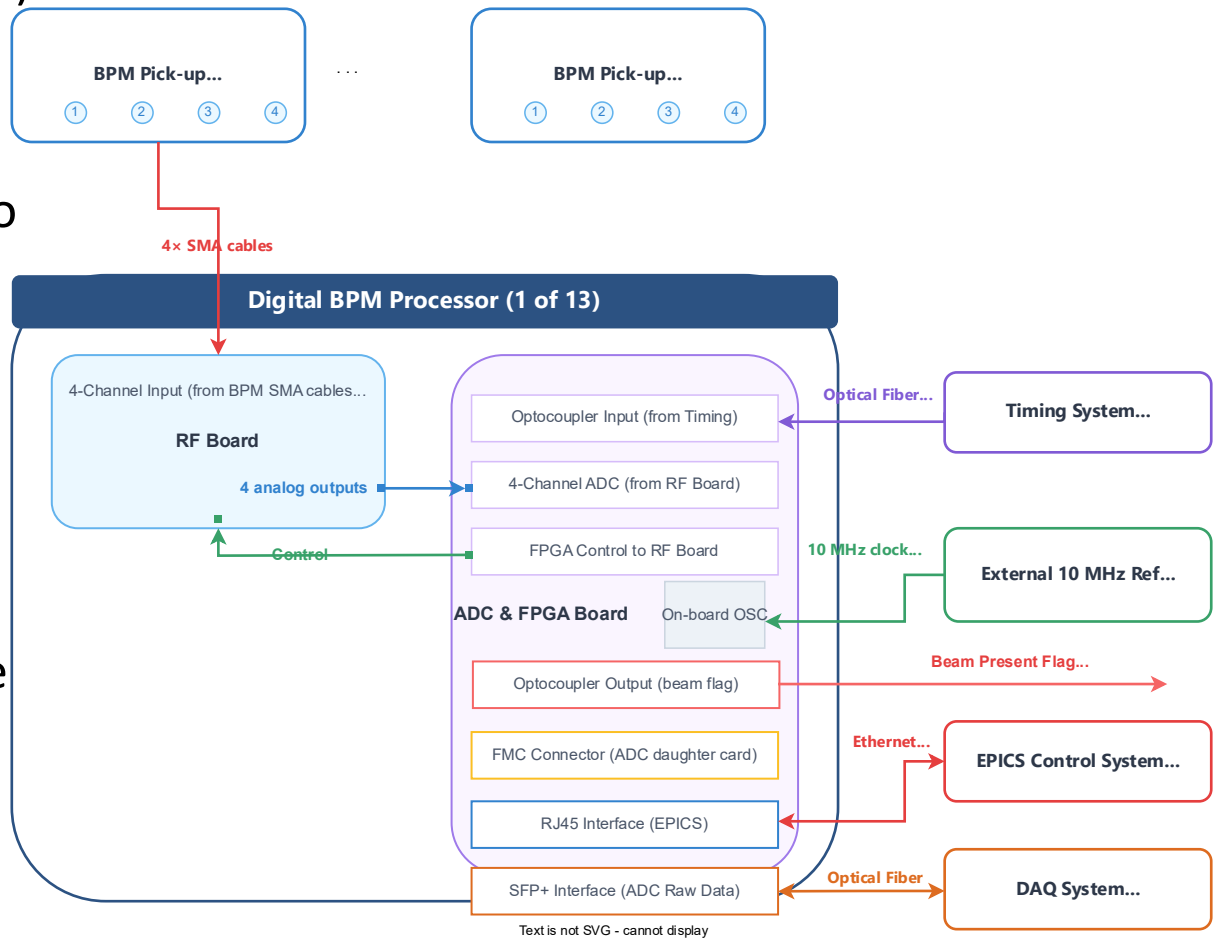
$$Y = K_y \frac{(V_A + V_B) - (V_C + V_D)}{SUM} + Y_{OFFSET}$$

4 RF signals from BPM pick-up are processed to calculate beam position (x, y)

Beam Position System for FEL-HMF

Digital BPM Processor Proposal

- **Main components:** Consists of RF front-end (RFFE) board, ADC & FPGA board, and AC/DC power supply module
- **Clock generation:** onBoard PLL/VCO , reference to TCXO or external clock
- **I/O interfaces:**
  - 1-in / 1-out optical coupler
  - 1-in / 1-out TTL SMA
  - RJ45 for EPICS (PV) and remote control
- **Data handling:** DDR + SFP+ interface for real-time ADC raw data storage and on-demand transmission
- **Expansion:** FMC connector to support an additional BPM pick-up



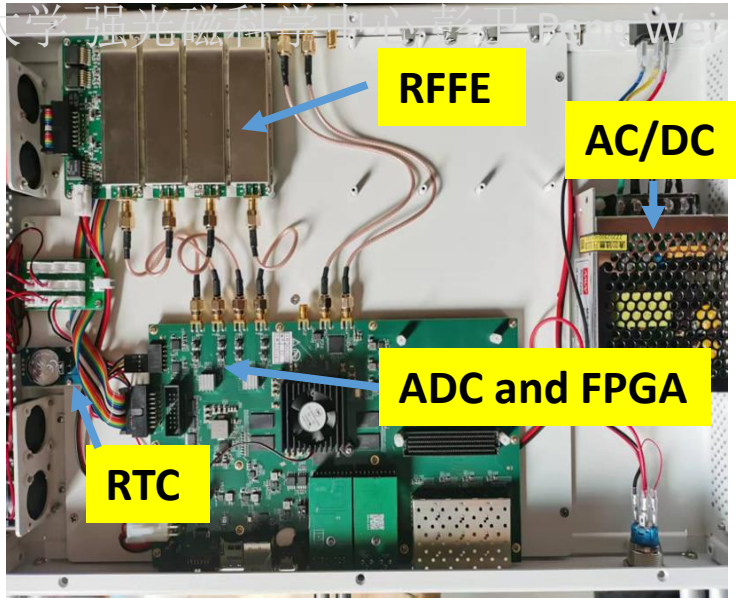
Digital BPM Processor for FEL-HMF

- **RFFE Board**
  - **Operating bandwidth:** 476-484 MHz
  - **Gain:** 40 dB
  - **Digital Step Attenuator (DSA):** 31 dB range, 1 dB step

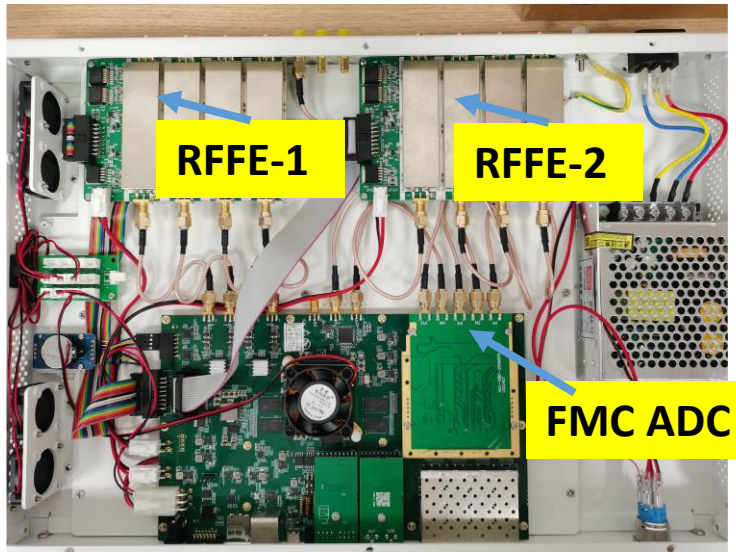
- **ADC and FPGA board**
  - **ADCs:** 2x 250 MSPS / 16-bit
  - **FPGA:** AMD XC7Z045
  - **Clock generator:** AD9516 and TCXO
  - **Memory:** 1GB DDR3
  - **Interfaces:** 1x RJ-45, 1x optical coupler (1-in / 1-out), 1x TTL SMA (1-in / 1-out), 4x SFP+, 1x FMC

- **FMC ADC**
  - 2x 250 MSPS / 16-bit

1 BPM mode

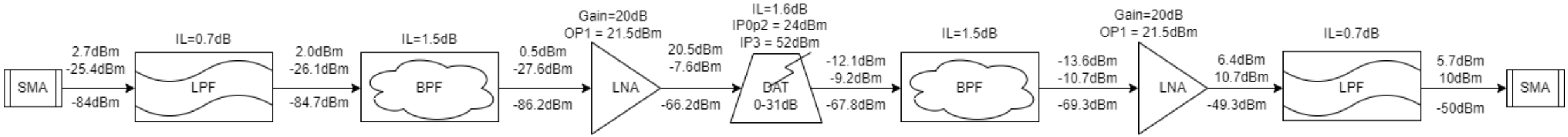


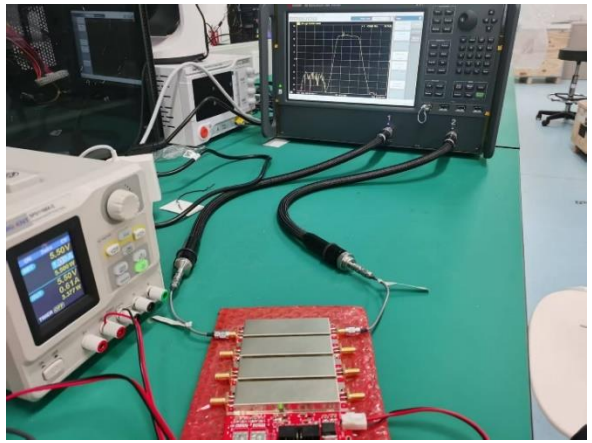
2 BPMs mode

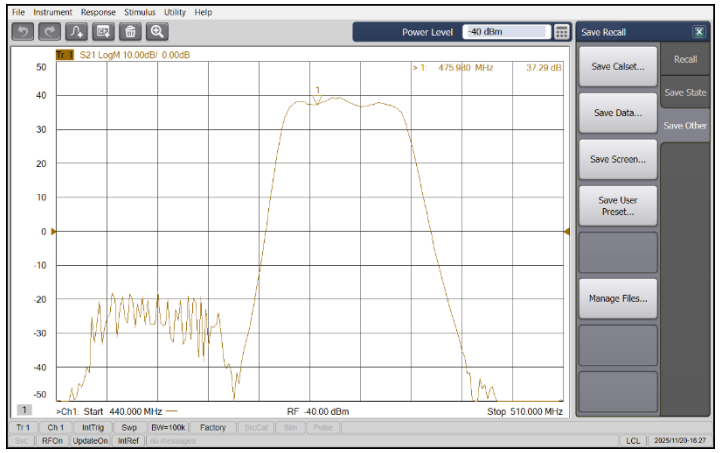


Hardware Test

- **RFFE board**





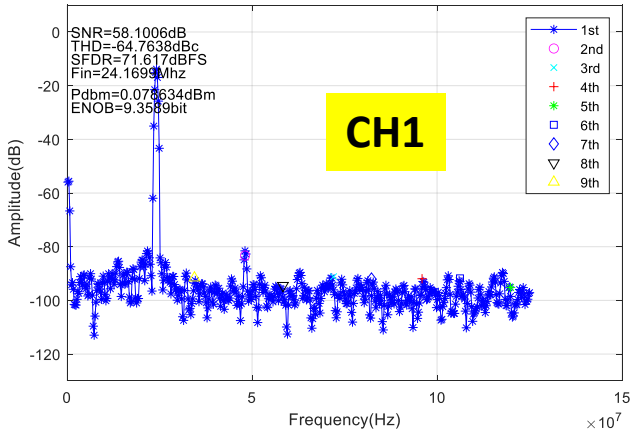


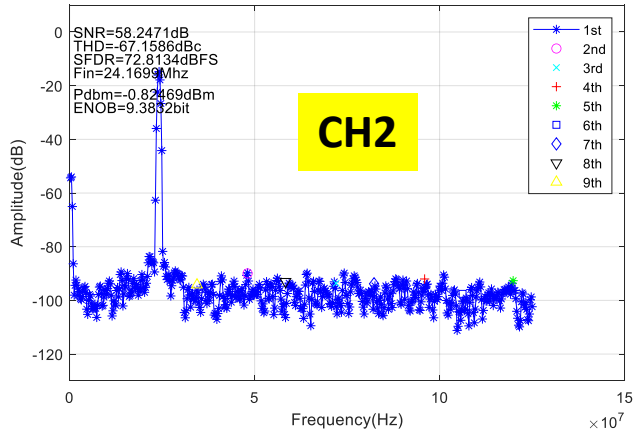
- Gain is linear with resect to the digital controlled attenuator (DSA) setting
- Out-of-band suppression >60 dB over 466–495 MHz. After sampling by the 250 Msps ADC, the RF signal falls into the 5-34 MHz range in the digital domain
- Gain ripples occur exist within the operating band and will be corrected via gain calibration and compensation

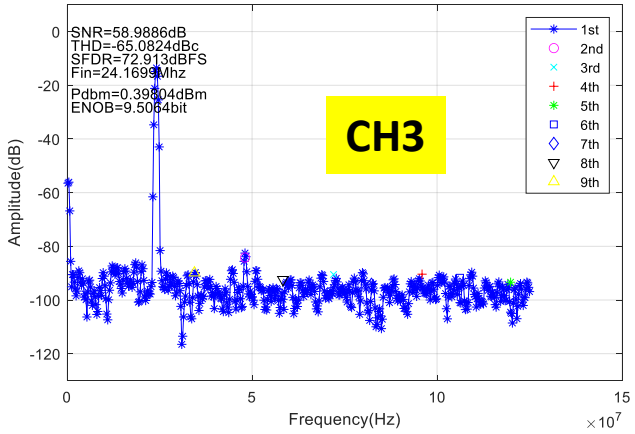
Hardware Test

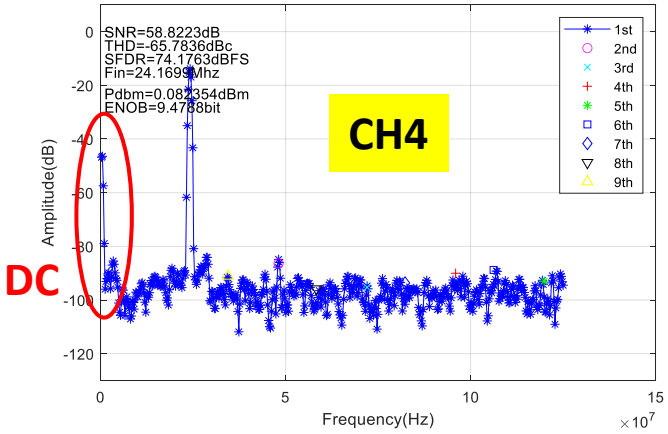
ADC and FPGA board

ADC raw data analyzed using FFT





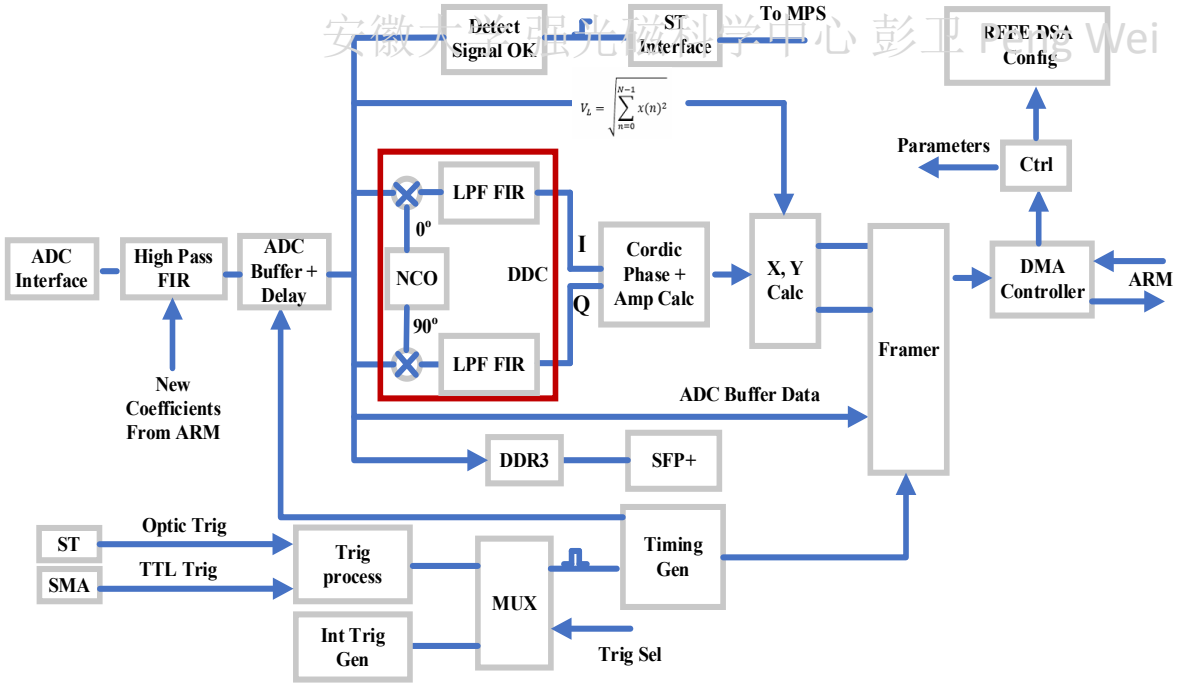


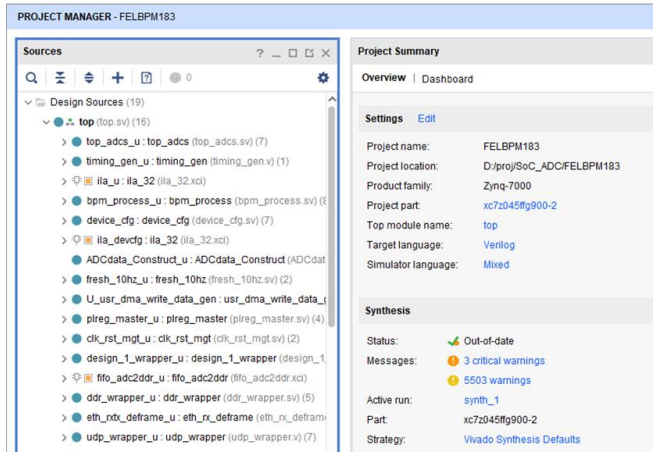


- 476MHz@0dBm
- SNR： 58.1 ~ 58.9 dB
- SFDR： 71.6 ~ 74.1 dBFS
- ENOB： 9.3 ~ 9.5 bits
- Exist DC component

Signal processing in FPGA

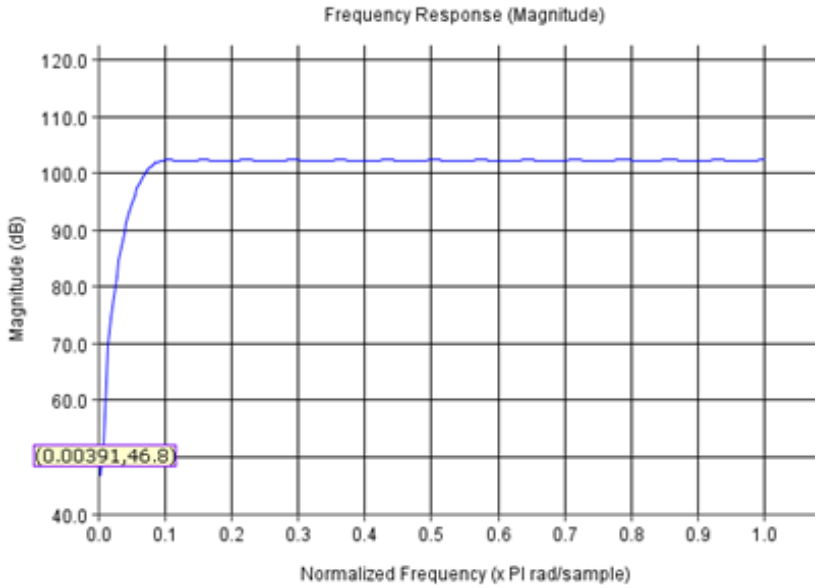
- **FPGA signal processing:** Reloadable High-pass FIR, DDC, CORDIC
- **Position (x, y):** calculated in FPGA @ 250 MHz
- Data path: ADC raw data → DDR3 （real-time buffering) → SFP+ transmission
- **Clock:** PLL/VCO (locked to 10 MHz), generates 250 MHz ADC sampling clock
- **RFFE attenuation:** 0 to 31 dB, 1 dB step
- Process timing and trigger, delay
- Handles data movement between FPGA and ARM cores



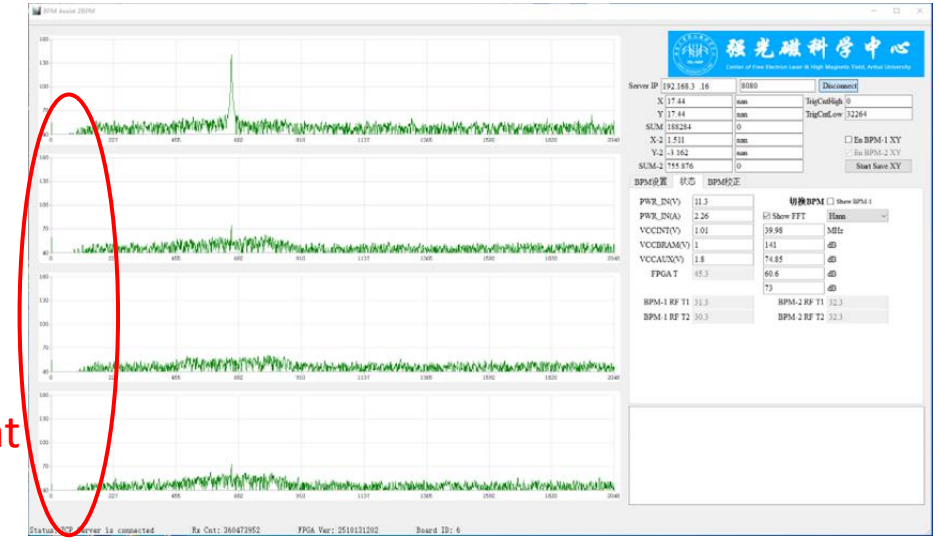


Signal processing in FPGA

- **Reloaded High-pass FIR Filter**
  - DC component removal
    - 1 MHz cutoff, 50 dB out-of-band suppression , and 0.1 dB in-band ripple
  - Convolution coefficients can be reloaded into the FIR IP core to provide gain and phase compensation
  - Vivado FIR IP core instantiated in FPGA



DC component removal

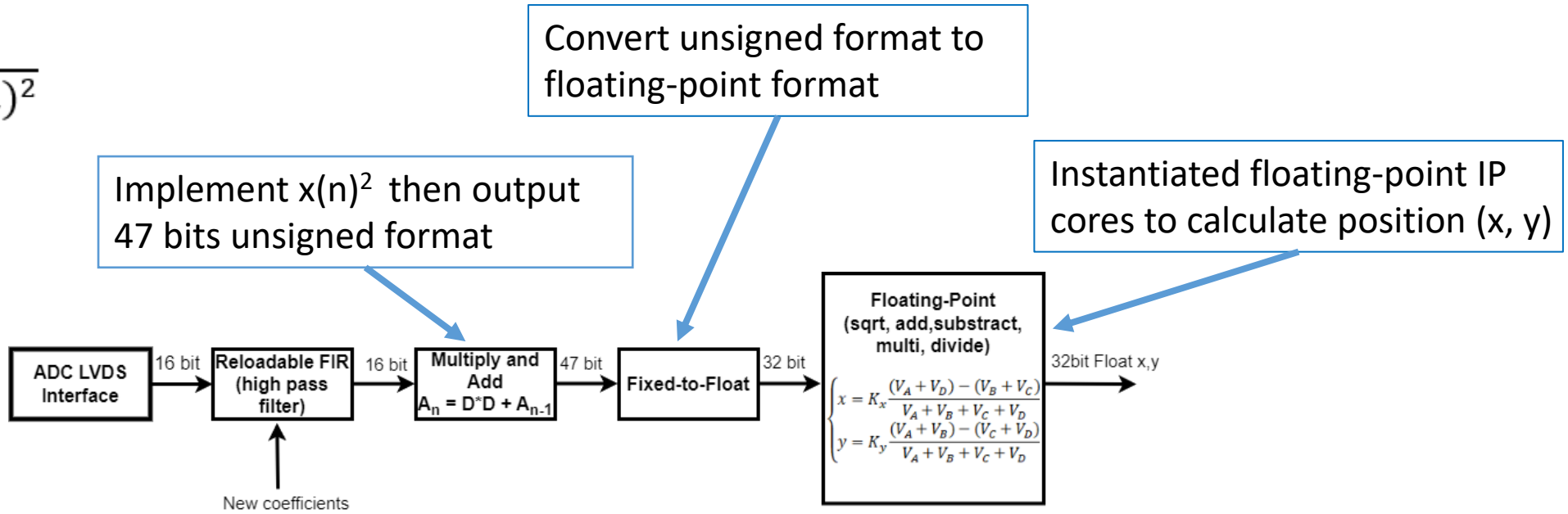


Signal processing in FPGA

- **Calculating beam position (x, y) in FPGA**
  - Update rate: one set of (x, y) per macro pulse (100ms)
  - Calculation inputs: amplitudes and scaling parameters
  - Amplitude calculation methods: (1) DDC + CORDIC algorithm, (2) **time domain processing (TDP)**

For TDP

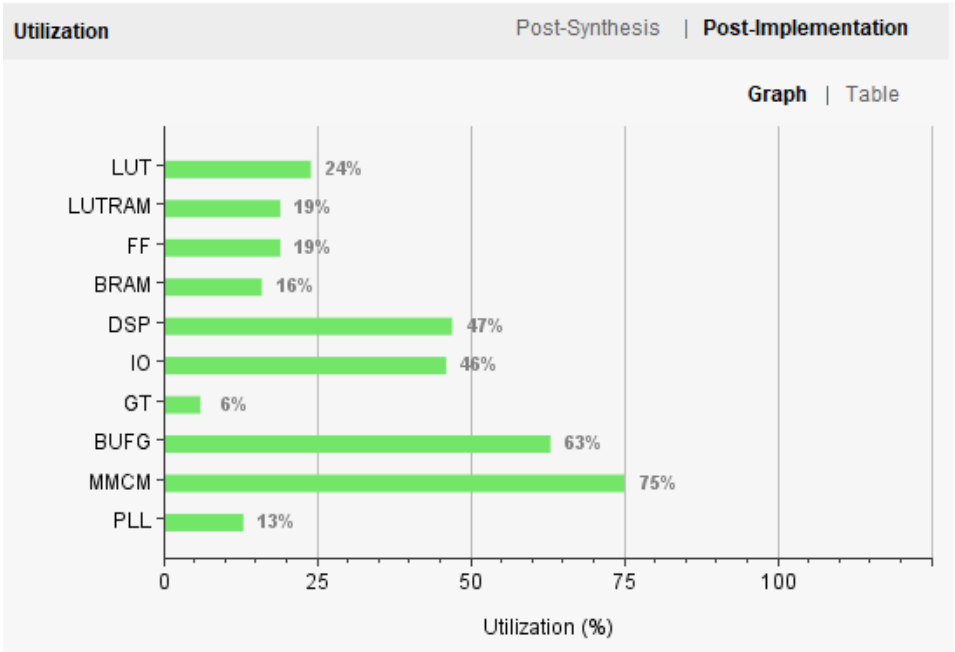
$$V_A = \sqrt{\sum_{n=0}^{N-1} x(n)^2}$$



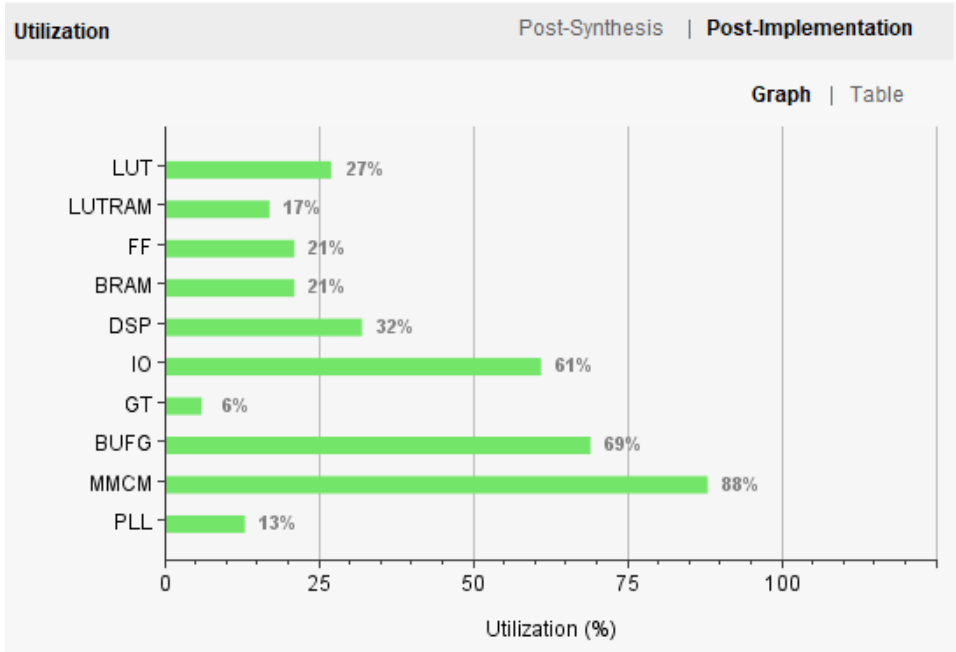
- **Typically, amplitudes and beam position (x, y) are calculated on the CPU**

Signal processing in FPGA

- **FPGA implementation resource utilization**
  - Single BPM pick-up: DSP and I/O ＞ 45%, MMCM and BUFG ＞ 60%, other resources ＜ 24%
  - two BPM pick-ups (DDC processing excluded due to timing violation), MMCM: 88%, BUFG: 69%, DSP: 32% (reduced), I/O: 61% (increased)



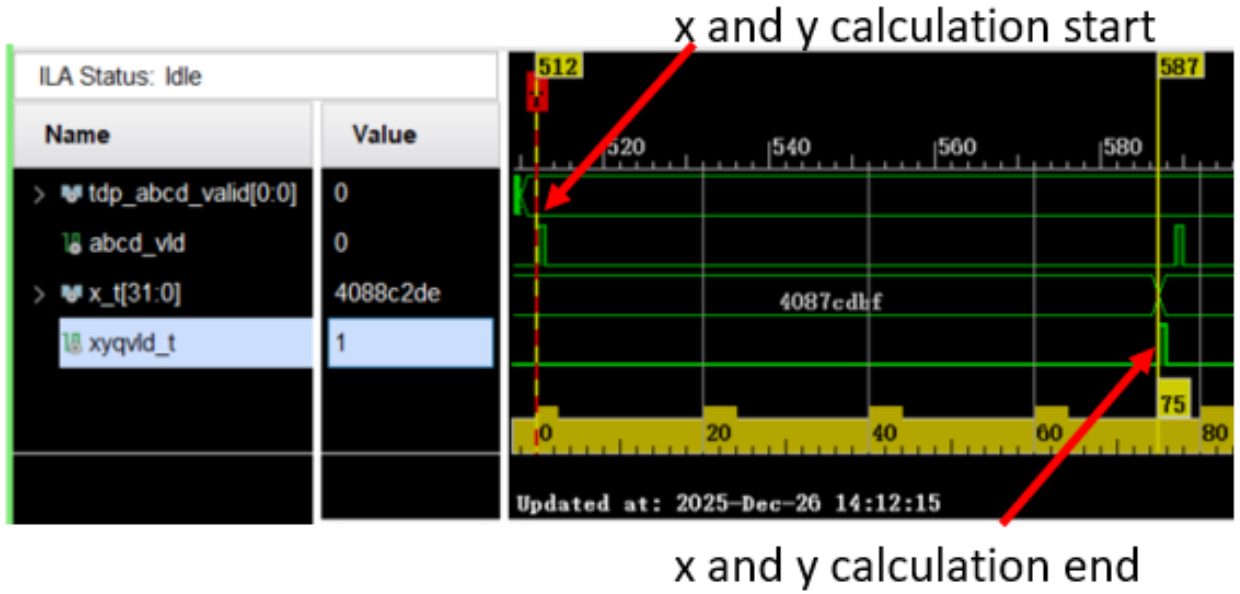
single BPM pick-up

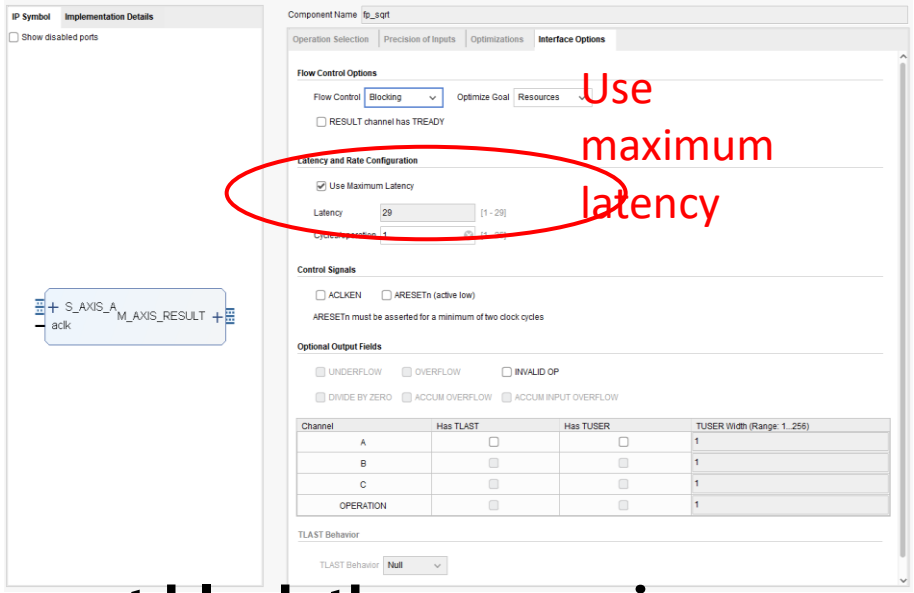


two BPM pick-ups

Test

- **X & Y calculation time measurement**
  - Floating-Point Operator cores: All latency settings to be maximum
  - Measurement method: Integrated Logic Analyzer (ILA) inside FPGA fabric
  - Total measurement time: 75 f_{sample} clocks
  - Preliminary square root (sqrt) process: 29 f_{sample} clocks





- **Total latency is 104 cycles at 250 MHz , which does not block the processing even at repetition rate of 2 MHz**

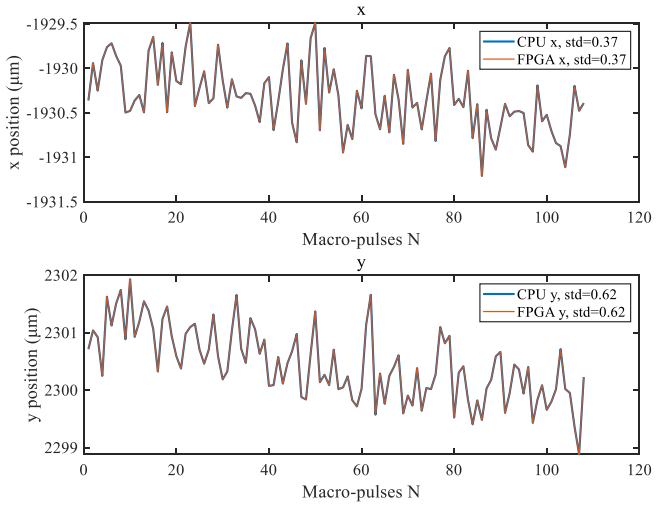
Test

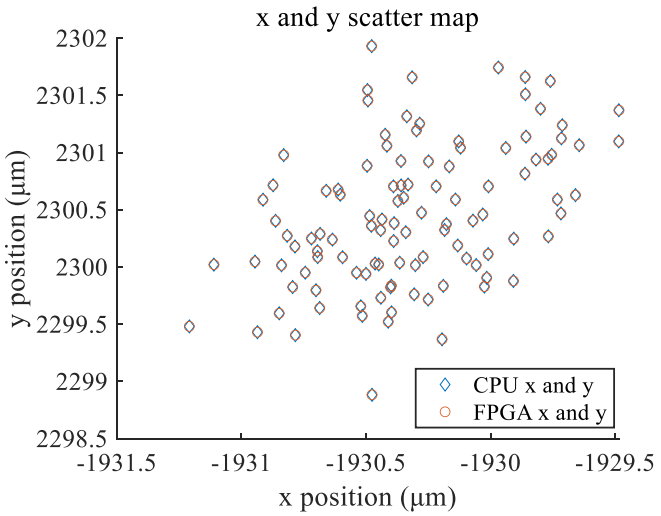
- **Comparison of FPGA and CPU results**
  - FPGA and CPU results are in excellent agreement**: identical STD values of 0.37 μm (x) and 0.62 μm (y)**
  - RMS differences are only **0.28 nm (x) and 0.26 nm (y)**

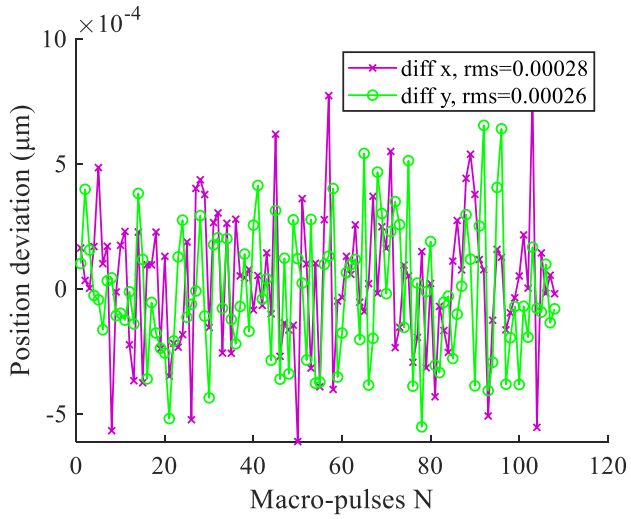
$$X = K_x \frac{(V_A + V_D) - (V_B + V_C)}{SUM}$$

$$Y = K_y \frac{(V_A + V_B) - (V_C + V_D)}{SUM}$$

K_x and K_y are 19.5 mm



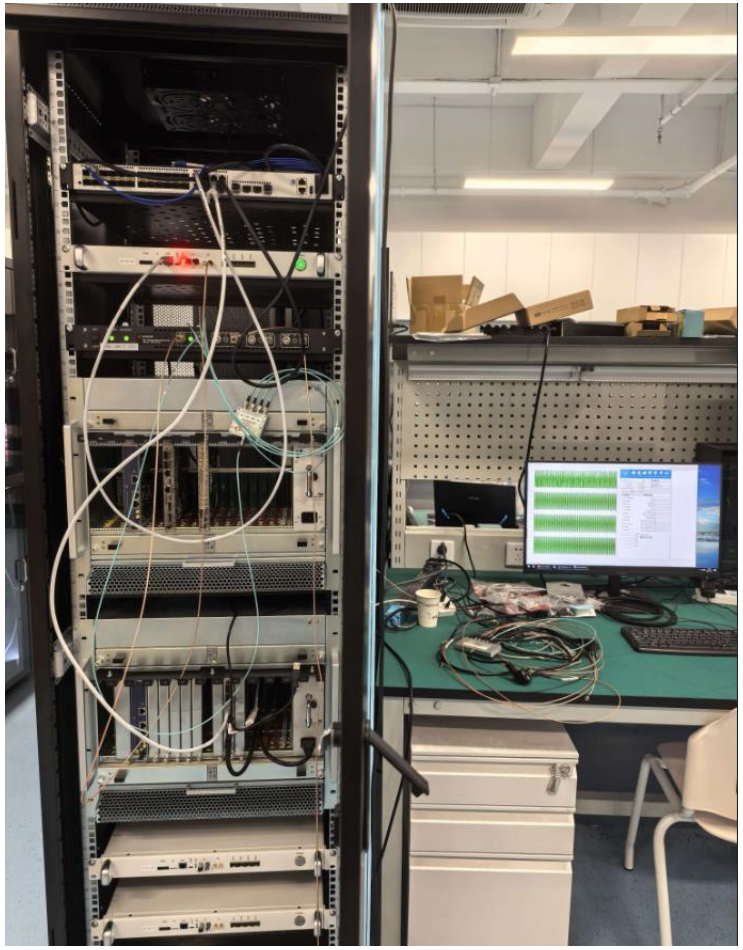




Summary and Perspectives

- Design a 476 MHz Digital BPM processor for FEL-HMF
- FPGA implementation reduces latency: FIR, amplitude, beam position (x, y) calculation
- The floating-point computation in FPGA yields identical results to CPU

- Calibrated gain bias (including RF cable variations) and verified at FEL-HMF
- Integrate real-time adaptive calibration for long-term stability
- Port to XC7Z020 for compact BPM readout modules
- Apply the same FPGA + floating-point methodology to other beam diagnostics (e.g., tune measurement, bunch length)



Thanks!