FRIB

Implementation of New Time Protocols on CTS Board for Clock Synchronization

Genie Jhang (changj@frib.msu.edu)

25th IEEE Real Time Conference
May 25th-29th, 2026

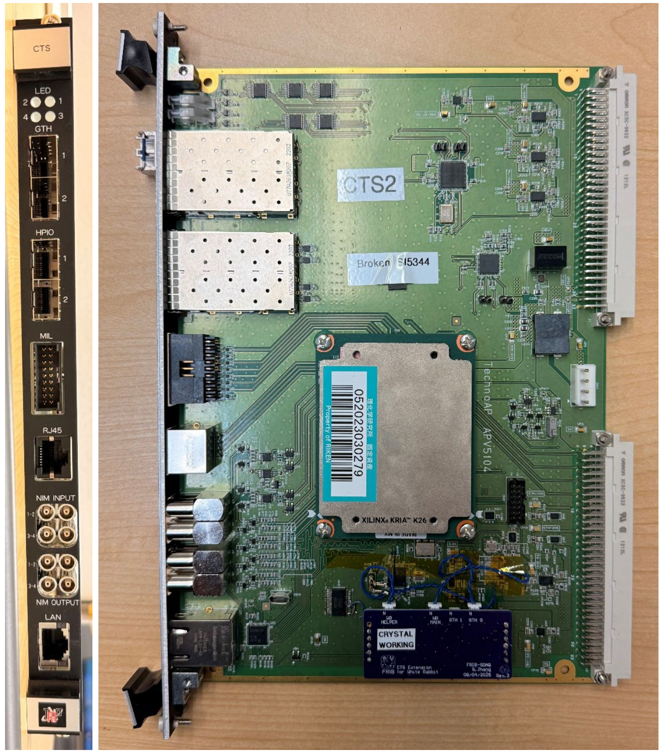
MICHIGAN STATE UNIVERSITY

U.S. DEPARTMENT of ENERGY | Office of Science

This material is based upon work supported by the U.S. Department of Energy, Office of Science, Office of Nuclear Physics and used resources of the Facility for Rare Isotope Beams (FRIB) Operations, which is a DOE Office of Science User Facility under Award Number DE-SC0023633.

CTS Board: Time Domains Converter

- Recent development in DAQ introduced new time protocols for synchronization from scientific collaborations (White Rabbit, MIKUMARI) and commercial companies.
- New electronics must coexist with old electronics and must synchronize properly as detector systems are becoming more complex (and the budget is limited).
- The collaboration between FRIB, RIKEN, and SPADI-A resulted in its firmware development for such purposes.
- The goal of this board is to provide a translation between different time domains for synchronization allowing to use new and old electronics as one system.
- Kria-based (SM-K26-XCL2GC) multi-purpose board
  - WRPTPCore, MIKUMARI (by R. Honda @ KEK), etc



Clock Timing Synchronizer board
designed by H. Baba (baba@ribf.riken.jp) @ RIKEN

White Rabbit PTP Core

- White Rabbit is a collaborative project started at CERN to provide time synchronization in sub-nanosecond accuracy.
- White Rabbit PTP Core is an FPGA implementation combining Synchronous Ethernet (SyncE) and the extended Precision Time Protocol (PTP).
  - 1Gbps Ethernet-based connection
  - Connecting long distances (~10km)
  - Picosecond precision of synchronization
- Open source hardware and software
  - Commercial options are also available

Synchronous Ethernet (SyncE) and Precision Time Protocol (PTP)

- In the standard ethernet, each node has its own free running clock and receiving node recovers clock from the data frame to deserialize bits.
- SyncE has a hierarchical structure between nodes with a system timing master.
- All the nodes' clock are synchronized (but not the same phase) to the system timing master's reference clock.

- PTP is an IEEE 1588 network standard designed for synchronizing the clocks in the sub-microsecond accuracy among devices across a network by exchanging timestamped messages.

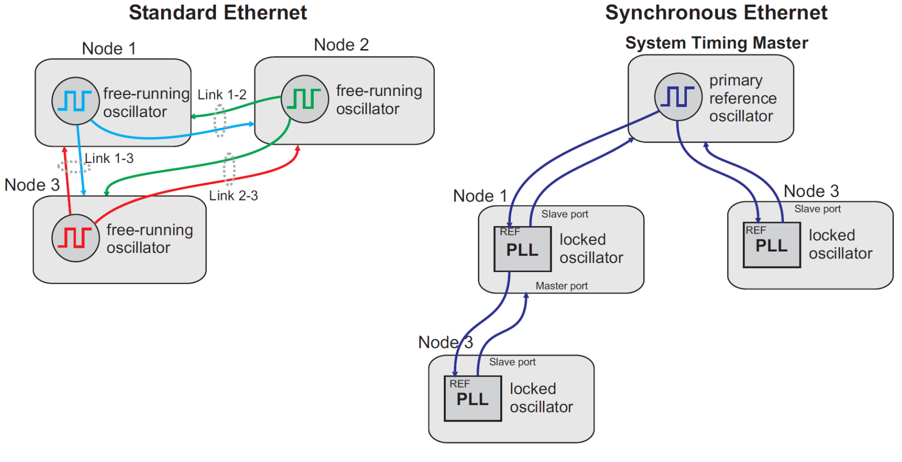


Figure 3.10. Comparison between standard and synchronous Ethernet

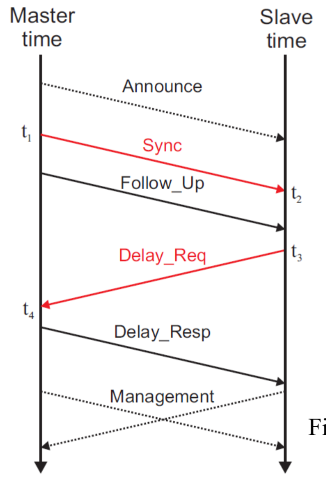


Figure 3.8. PTPv2 message exchange for a two-step End-to-End clock synchronization.

Reference: Precise time and frequency transfer in a White Rabbit network, Tomasz Włostowski, Master of Science Thesis

White Rabbit Synchronization Flow

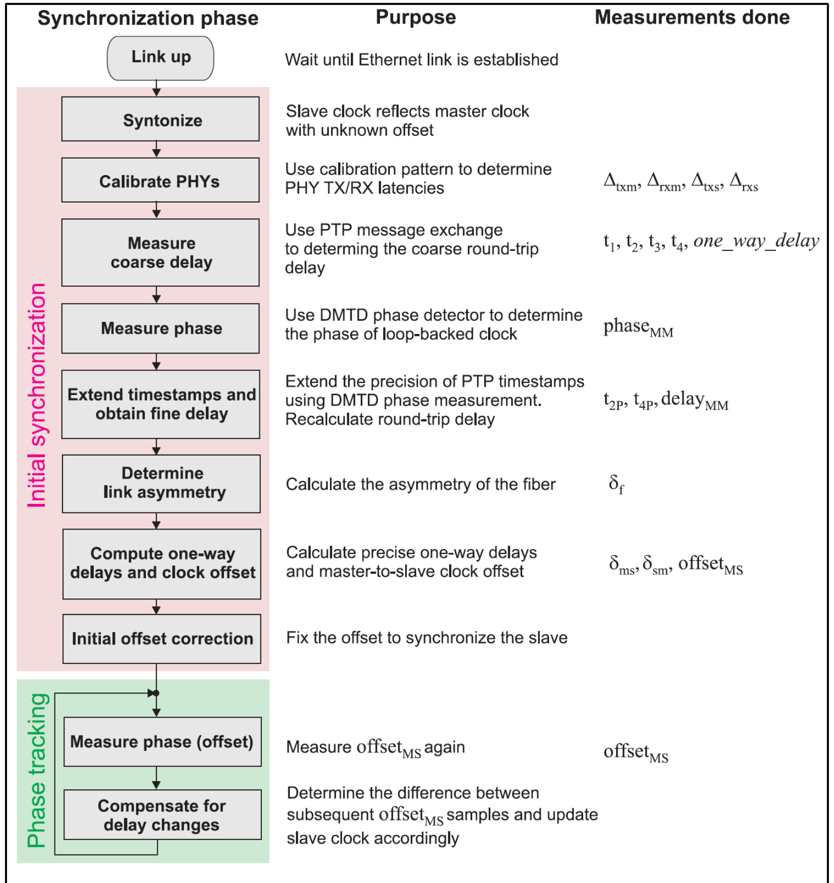


Figure 3.13. WR synchronization flow

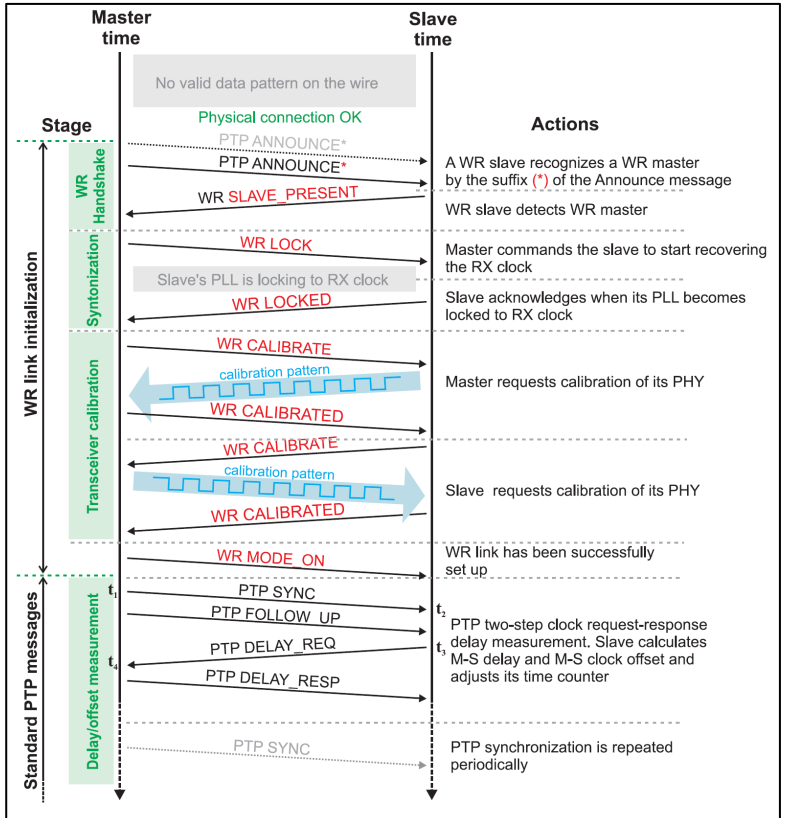


Figure 3.28. PTP message flow during WR synchronization.

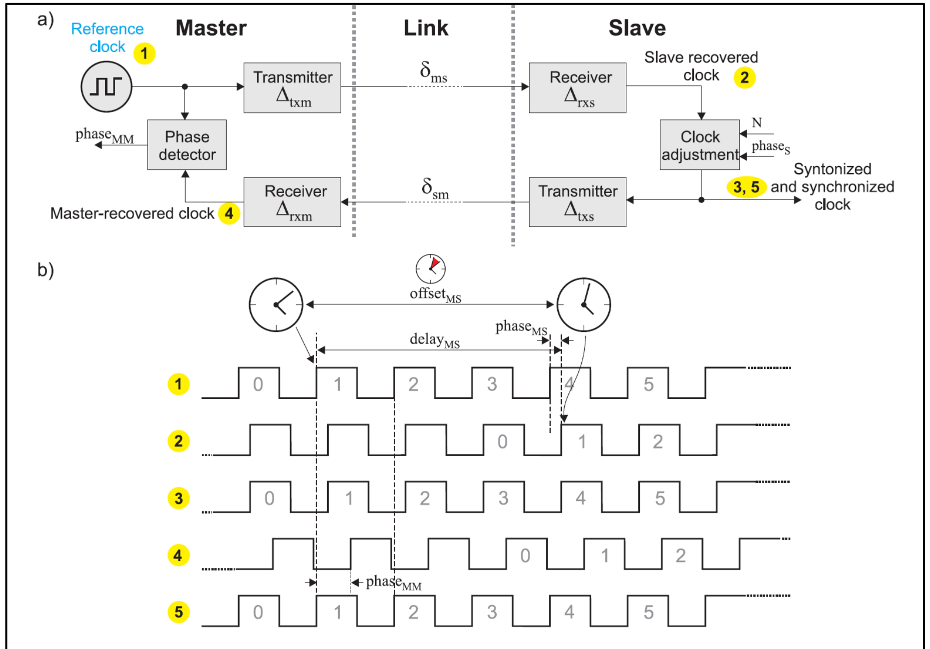


Figure 3.12. Model of a WR link (a) and relations between master and slave clocks (b)

Δ_{TXM} - transmission delay of WR Master

Δ_{RXM} - reception delay of WR Master

Δ_{TXS} - transmission delay of WR Slave

Δ_{RXS} - reception delay of WR Slave

ε_M - bitslide of Master's RX path

ε_S - bitslide of Slave's RX path

δ_{MS} - Master-to-Slave fiber latency

δ_{SM} - Slave-to-Master fiber latency

t_{2P} - phase corrected t_2

t_{4P} - phase corrected t_4

$$one\_way\_delay = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

Reference: Precise time and frequency transfer in a White Rabbit network, Tomasz Włostowski, Master of Science Thesis

Digital Dual-Mixer Time Difference (DDMTD)

- Using a clock slightly lower frequency than the measuring target clocks, magnifying the phase difference into measurable level.

$$f_{PLL} = \frac{2^N}{2^N + 1} f_{clkA}$$

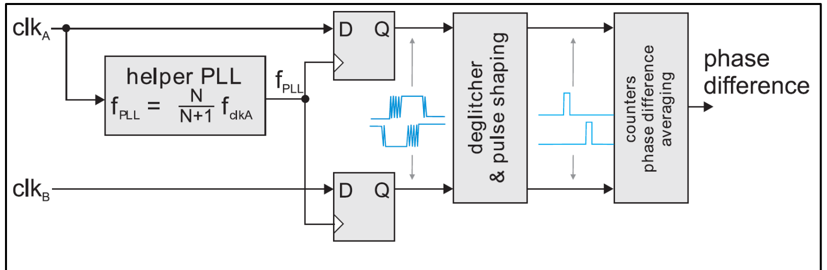
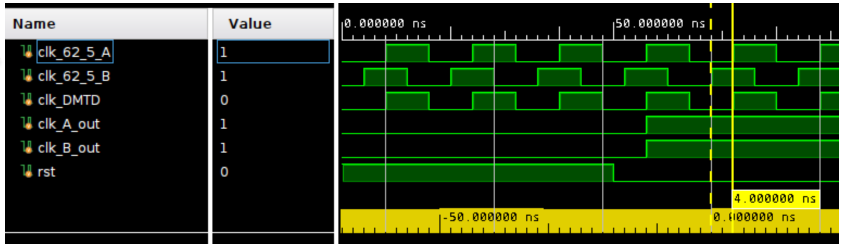


Figure 3.19. Structure of a digital DMTD phase detector

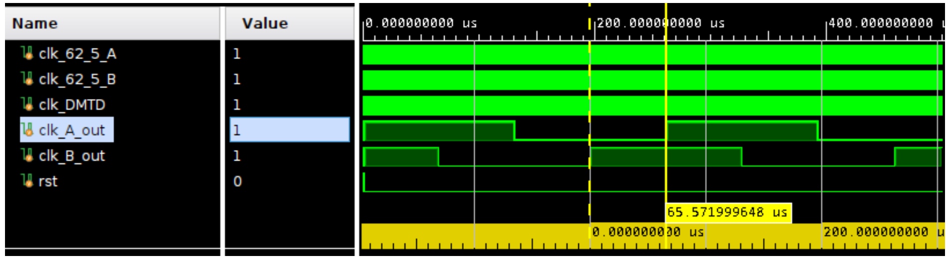
- The minimum measurable phase difference $\Delta\phi_{\min} = \frac{1}{2^N f_{PLL}}$
- The relation between the output and the input frequencies becomes $f_D = (2^N + 1) f_Q$.

Two clocks having 4ns phase difference



Zoom out

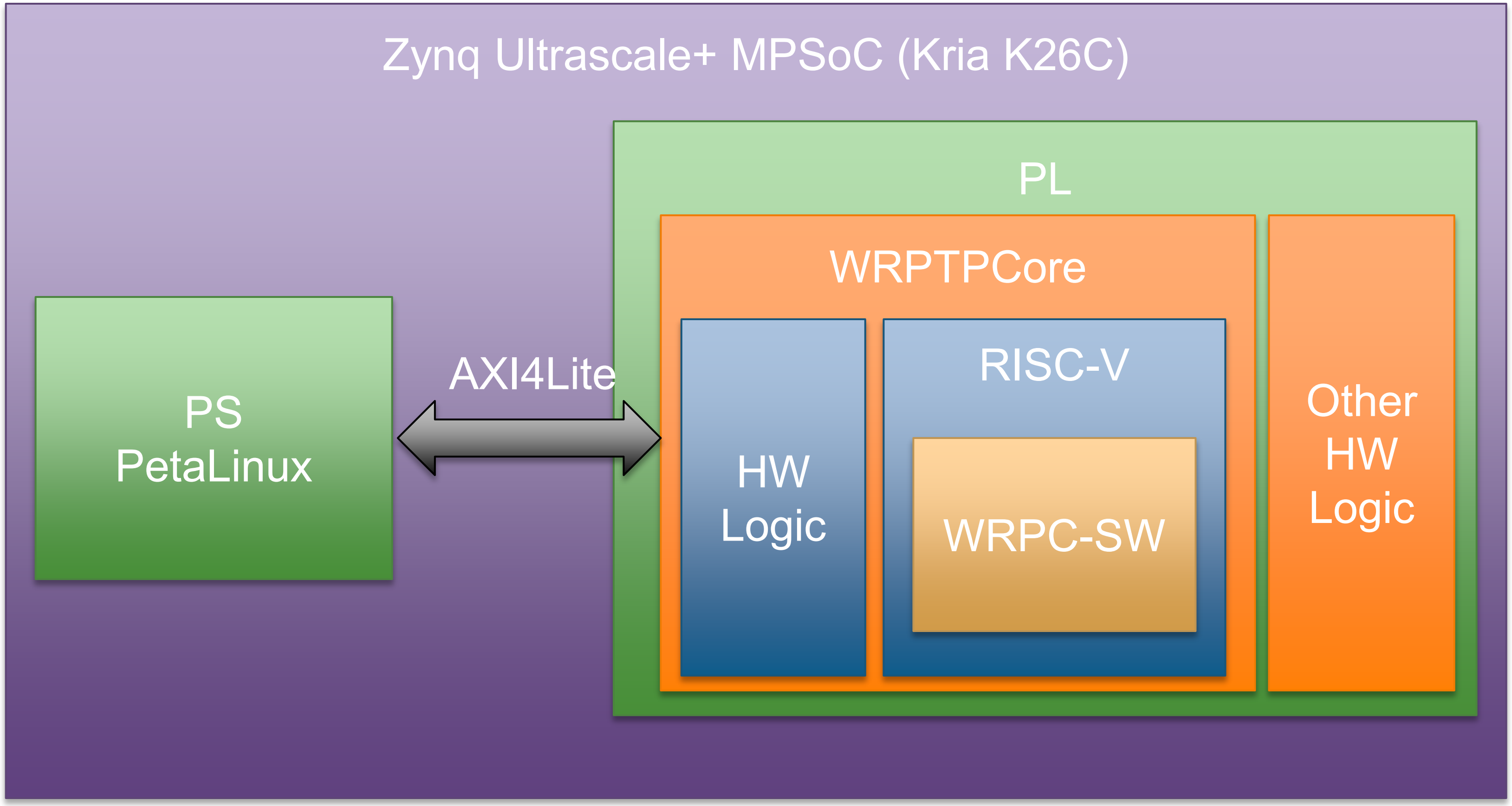
Magnified phase difference



- WR PTP Core
  - $f_{clkA} = 62.5$ MHz
  - $N = 14$
  - Multiplication factor: 16,385

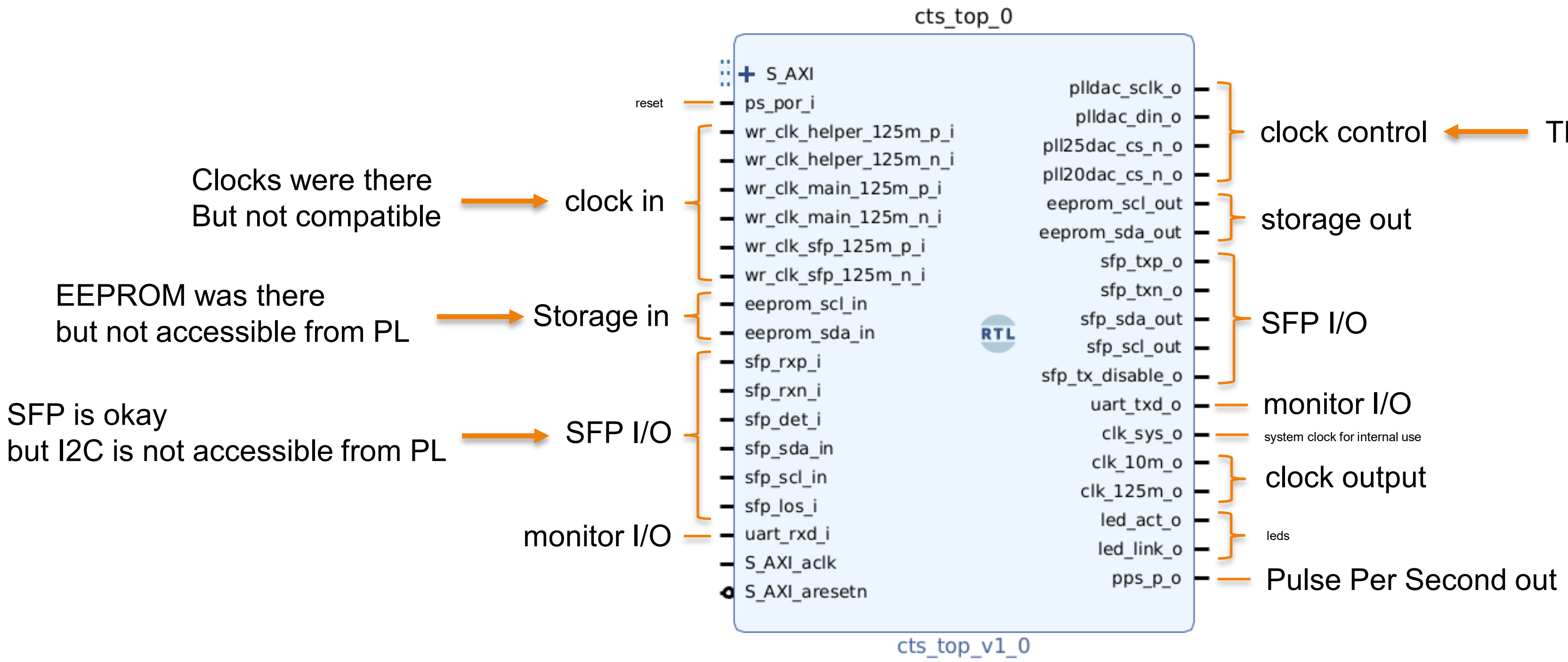
Reference: Precise time and frequency transfer in a White Rabbit network, Tomasz Włostowski, Master of Science Thesis

Over-simplified block diagram



How to implement White Rabbit for CTS?

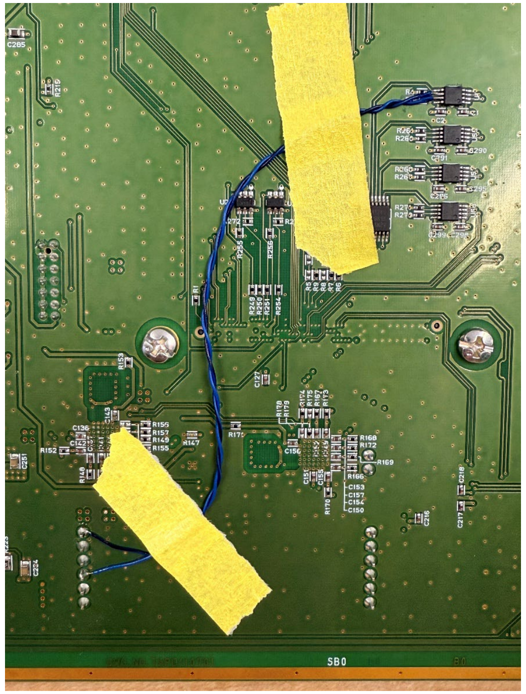
- With complete (or at least close to complete) understanding of WRPTPCore source code, re-write the clock adjusting parts to use components on CTS boards
- Try to put additional components via extension I/Os so that the existing FPGA design works with minimal changes



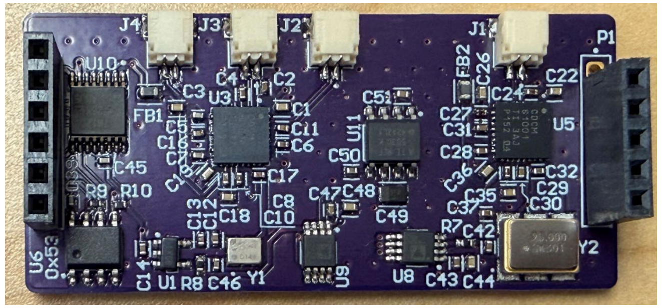
S_AXI*: AXI4 Lite bus pins for accessing internal registers from PS Linux

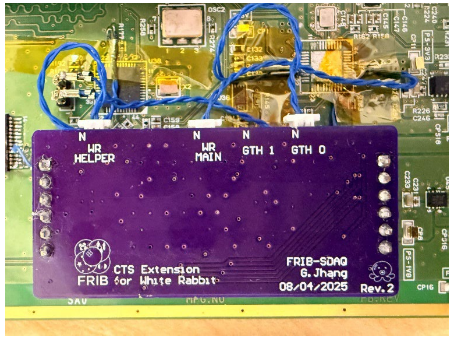
Board modification

- SFP I2C from PL



- CTSExtension board





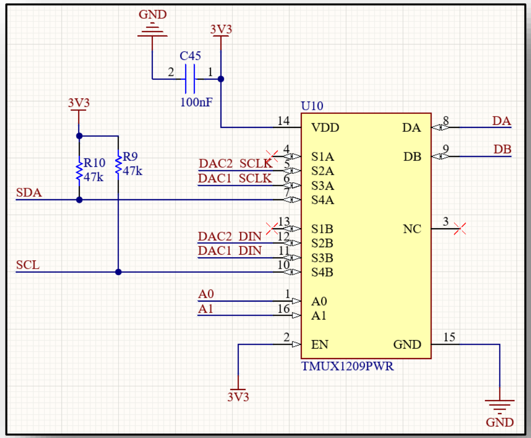
Main XO: O 25,0-JTS32CSV-F-K-3,3-1510-1015-LF

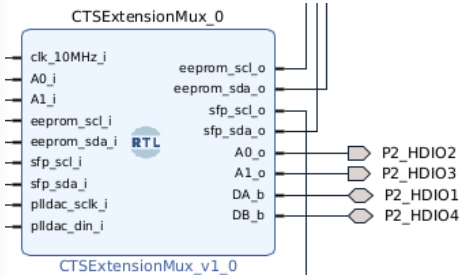
Stability: ±280 ppb
Pullability: ±10~±15 ppm

Helper XO: SVC75C3A48B2-25.000M

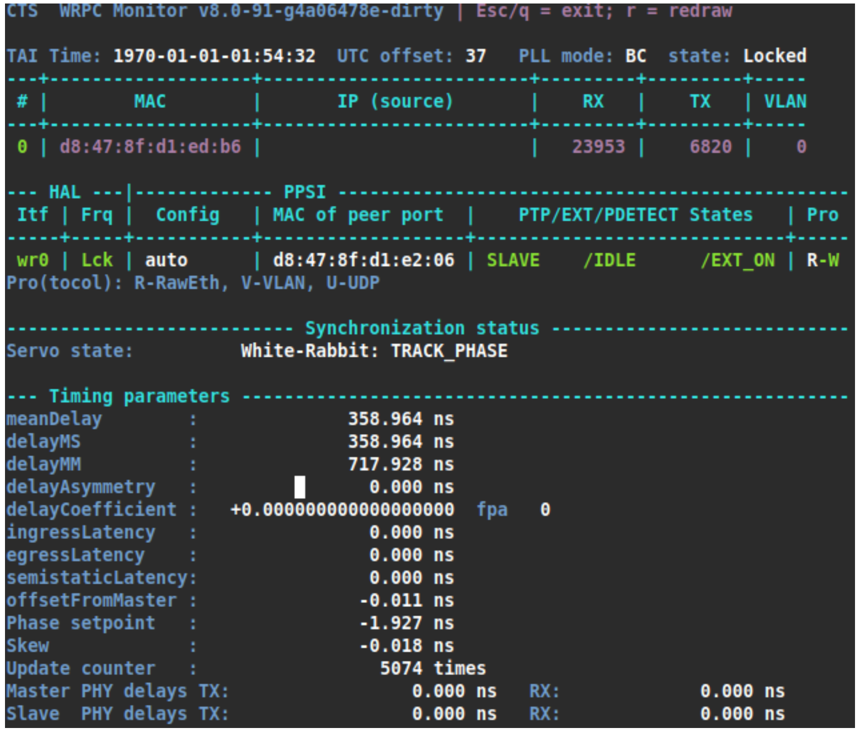
Stability: ±25 ppm
Pullability: ±100 ppm

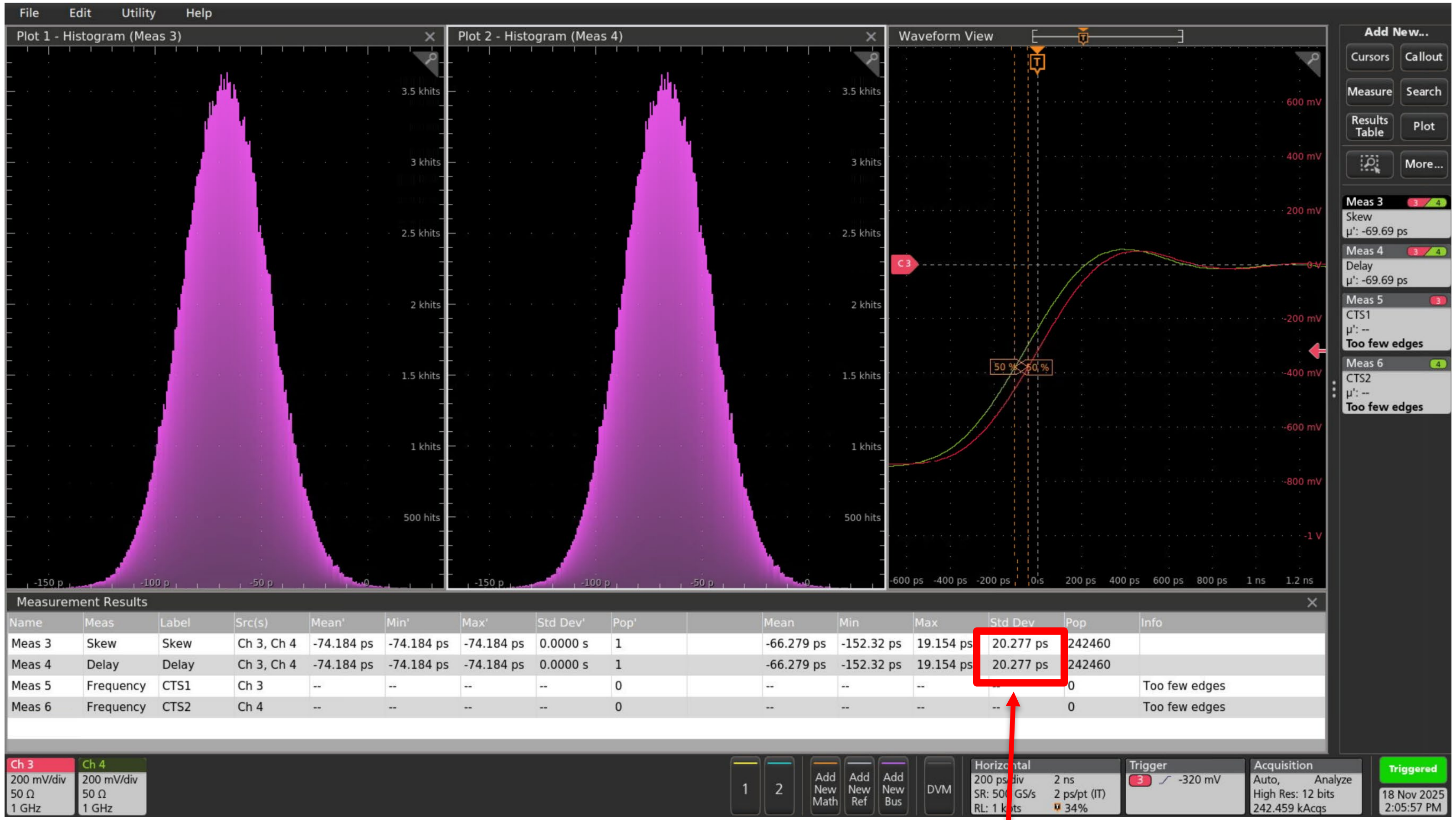
- External clocks frequency adjustable by DAC
- EEPROM for storage
- Multiplexer IC for controlling multiple components in limited pins





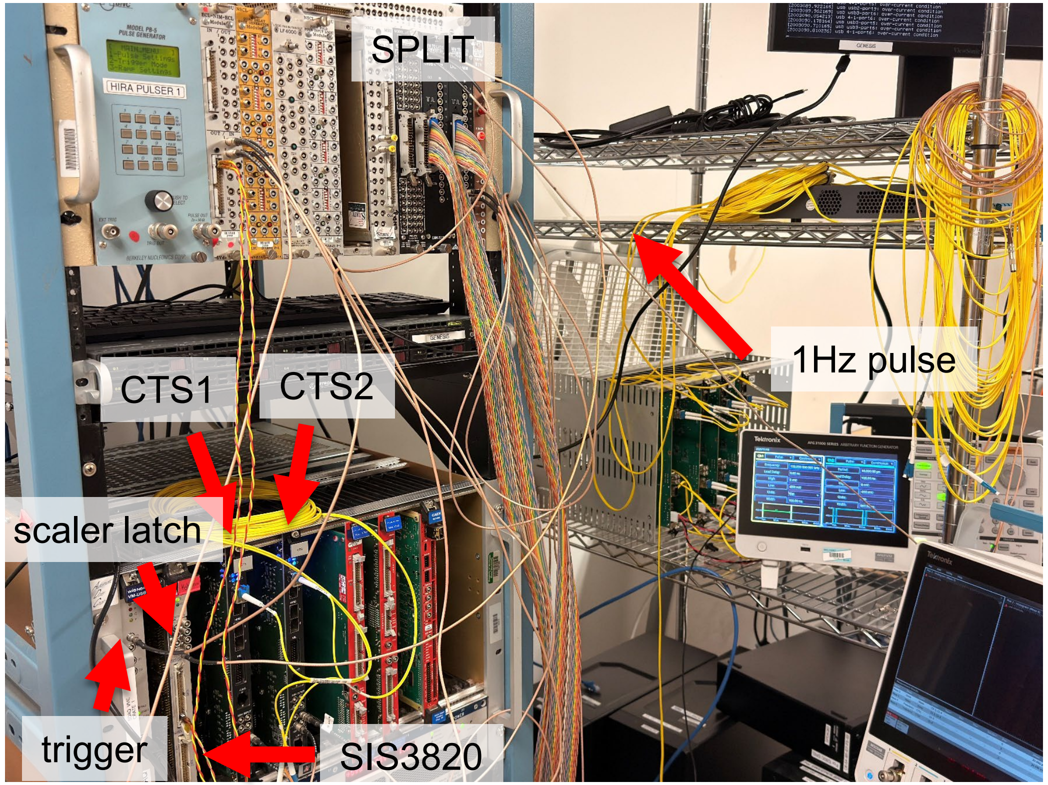
Synchronization status between “CTS”s



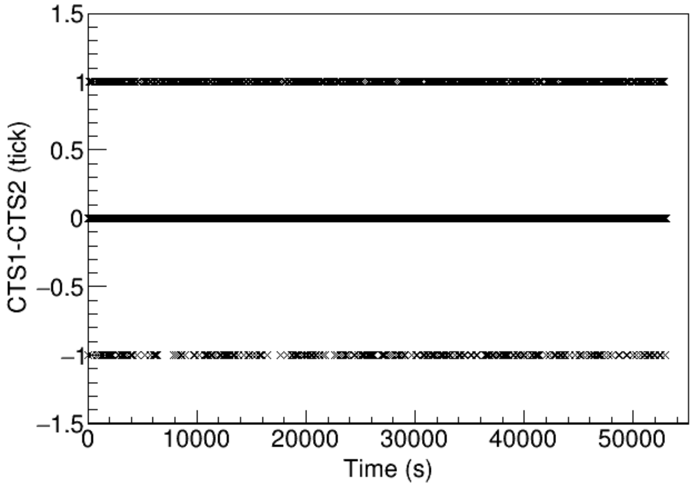


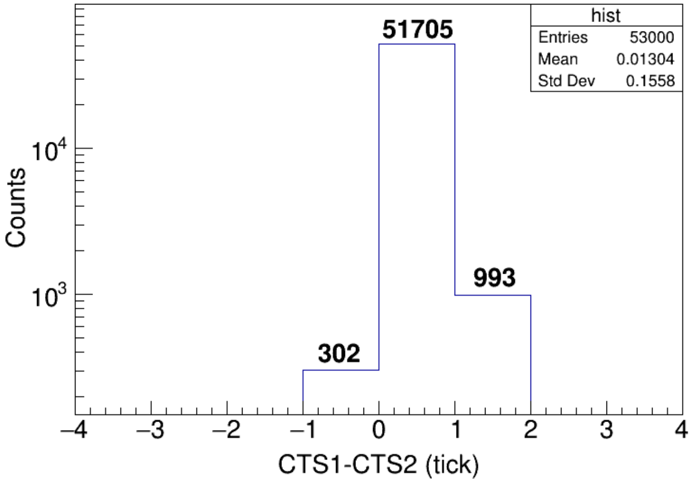
125MHz clocks from CTS1(red) and CTS2(green) are synchronized with ~20ps jitter

SI3820 scaler test of synchronized 125MHz clock



- 125 MHz clocks from each CTS used as inputs to SIS3820 scaler.
- 1Hz pulse from the function generator fed into the scaler latch and VMUSB trigger.
- Two clocks counted over ~15hours stay stable within ±8ns (± 1 tick).



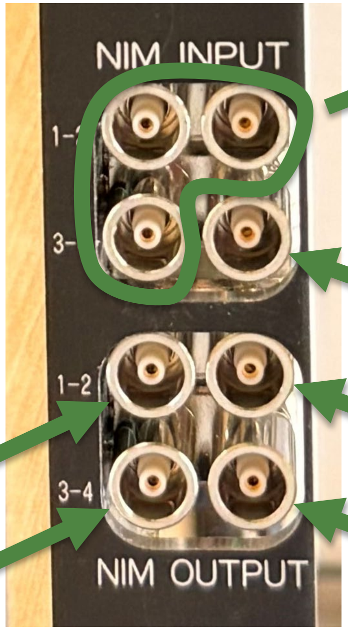


FRIB
Facility for Rare Isotope Beams
U.S. Department of Energy Office of Science | Michigan State University
640 South Shaw Lane • East Lansing, MI 48824, USA
frib.msu.edu

Clock output configuration for NIM IO ports

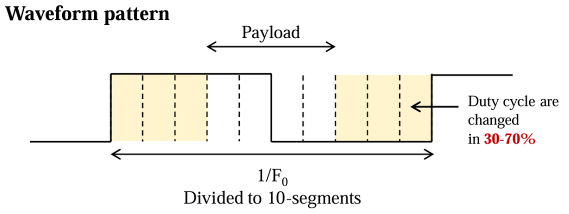
- 10 MHz clock and PPS signal are provided by default in case of the use of CTS as a GrandMaster.
- NIM O3 is set to 125 MHz clock programmable by NIM I1-3
- NIM O4 is emitting constant 1 for setting the inputs using fan-in/fan-out.
- NIM I4 is used for resetting only WRPC SW without restarting the module or power cycling the crate.

IN 3	IN 2	IN 1	OUT 3
0	0	0	125 MHz
0	0	1	20 MHz
0	1	0	25 MHz
0	1	1	50 MHz
1	0	0	100 MHz
1	0	1	Not programmed
1	1	0	Not programmed
1	1	1	Not programmed



MIKUMARI firmware for CTS (CTS-MIKUMARI)

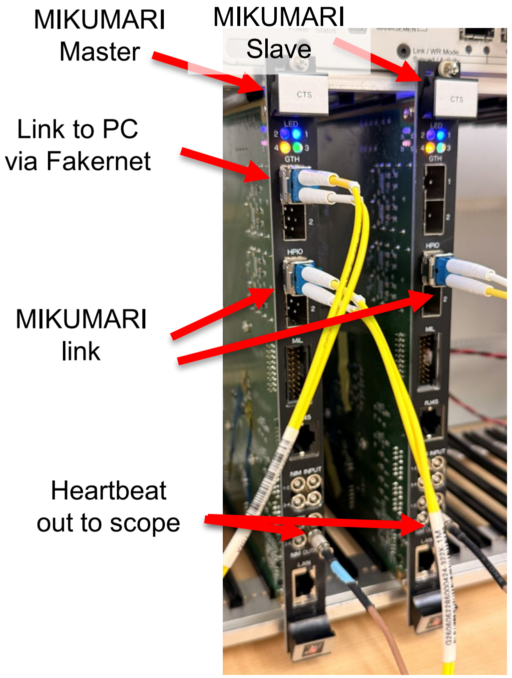
- MIKUMARI protocol [1] is a protocol based on the Clock Duty Cycle Modulation (CDCM) technique [2].
- Originally firmware is developed for AMANEQ board with Kintex-7 (XC7K-160T-2FFG676C).
- R. Honda provided the core packages of MIKUMARI protocol on Zynq Ultrascale+.
- Fakernet is implemented partly to replace the SiTCP (not supported ZU+) for diagnostics information retrieval.

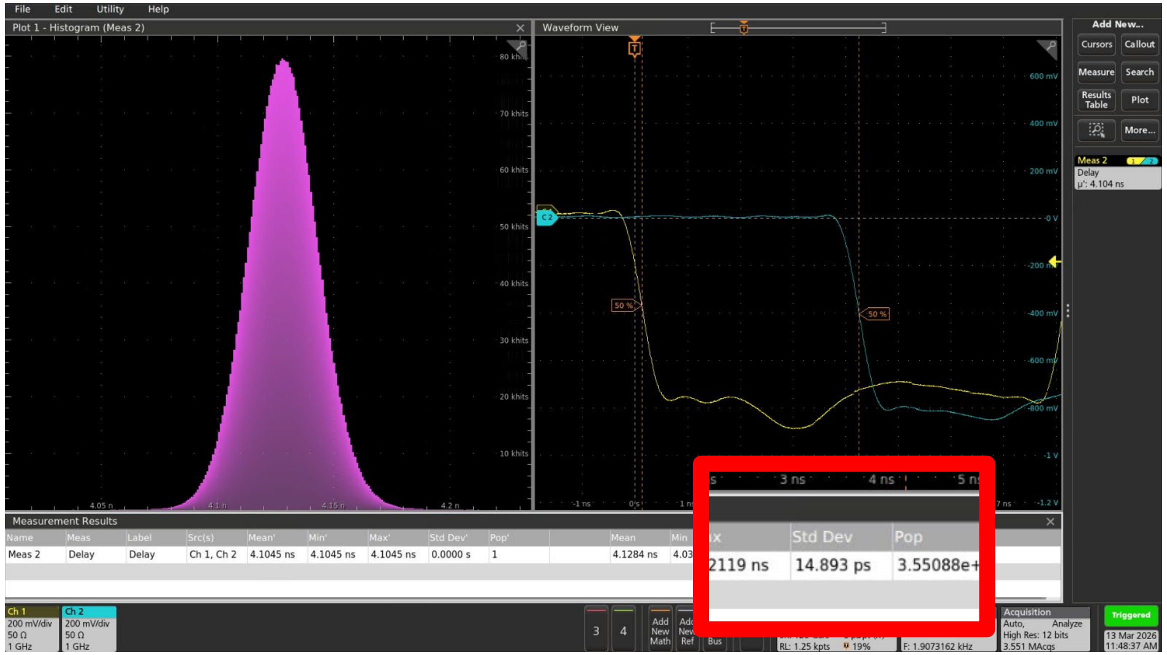


CDCM-10-2.5

CDCM-10-2.5 encode table

Binary	Encoded
00	0000
01	0001
IDLE	0011
10	0111
11	1111





[1] R. Honda: https://ieeexplore.ieee.org/document/10098185
[2] D. Calvet: https://ieeexplore.ieee.org/document/9131833

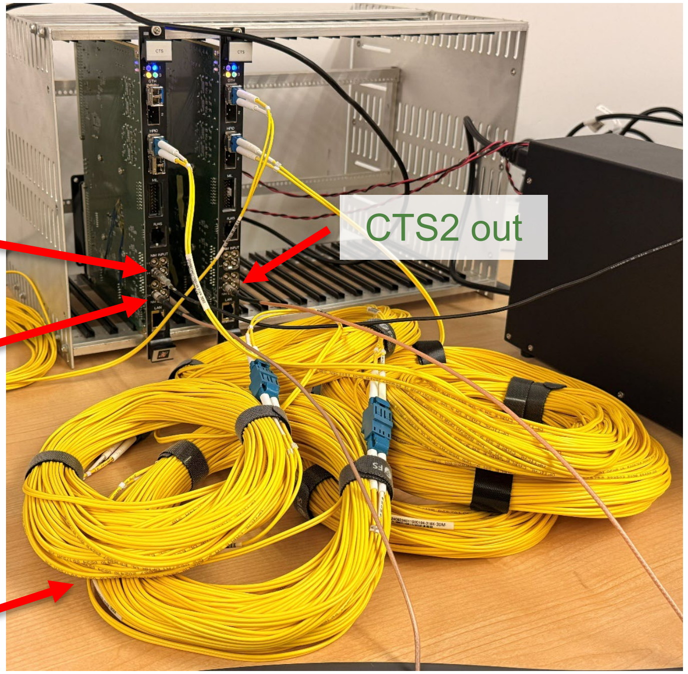
Delayed synchronized signal distributor with CTS-MIKUMARI

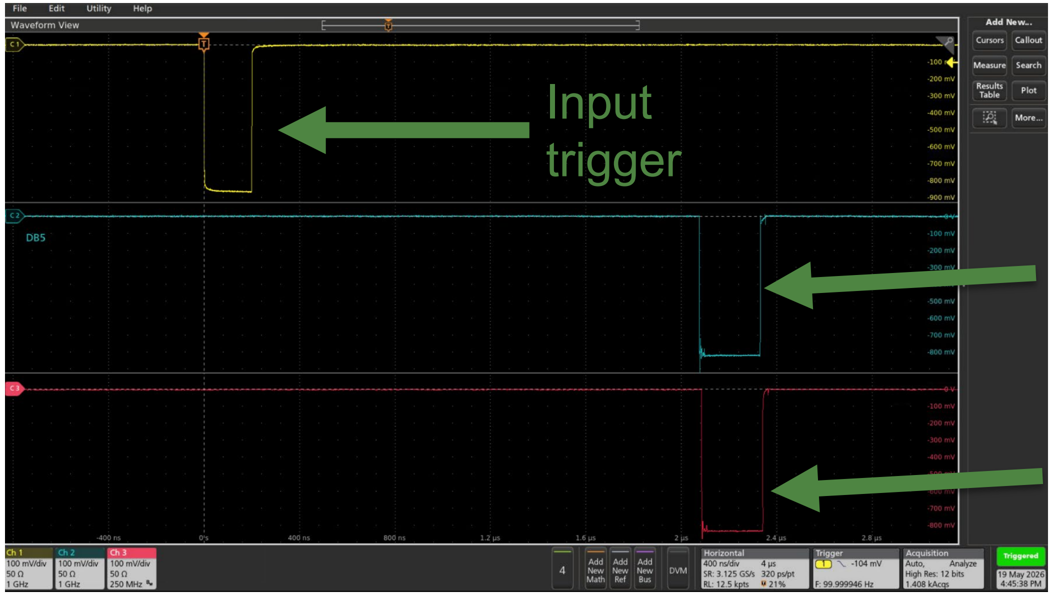
- Local area common clock protocol (LACCP) frame has 5 reserved bits.
- Input signals from either end of CTS are transferred to the other end and emitted at the same time after 2us to take into account the propagation time.

Trigger in

CTS1 out

200m fiber
(1us delay)





Synchronized trigger output from CTS1

Synchronized trigger output from CTS2

Summary

- White Rabbit and MIKUMARI firmwares are developed for CTS board as a translator between different time domains between streaming readout electronics and conventional trigger-based electronics.
- White Rabbit provides synchronized clocks with jitter ~20ps (RMS).
  - Many different clock frequencies available and configurable
- MIKUMARI provides syntonized clocks with jitter ~14ps (RMS).
  - Delayed synchronized signal

Future plans

- Building a web interfaces
  - Switching one firmware to the other firmware
  - Configuring output clock frequencies (CTS-WhiteRabbit)
  - Configuring the delay time of synchronized signals and the number of channels (CTS-MIKUMARI)
- Developing a new firmware connecting White Rabbit and MIKUMARI
  - CTS becomes White Rabbit master and shared clock with CTS-MIKUMARI master