IEEE NPSS NUCLEAR & PLASMA SCIENCES SOCIETY

25th IEEE Real Time Conference

Early Statistical Estimation for Data Rate Optimization in Dark Count Limited Detectors Using Fully-Analog Processing

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UNIVERSITAT POLITÈCNICA DE VALÈNCIA

Donostia International Physics Center

next

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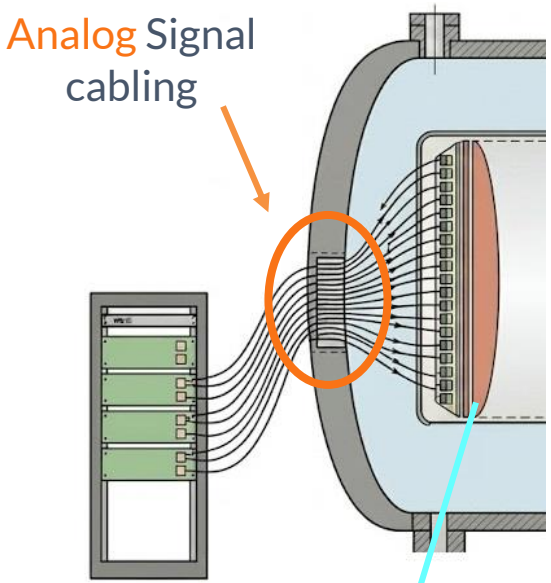
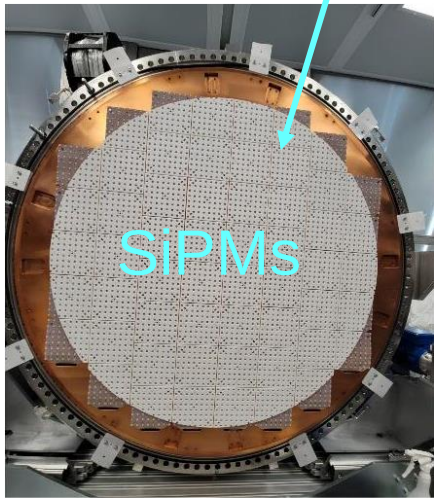
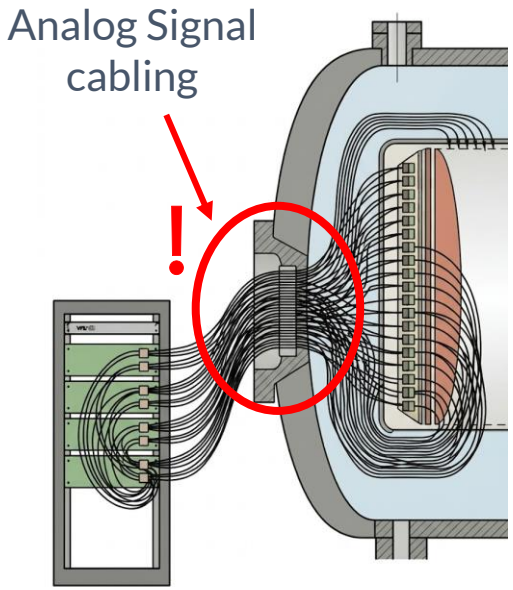
TPCs Evolution





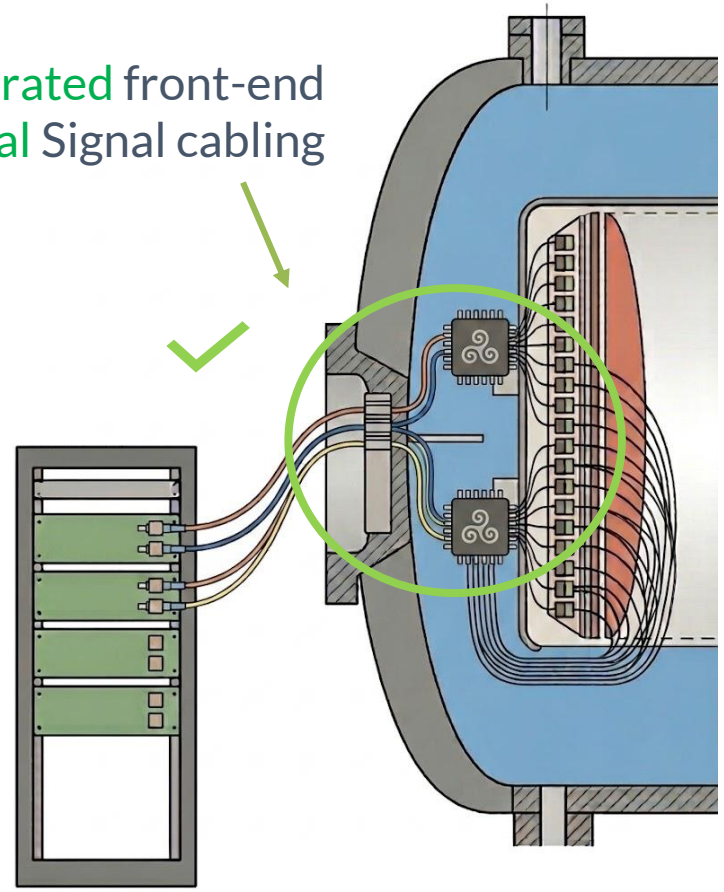


Signal distortion (Crosstalk)

Feedthrough Complexity

High Density Plane

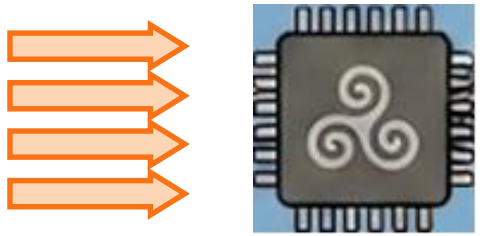
High Dark Count Rate



Needs

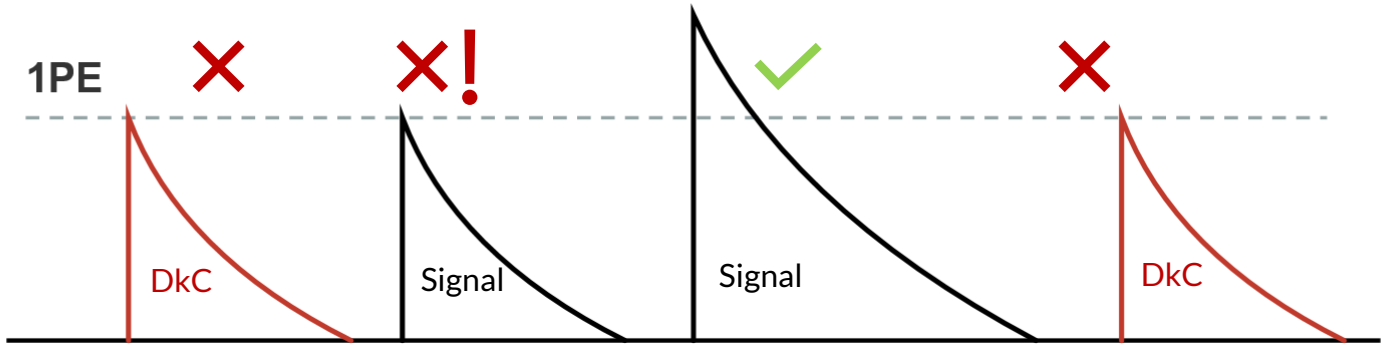
- Channel Management Solution → **ASIC**

SiPM Analog Inputs



Fast Digital Output

- Standard ASIC Solution → **Slow Path** (Preamplifier + Integrator + ADC)
- Standard DkC Solution → **Pe Threshold**



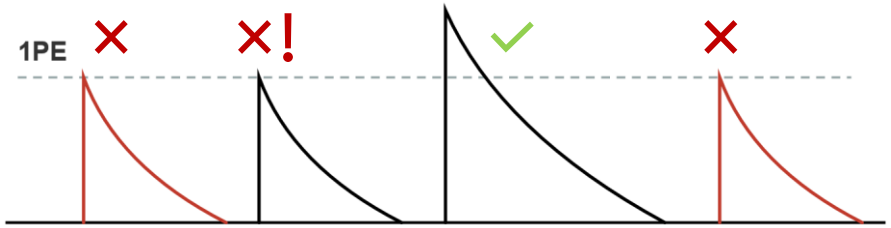
DkC properly filtered

Signal information Lost !

Solution proposed

Early Statistical Estimation for Data Rate Optimization in Dark Count Limited Detectors Using Fully-Analog Processing

- Amplitude Threshold



- **Statistical Threshold** ≈ DkC vs. Signal
  - **DkC Rejection**
  - **Signal Recovery**
- **Early processing** ⇨ Full-Analog Implementation

Solution proposed

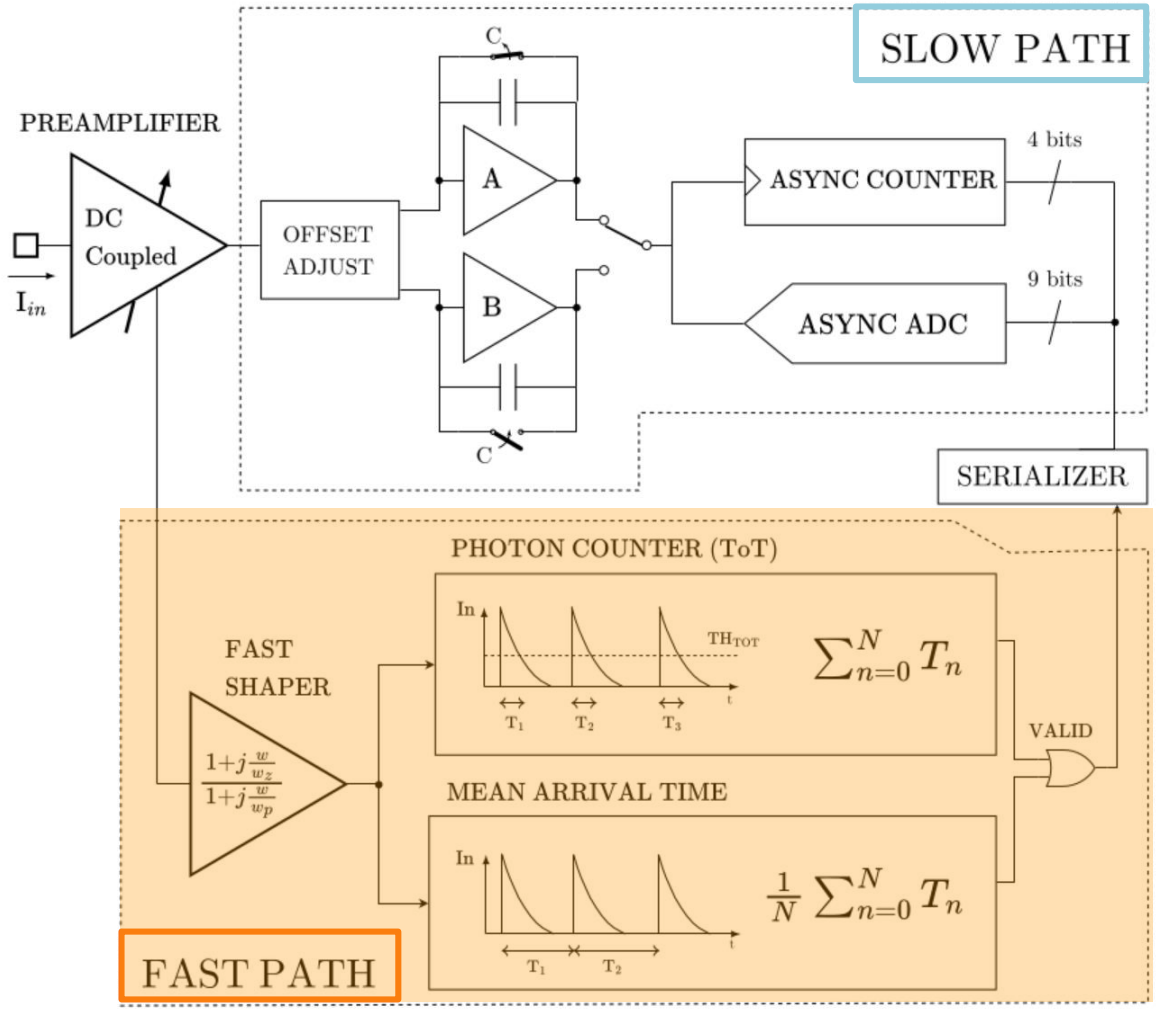
Slow Path

(Preamplifier + Integrator + ADC)

Working in parallel

Fast Path

Photon Couting Statistics

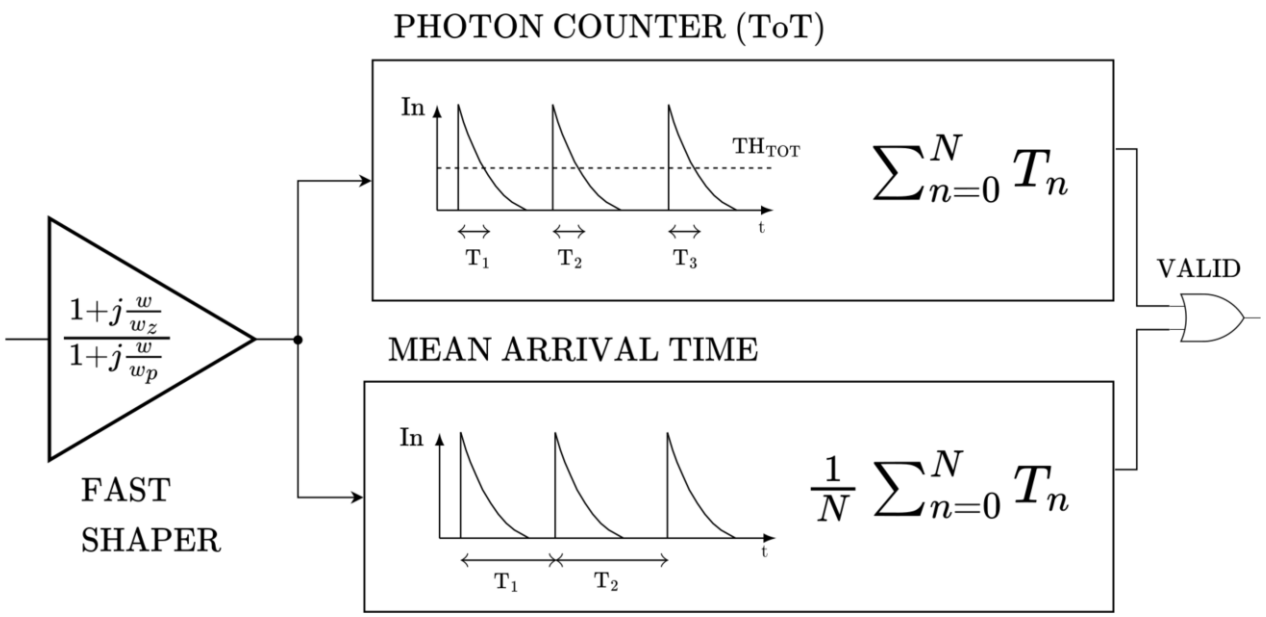


Fast Path Architecture

Statistical estimator

Fully-analog Implementation

Pile-up effects overcome



Dark Count Rejection

Information and Signal Trigger

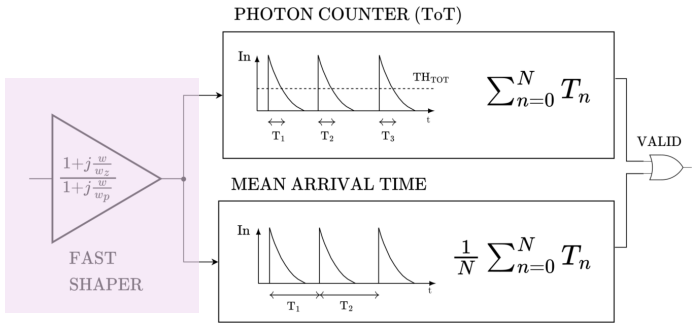
Integrating Time Window based Systems

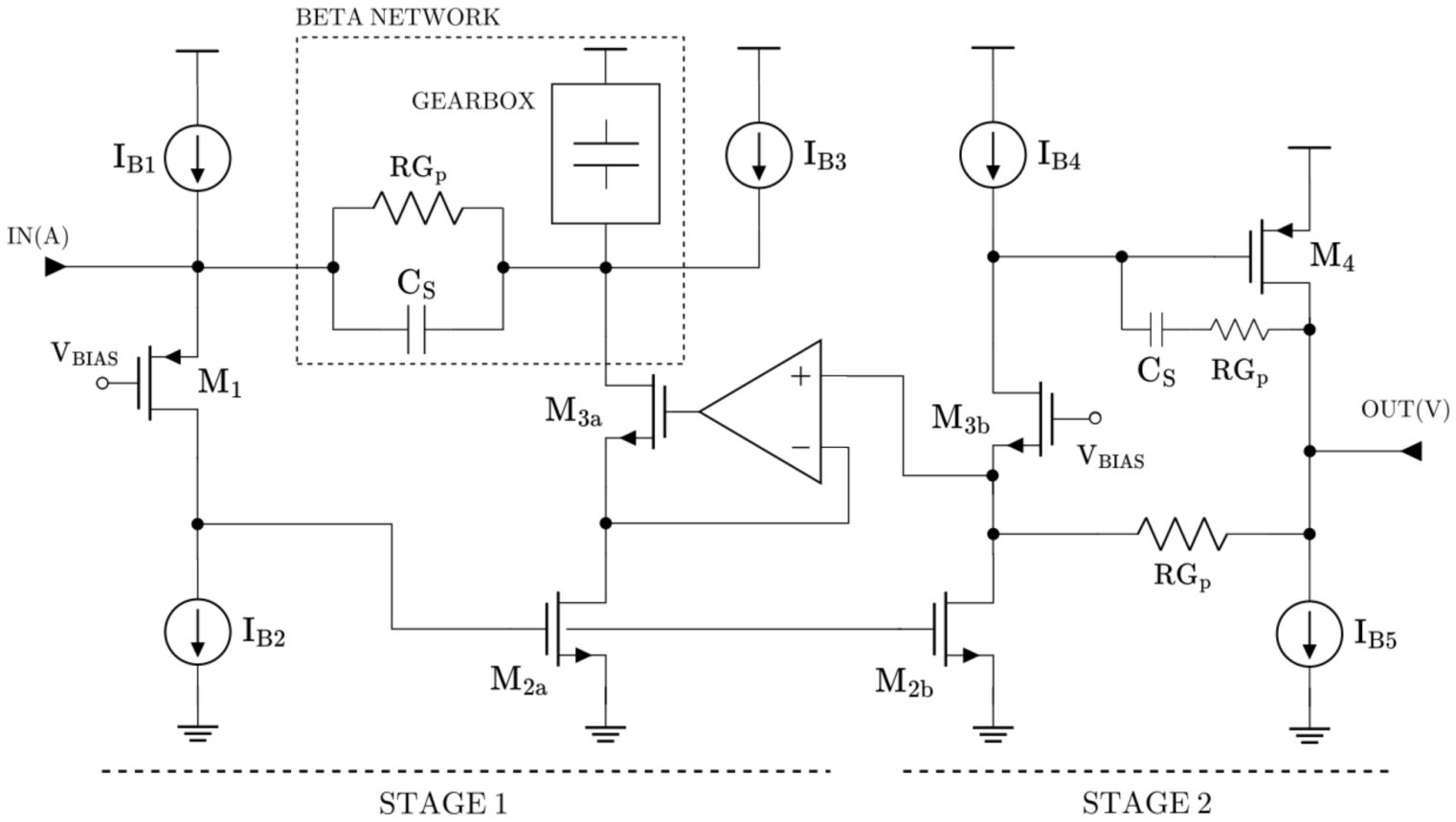
Signal recovery

Low Power Consumption

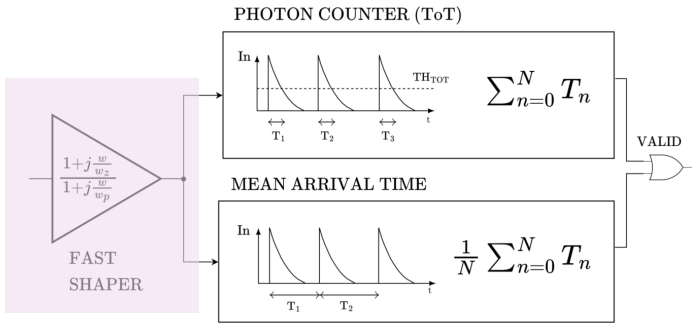
Fast Shaper Module

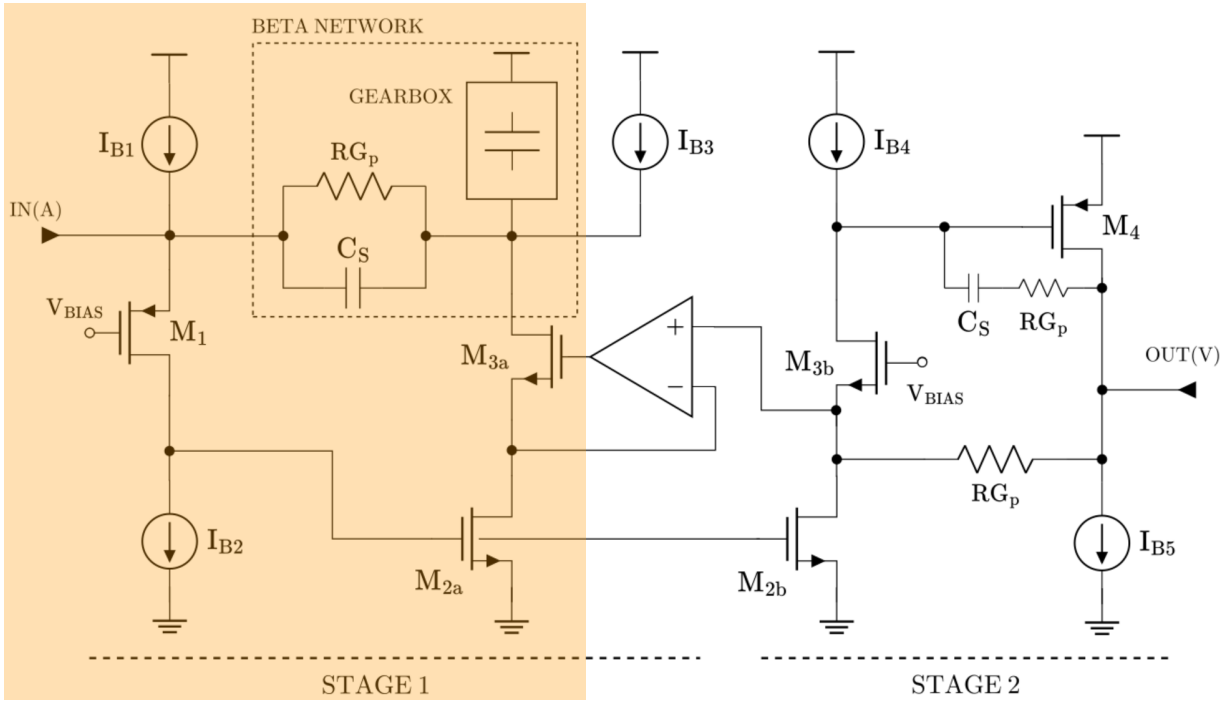
2 Stages | Fast Shaping
Current-Voltage Converter





Fast Shaper Module





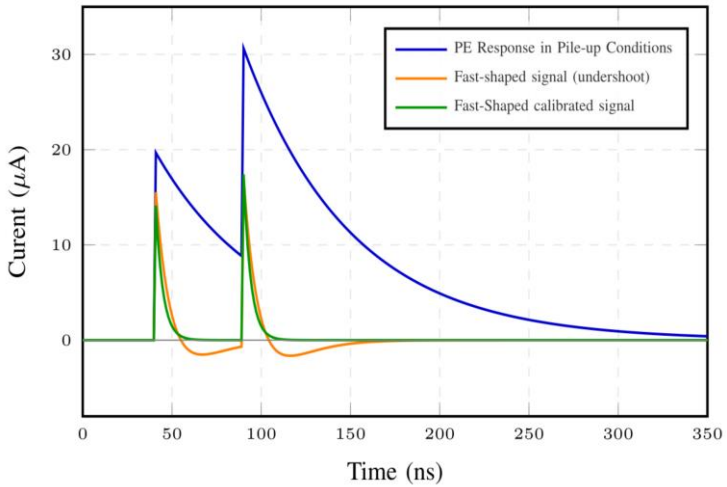
Deal with Pile-Up problems

Make PE Response faster

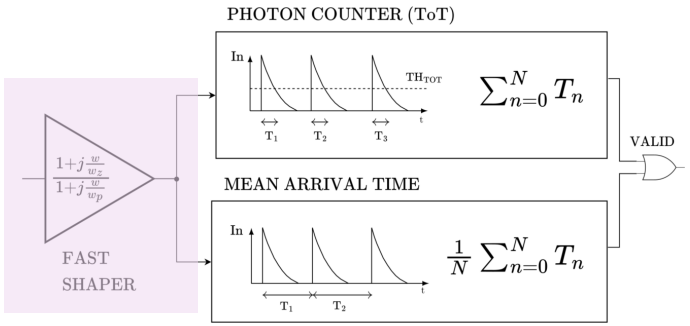
Calibration Algorithm to eliminate undershoot

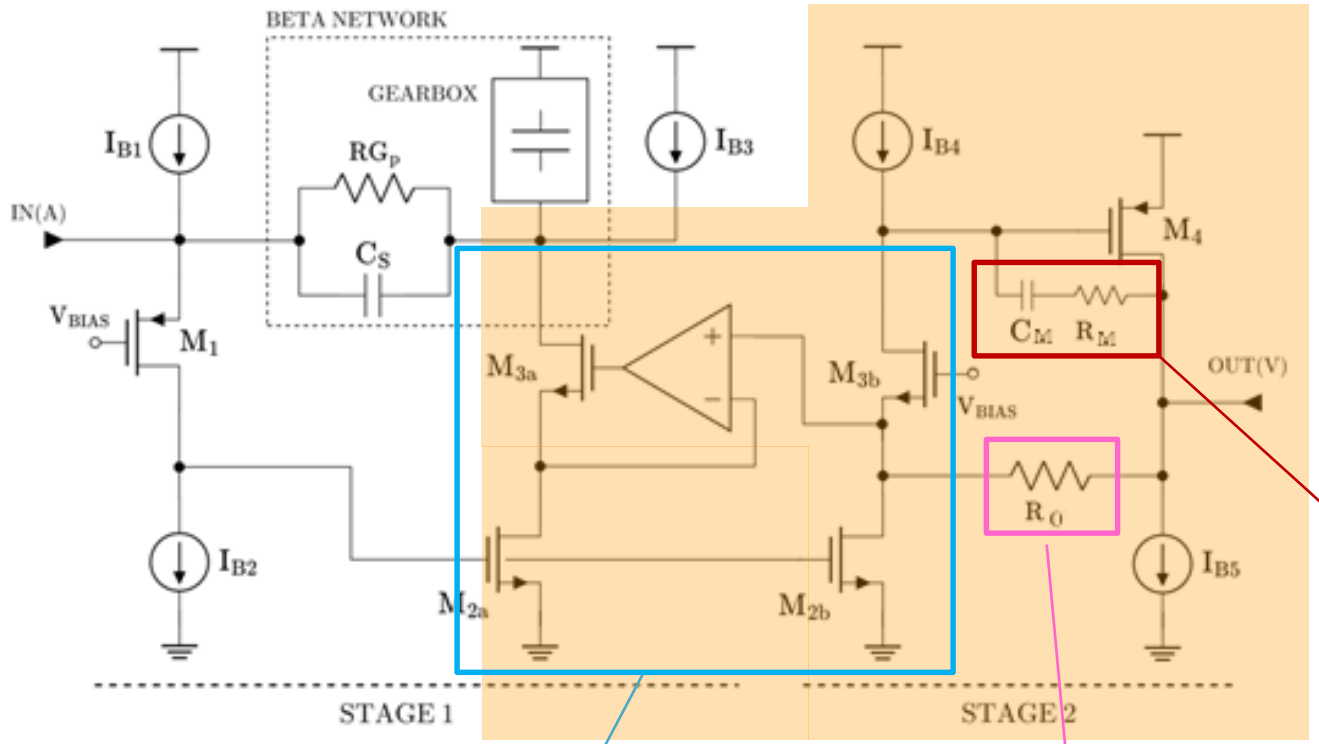
Pole-Zero cancellation $\frac{1}{1+s/\omega_{p_0}} \cdot \frac{1+s/\omega_z}{1+s/\omega_p} = \frac{1}{1+s/\omega_p}$

Filter in Feedback Loop $H_{filter} = \frac{1}{\beta} = \frac{1+R_{Gp}\ s(C_{gearbox}+C_s)}{1+R_{Gp}\ sC_s}$



Fast Shaper Module





Current-Voltage Conversion

Coming stages have several voltage comparators

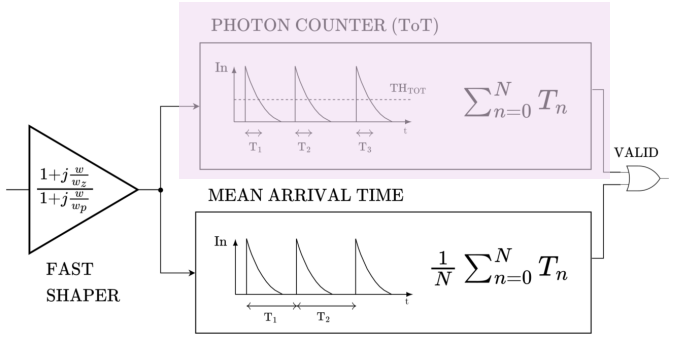
Input Voltage NEEDED

Regulated Cascode Current Mirror

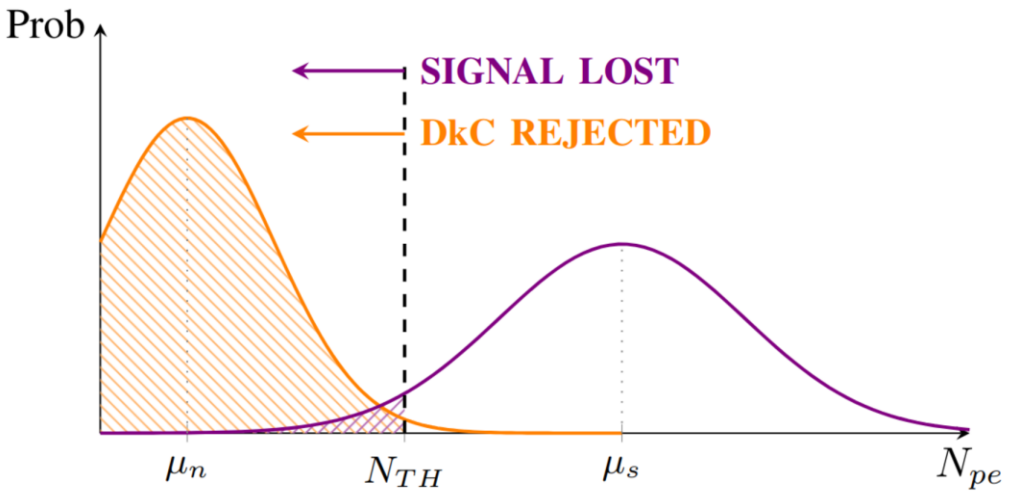
High Gain Loop

Stable Frequency Response with Miller Compensation

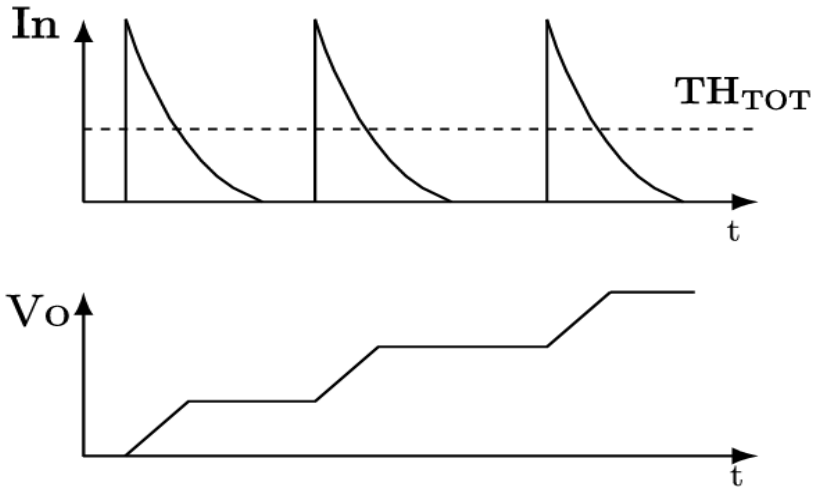
Photon Counting Module



Poisson Counting Statistics



$\lambda_{signal} > \lambda_{DkC}$



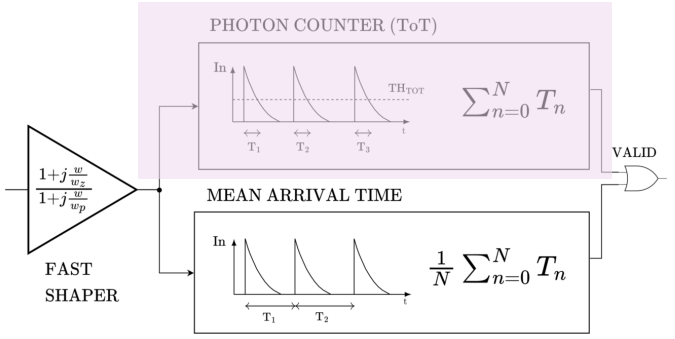
Time Over Threshold (TOT)

Counting photons inside Time Windows

$N_{TH} \uparrow\uparrow$ | ↑ DC Rejection ✓
↑ Signal Loss ✗

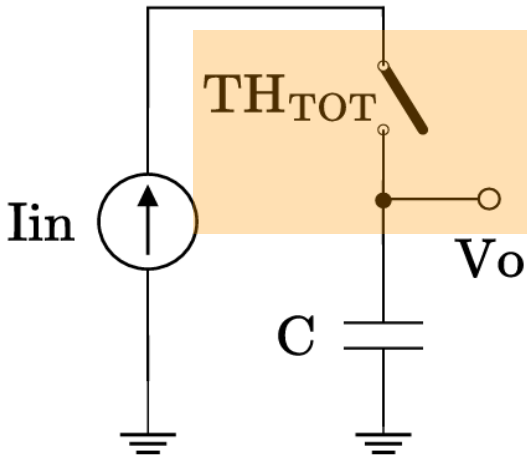
TRADE-OFF

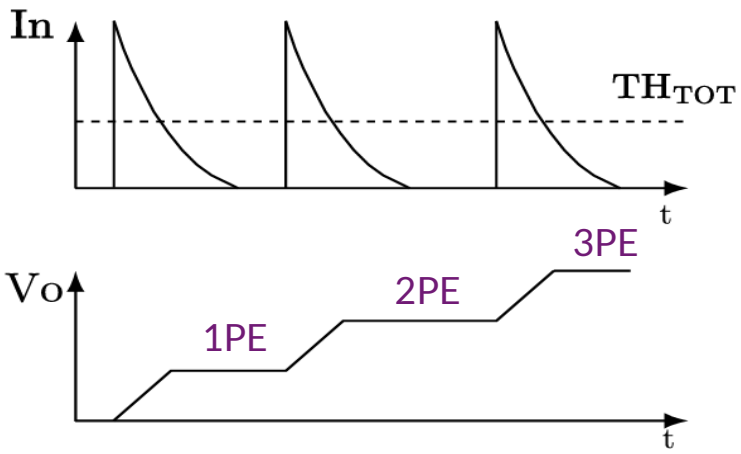
Photon Counting Module



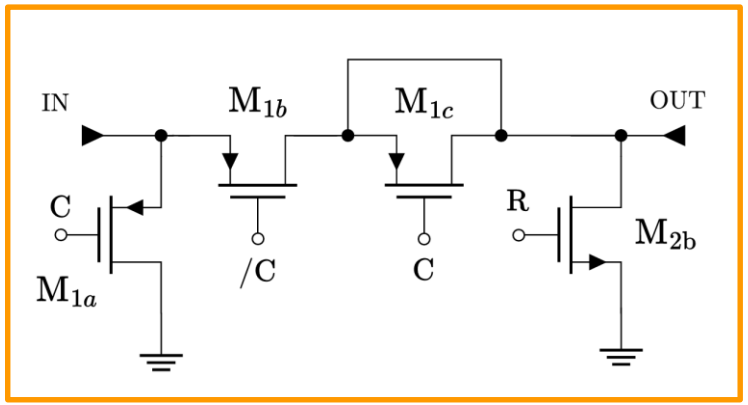
Straight forward Implementation

Current Source + Switch * + Capacitor



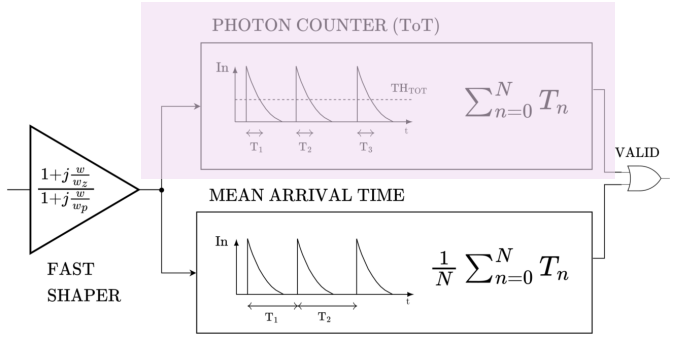


* Current Steering Switch



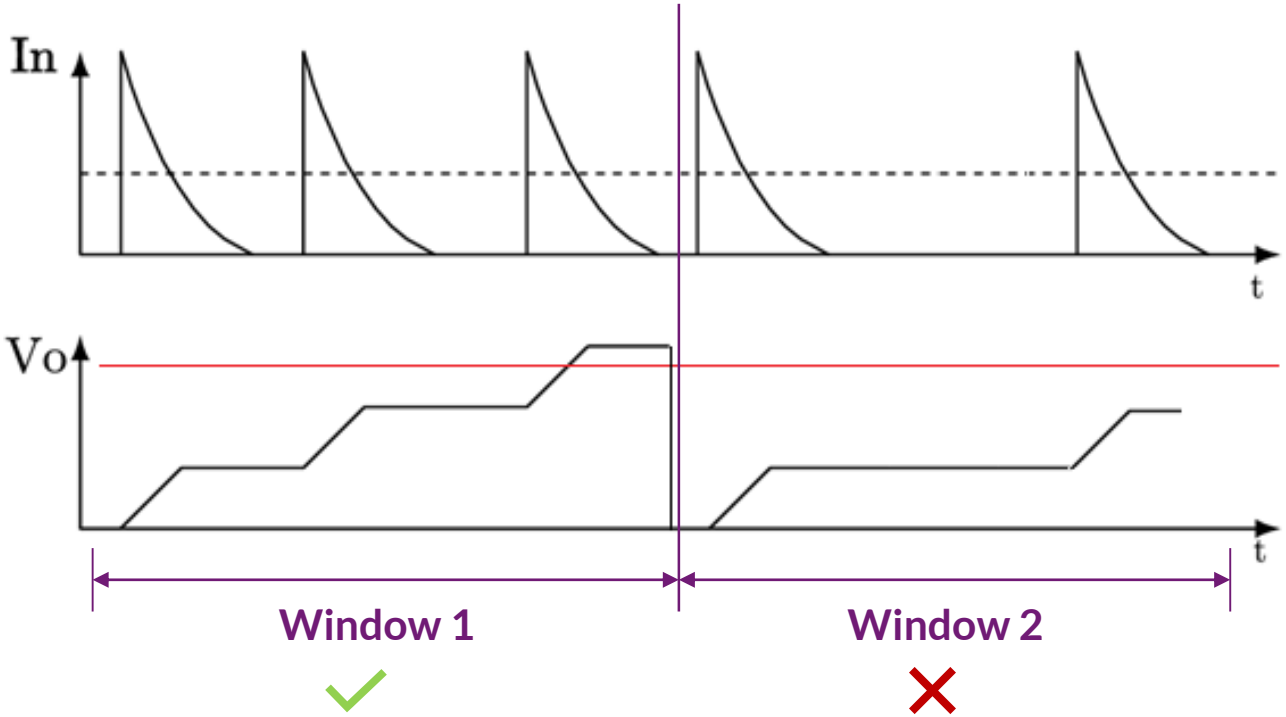
Vo **proportional** to Number of Photons in a Window

Photon Counting Module



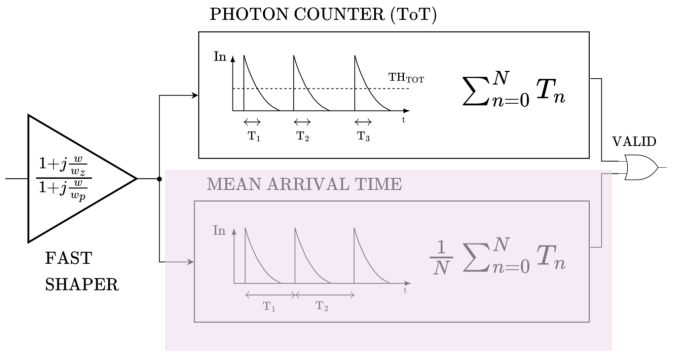
Below N_{TH} some signal is lost due to statistics and time windows division

Signal of 5 PEs accross windows

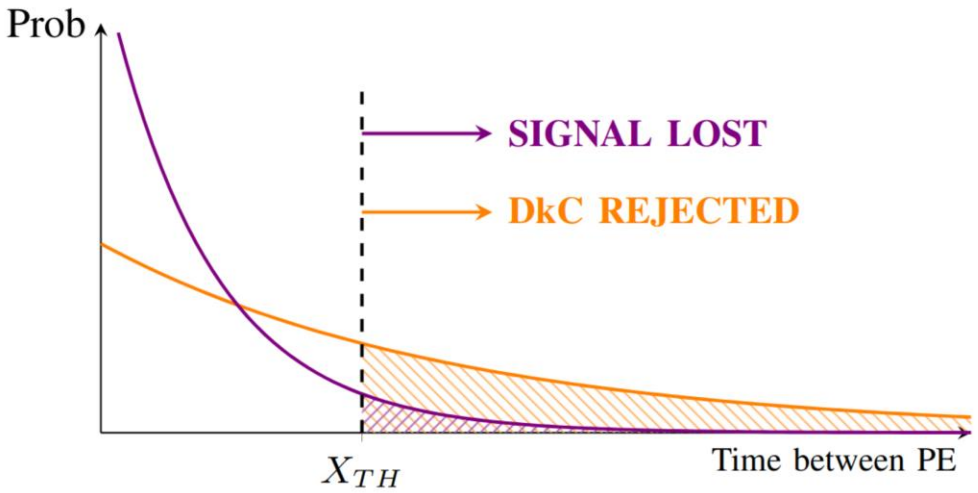


N_{TH} > 2PEs

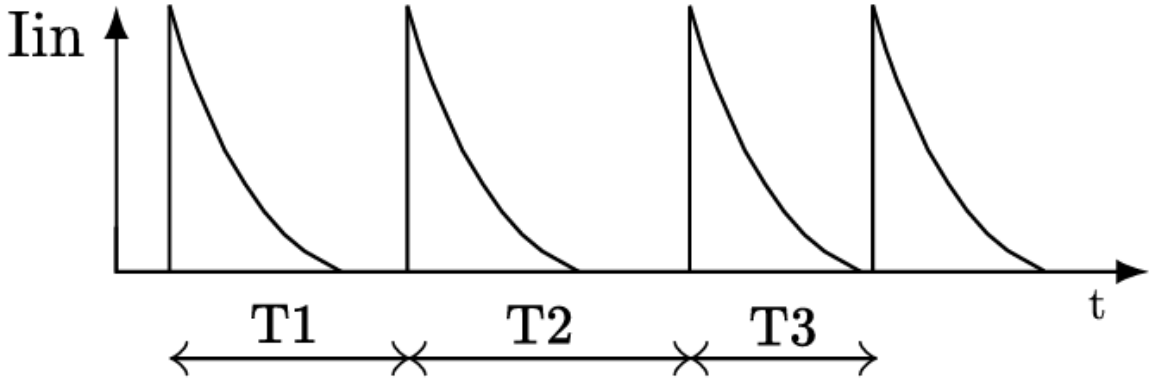
Mean Arrival Time Module



Exponential Time Statistics



$$\frac{1}{N}\sum_{n=0}^{N} T_n$$



$\lambda_{signal} > \lambda_{DkC}$

$X_{TH} \downarrow\downarrow$ | ↑ DC Rejection ✓
↑ Signal Loss ✗

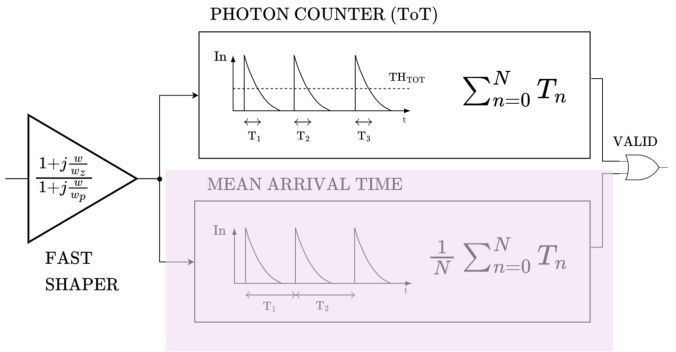
TRADE-OFF

Mean Arrival Time Measurement

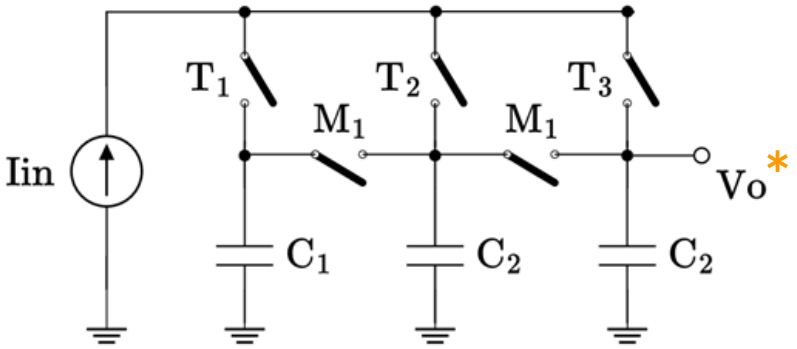
Recover signal photons below PE threshold

Works accross several time windows

Mean Arrival Time Module



Mean Computation Principle

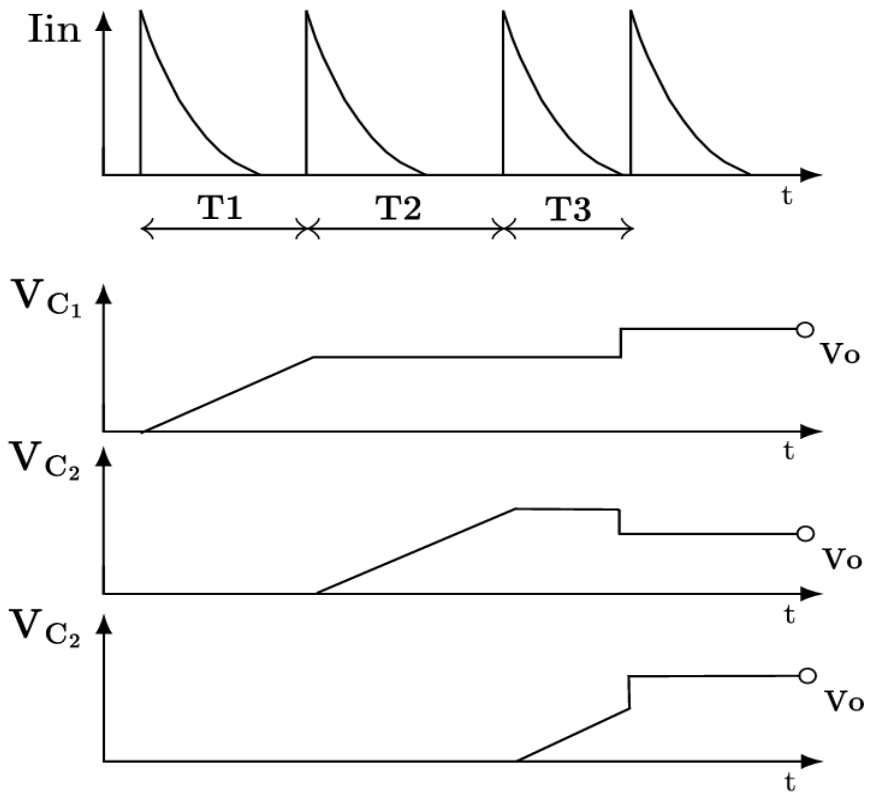


* Charge Sharing among Capacitors

$$V_{C1} = \frac{I_{CTE}}{C} T_1 \qquad V_{C2} = \frac{I_{CTE}}{C} T_2 \qquad V_{C3} = \frac{I_{CTE}}{C} T_3$$

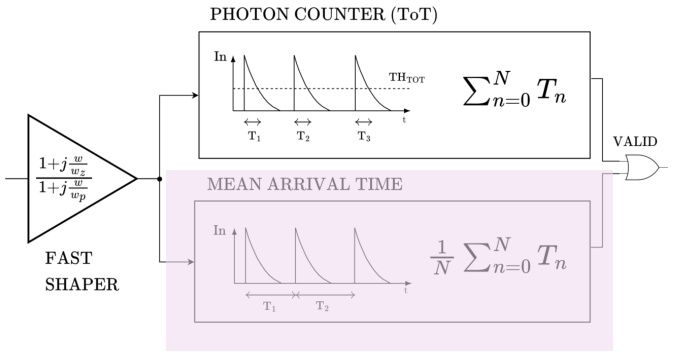
$$V_O = \frac{V_{C1}.C + V_{C3}.C + V_{C3}.C}{3.C}$$

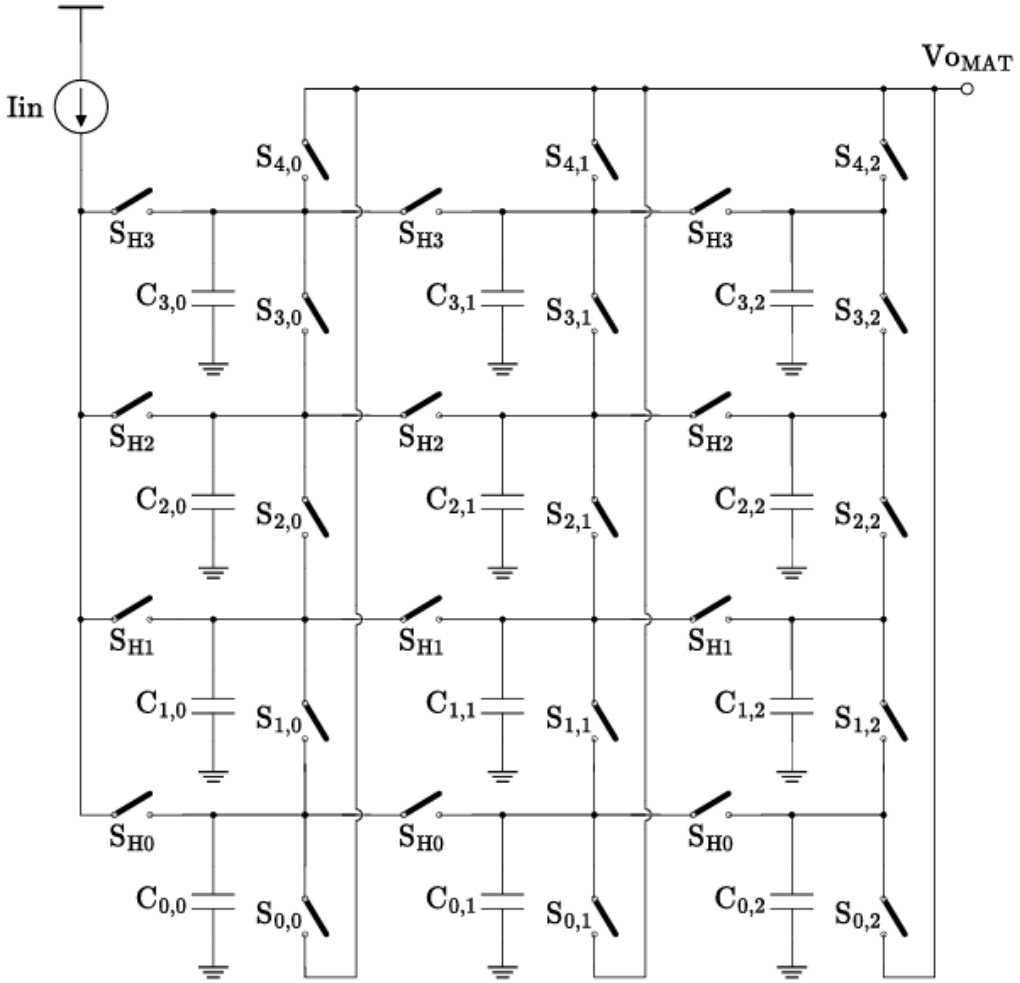
$$V_o = \frac{I_{CTE}}{C} . \frac{\sum_1^N T_n}{N}$$



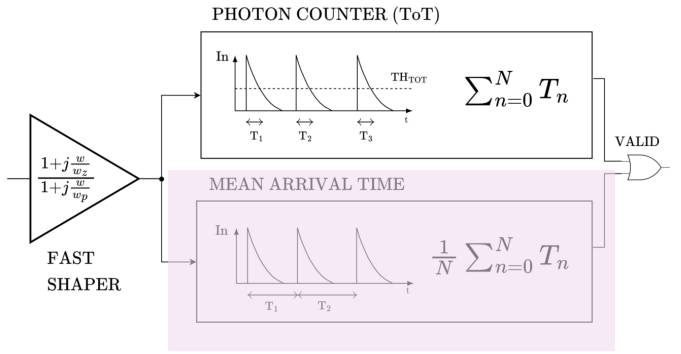
⚠ Information is lost after mean operation

Mean Arrival Time Module



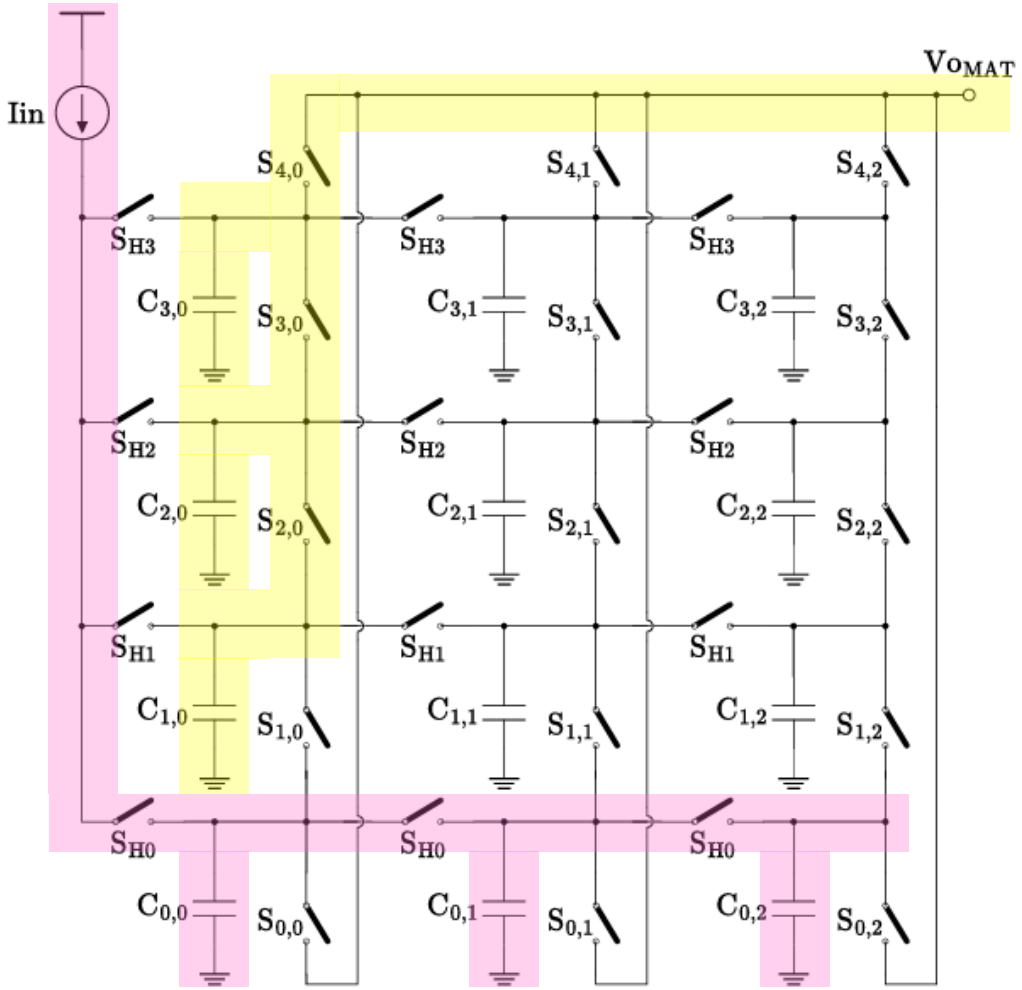


Mean Arrival Time Module



Arrival Time Measurement

Mean Computation

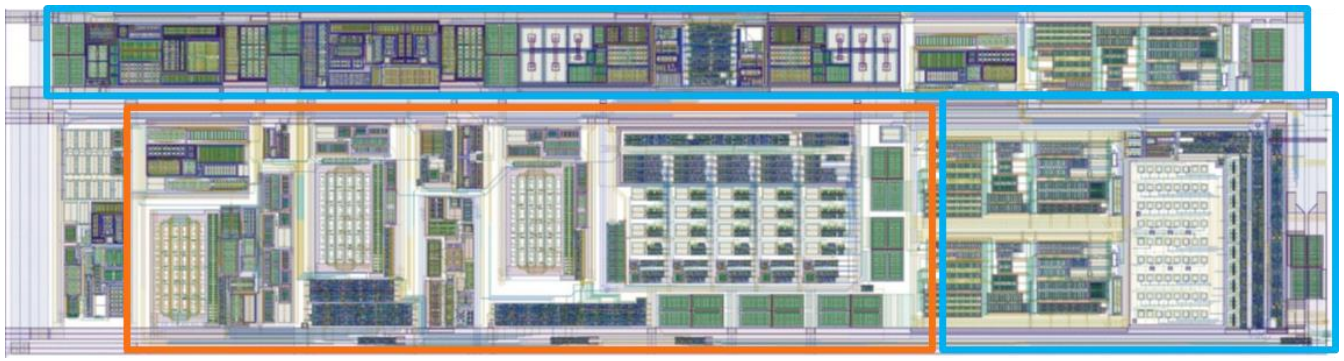


Simulation Results

Full System (PC + MTA)		
PE > 1	DkC Rejected	Signal Lost
Th time = 560 ns	53%	4.44%
Th time = 600 ns	50%	2.96%
PC		
	DkC Rejected	Signal Lost
PE > 1	77%	55%
MTA		
	DkC Rejected	Signal Lost
Th time = 600 ns	56.6%	3.25%

TRISK-J

Threshold signal Recovery and Improvement for Statistical darK count reJection



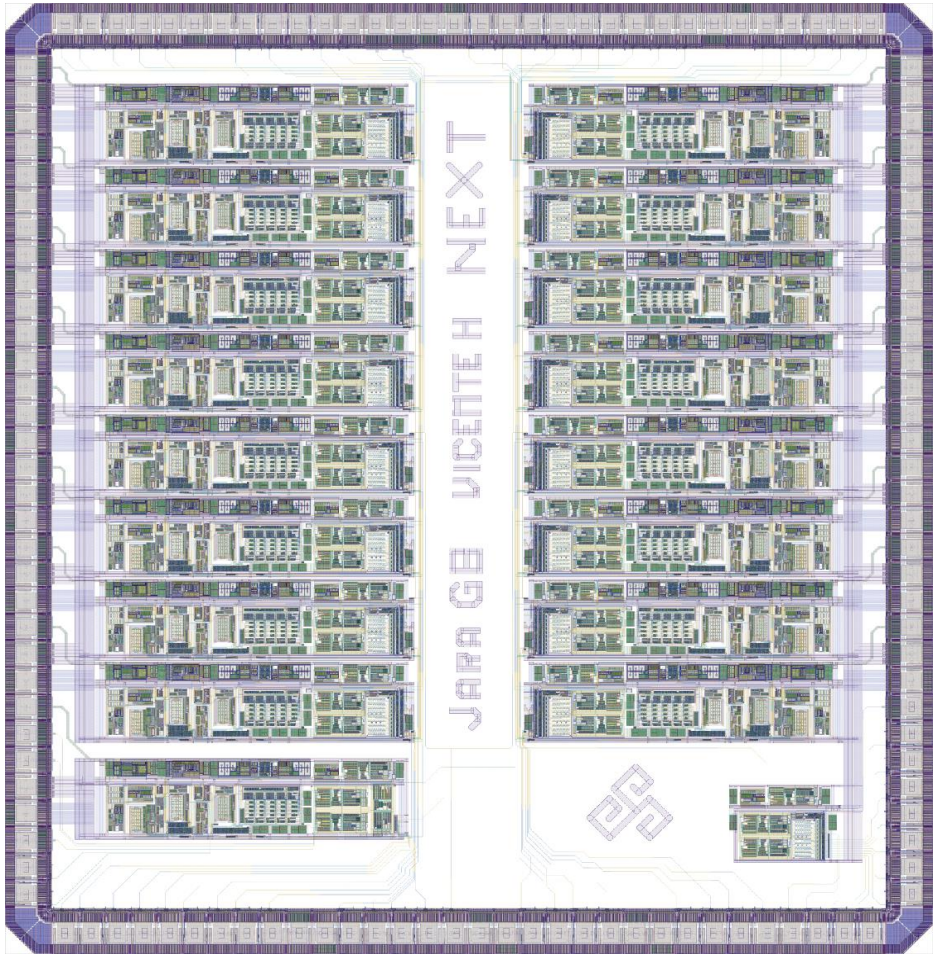
Slow Path

(Preamplifier + Integrator + ADC)

+

Fast Path

(Signal Optimization Processing)



* **Talk**, TRISK-J ASIC, this afternoon at 15:40h

25th IEEE Real Time Conference

Questions!

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This work was supported by the European Research Council (ERC) through a Synergy Grant under the EU Horizon 2020 (grant agreement No. 951281).