

25<sup>th</sup> IEEE Real Time Conference

# TRISK-J: a Novel Integrated Front-End with Edge Computing Capabilities for NEXT Experiment

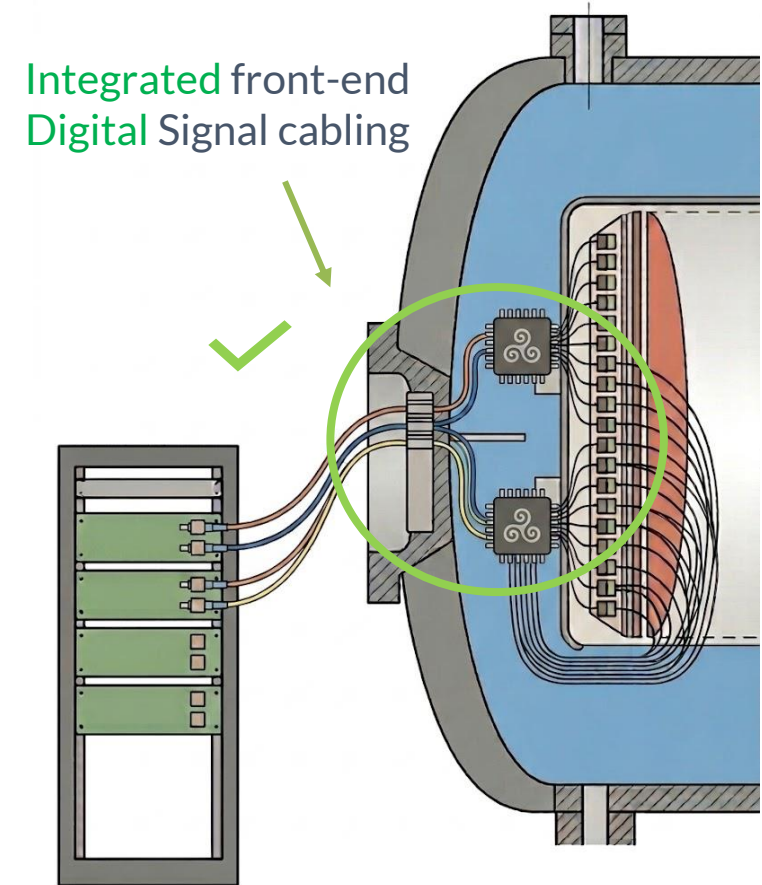
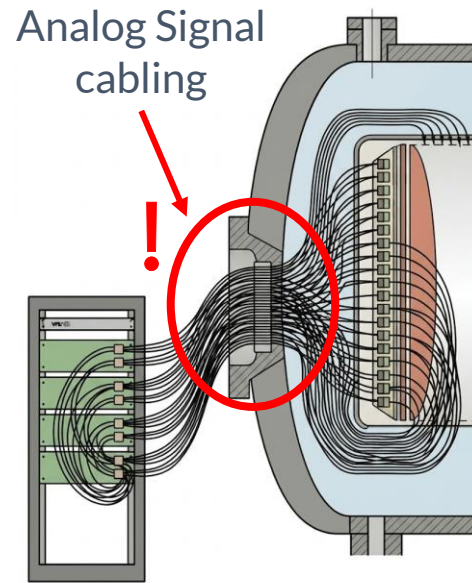
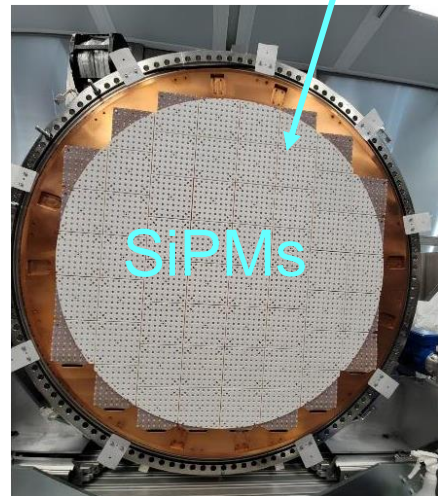
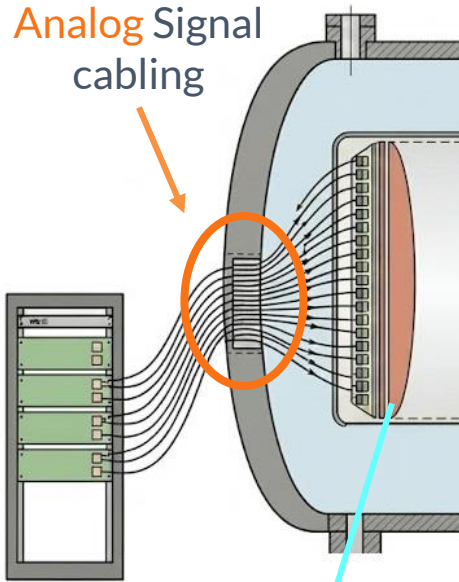
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J.J Gómez-Cadenas

Universitat Politècnica de València (UPV)

May 26<sup>th</sup>, 2026

# TPCs Evolution

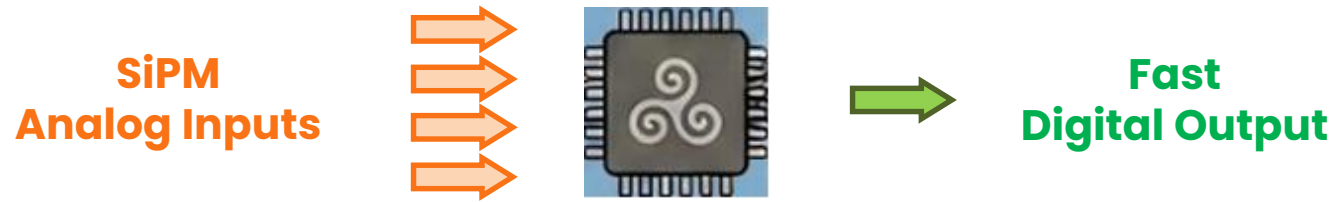


- Signal distortion (Crosstalk)
- Feedthrough Complexity
- High Density Plane
- High Dark Count Rate

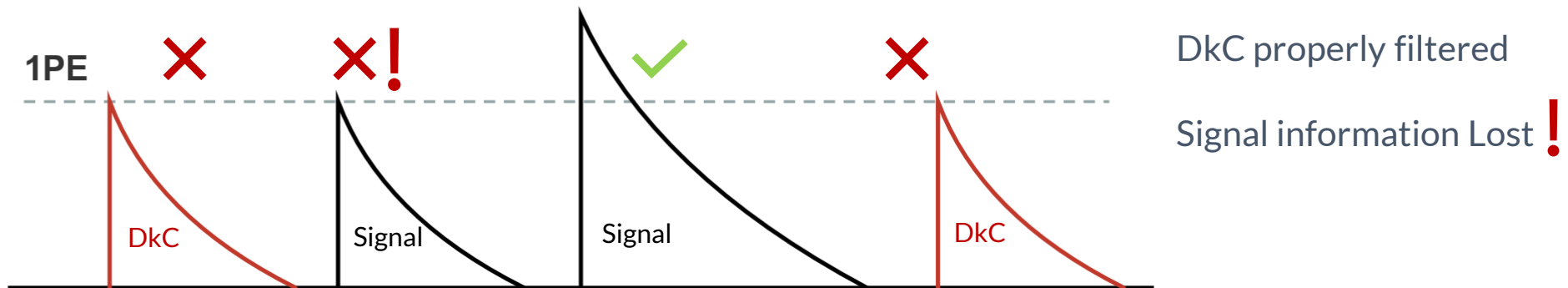
# NEEDS



- Channel Management Solution → **ASIC**



- Standard ASIC Solution → **Slow Path** (Preamplifier + Integrator + ADC)
- Standard DkC Solution → **Pe Threshold**

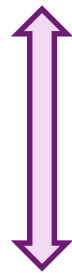


# TRISK-J: ARCHITECTURE



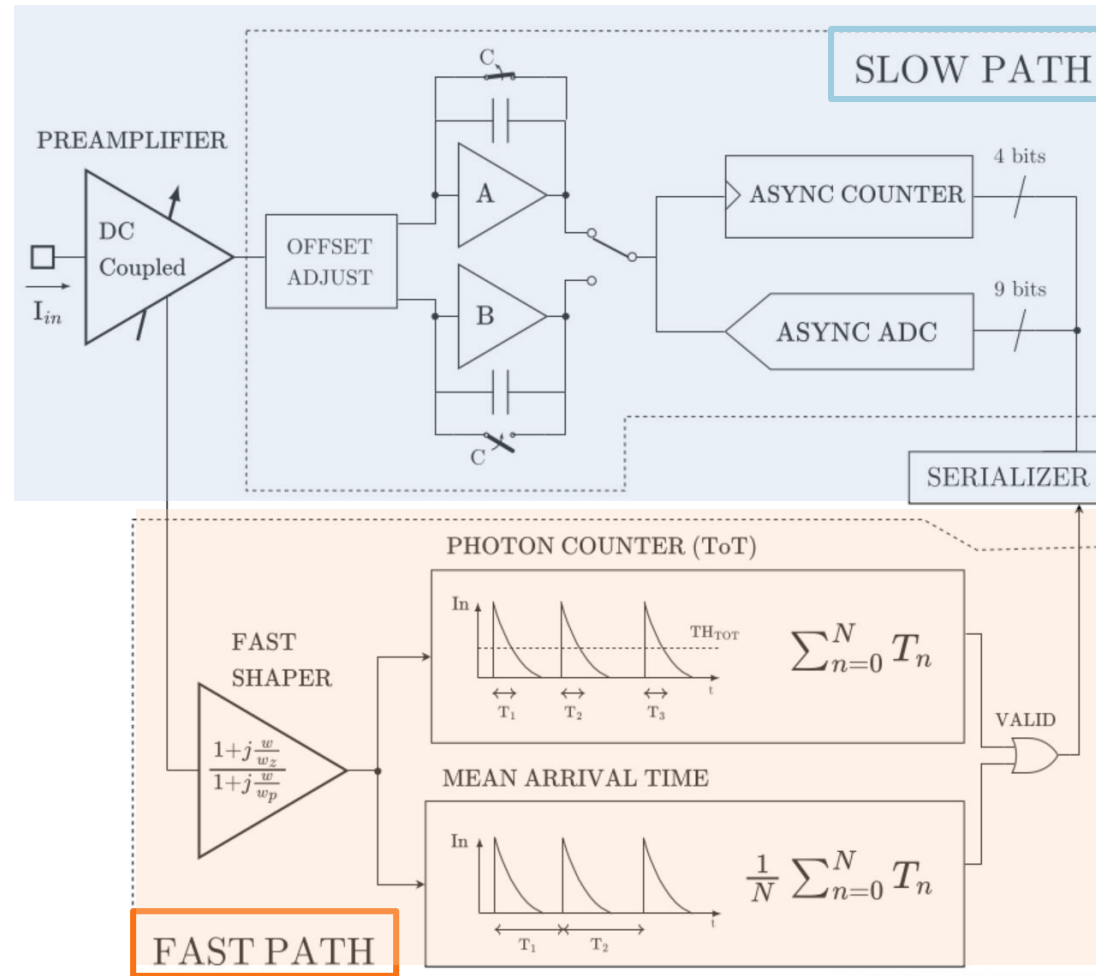
Threshold signal **R**ecovery and **I**mprovement for **S**tatistical **d**ark **K** count rejection

- **Slow Path**  
(Preamplifier + Integrator + ADC)



Working in parallel

- **Fast Path**  
Photon Counting Statistics



# PREAMPLIFIER: DESIGN SPECS



- Arbitrary Signal Shape

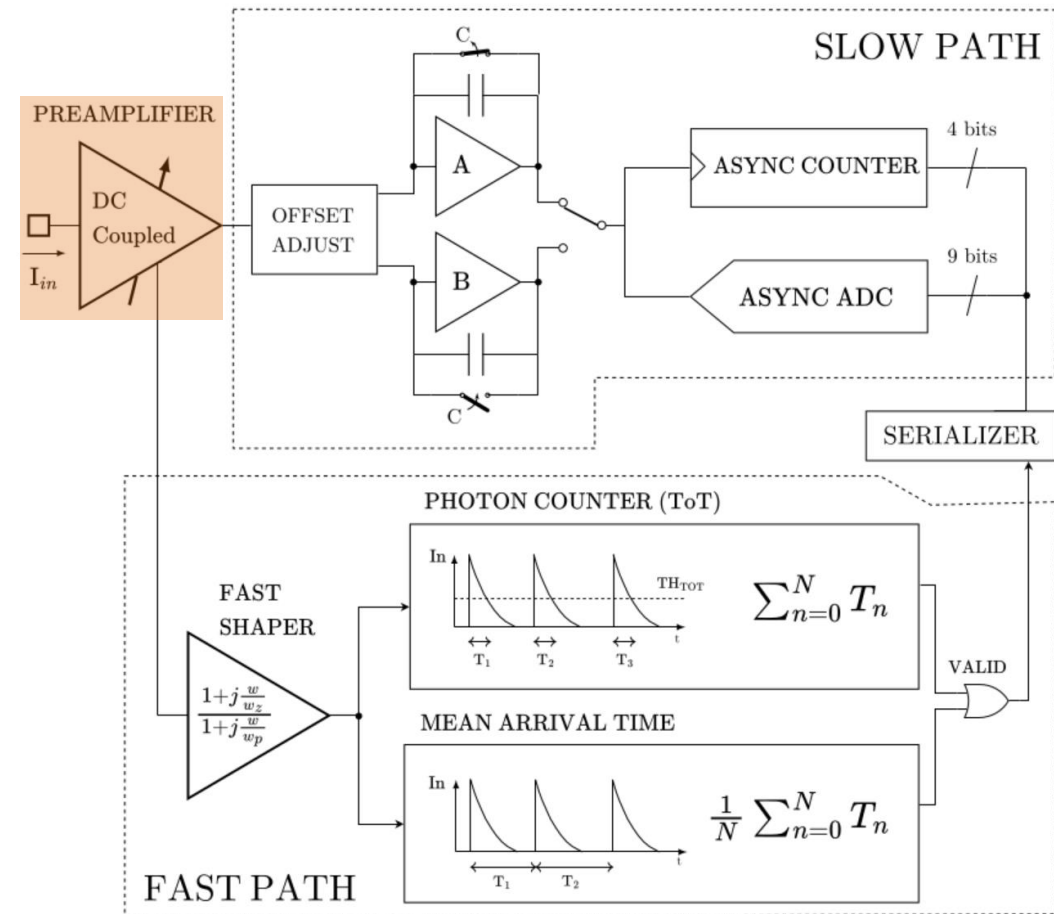
DC coupled scheme

- Several Sensor Options

Configurable to work under a wide range of SiPM

- Fine readout specs

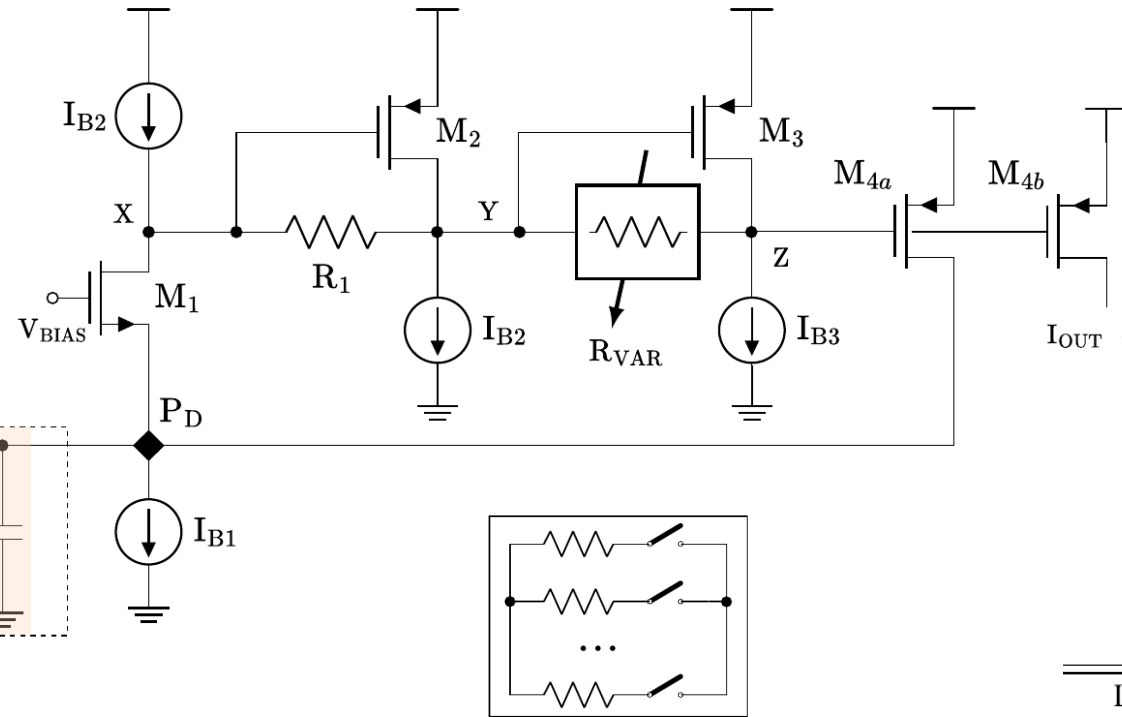
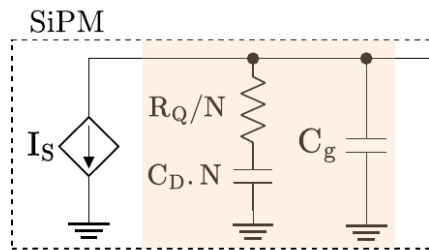
Low noise & Distortion under all usage conditions



# PREAMPLIFIER



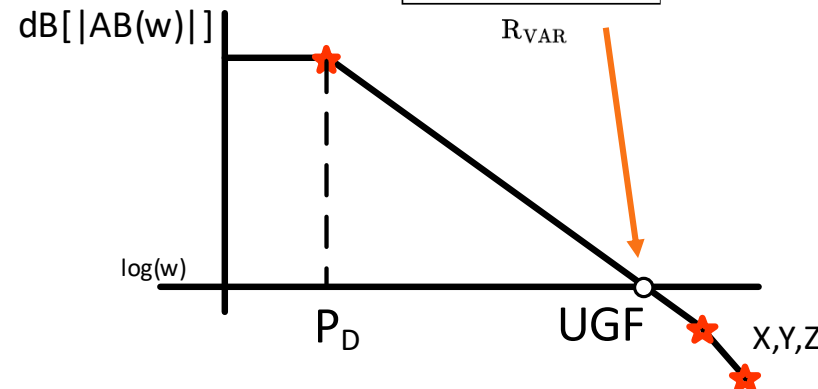
Equivalent  
Capacitance for  
external dominant  
pole



DC Coupled  
OFFSET  
correction  
required

$$\omega_{PD} \approx \frac{g_{m1}}{(N \cdot C_D + C_g)}$$

$$A\beta_{DC} = g_{m4a} R_1 R_{VAR} \frac{g_{m2} g_{m3}}{g_{m2} + g_{m3}}$$



Specification	150 pF	600 pF	2.4 nF
Loop Gain (dB)	28.4	28.4	42.3
PM	59.1°	73.49°	62.2°
Linearity (%)	0.98	0.63	0.52
Max. Current (mA)	2	2	2
Output Noise (pA/√Hz)	6.6	13.8	38.5
Power consumption	2.5 mW		

# INTEGRATOR: DESIGN SPECS



- Low data rate generation + Accurate charge measurement

## GATED integrator scheme

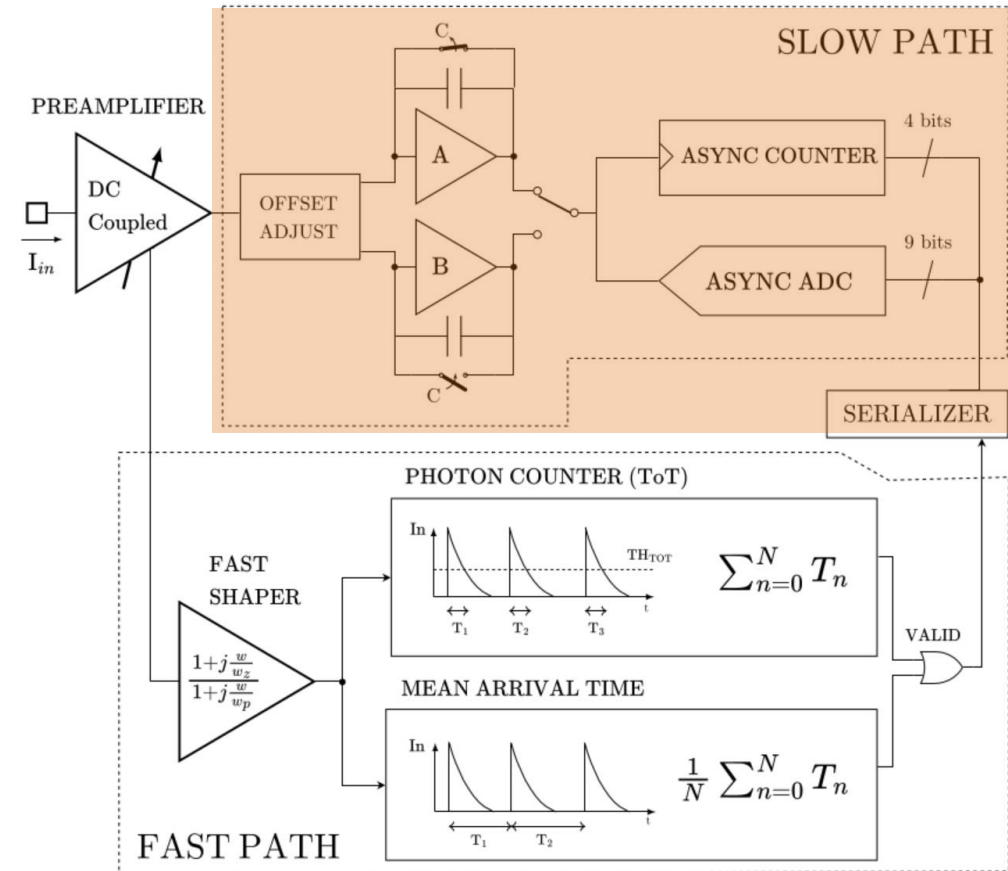
- Extended Dynamic Range

Over 600 PE per integration window

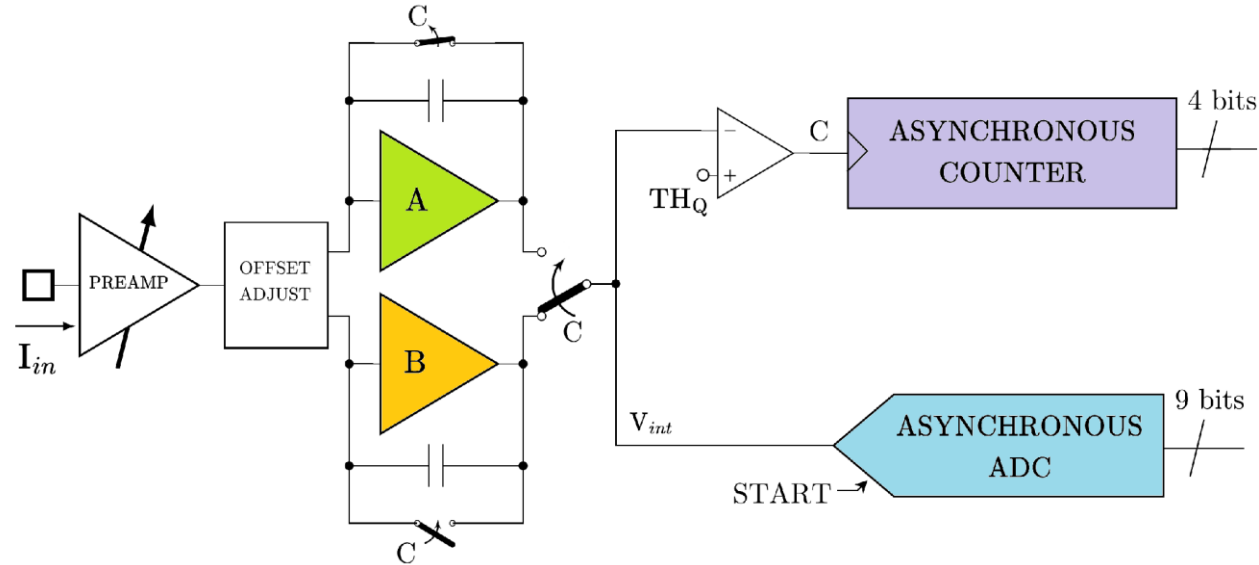
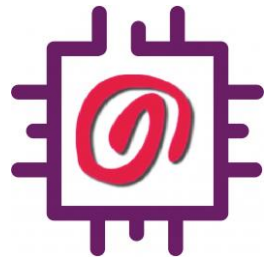
Good PE resolution for PE spectrum based calibration

- Good Linearity

Under different signal types and conditions



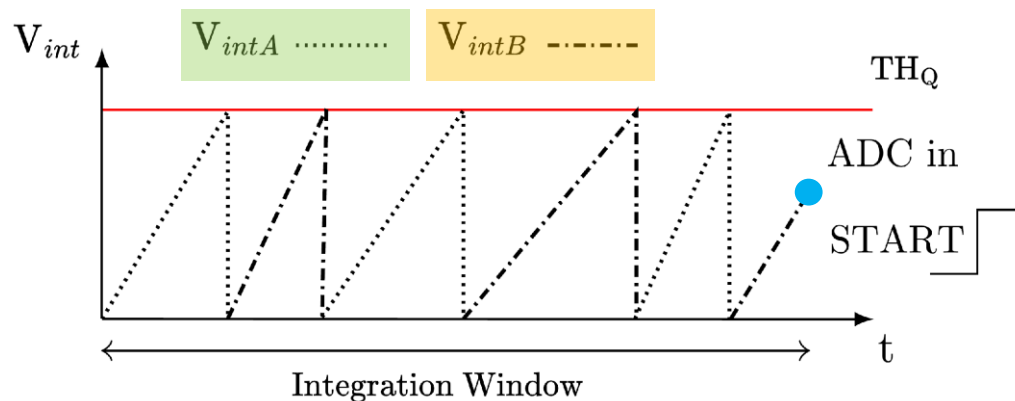
# INTEGRATOR: PING – PONG SCHEME



Incremented with each handover operation

TH<sub>Q</sub> → Quantum of Charge

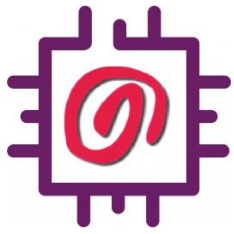
Final residue ADC conversion



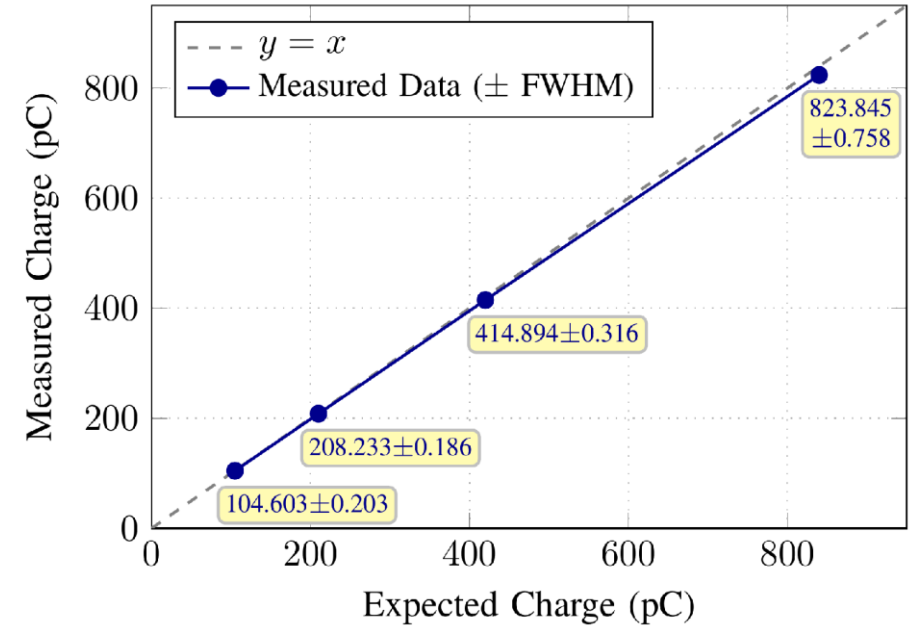
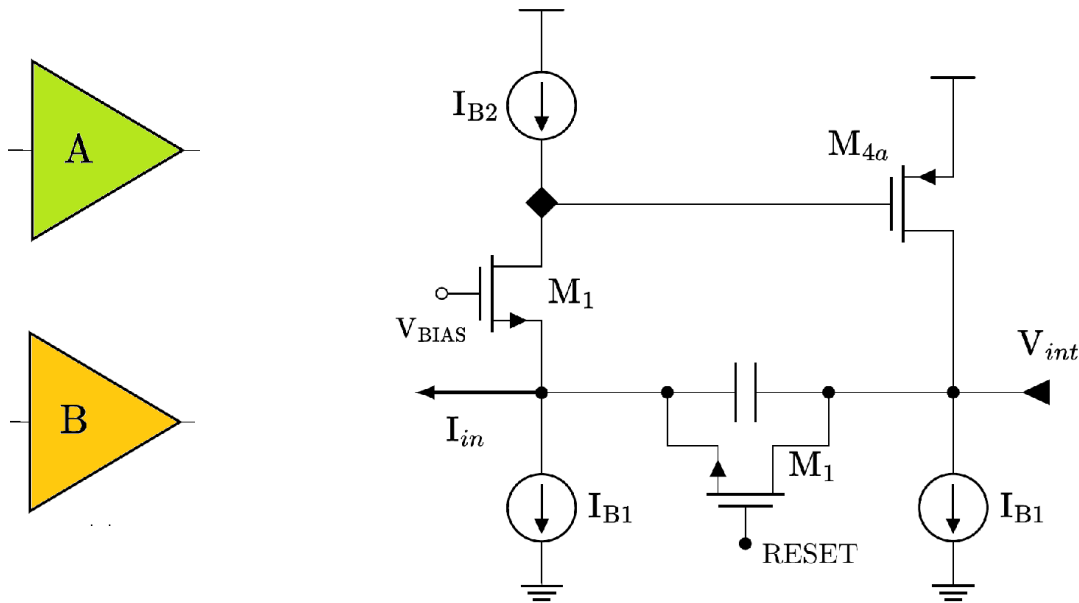
12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	1	0	0	1	1	1	0

**RESET time required for PING integrator is covered by PONG (and viceversa)**

# INTEGRATOR: Results



## PING-PONG integrators implementation



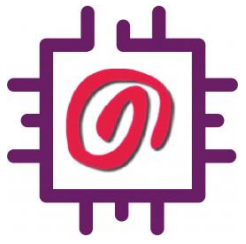
### INTEGRATOR SPECIFICATIONS

Specification	Value
GAIN (mV/pC)	161.8
Resolution (FWHM)	0.2 %
Linearity error	0.98 %
Power consumption	2.2 mW

RESET introduces a momentary OPEN LOOP condition when released

LOW input impedance required to reduce transitory at the start of integration

# Analog to Digital Converter



## DESIGN SPECS

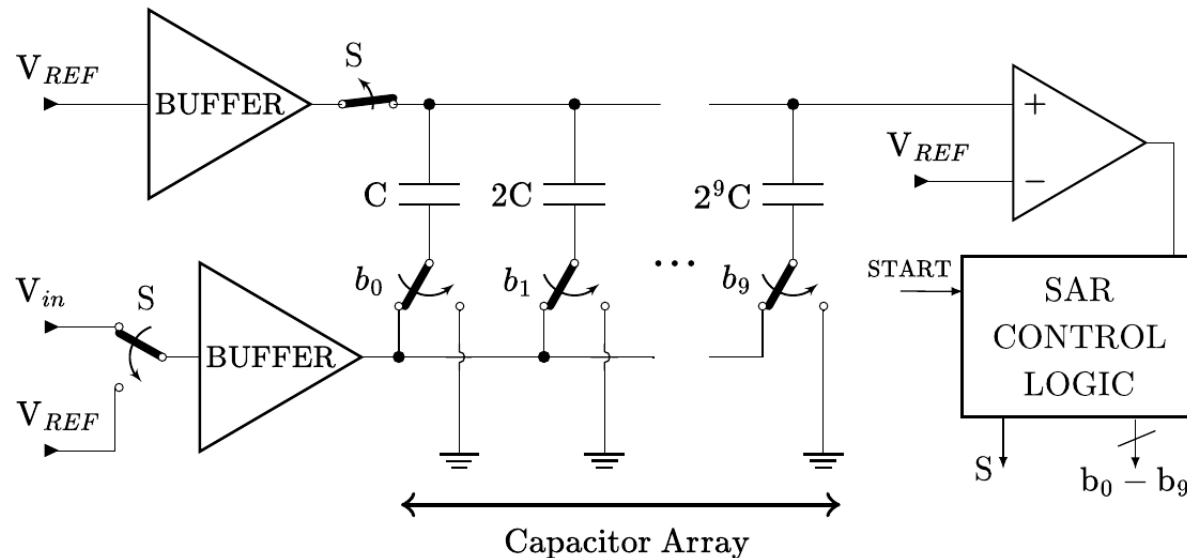
High density channel integration

High Speed

Asynchronous Control

Capacitive Successive Approximation (SAR)

Sampling included

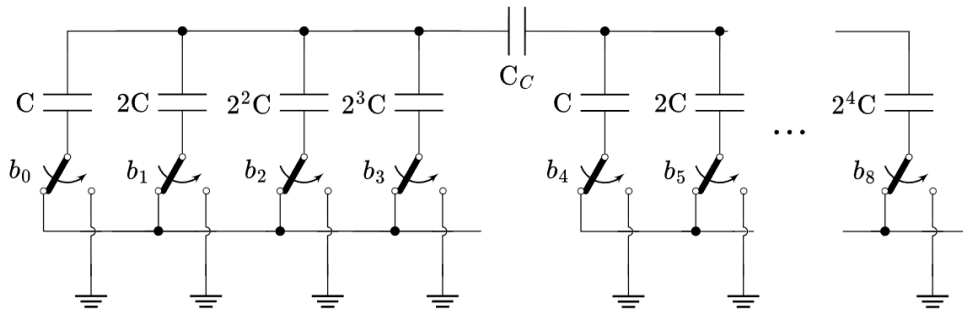


# Analog to Digital Converter



## OPERATION & DETAILS

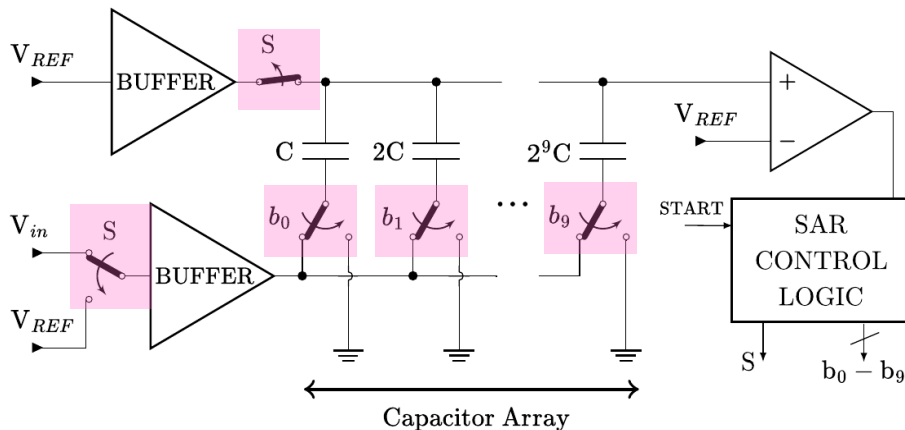
### SPLIT CAPACITOR SUBDACs



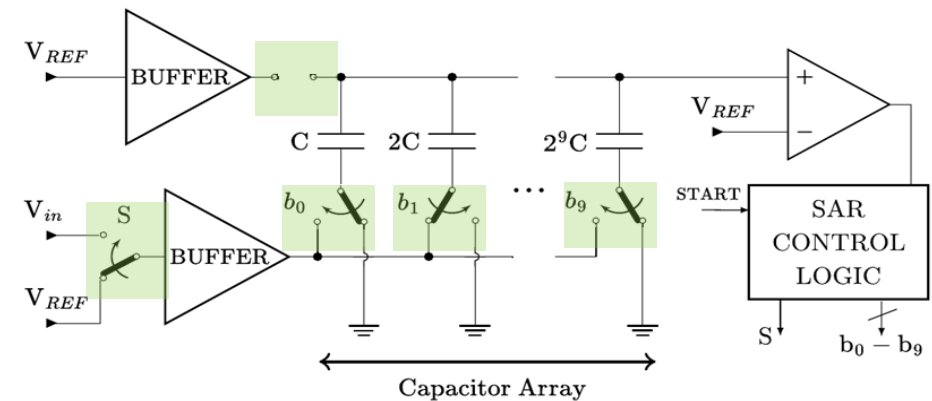
### ASYNCHRONOUS ADC SPECIFICATIONS

Specification	Value
ENOB	9
Minimum conversion time	250 ns
Power consumption	3.2 mW

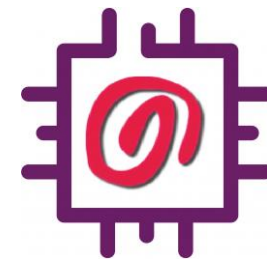
### SAMPLE: Capacitor Array $V_{IN} - V_{REF}$



**BINARY SEARCH:** 
$$V_+ = \left( \sum_n b_n \cdot \frac{1}{2^n} + 1 \right) \cdot V_{REF} - V_{in}$$



# FAST PATH\* – Edge Analog Computing

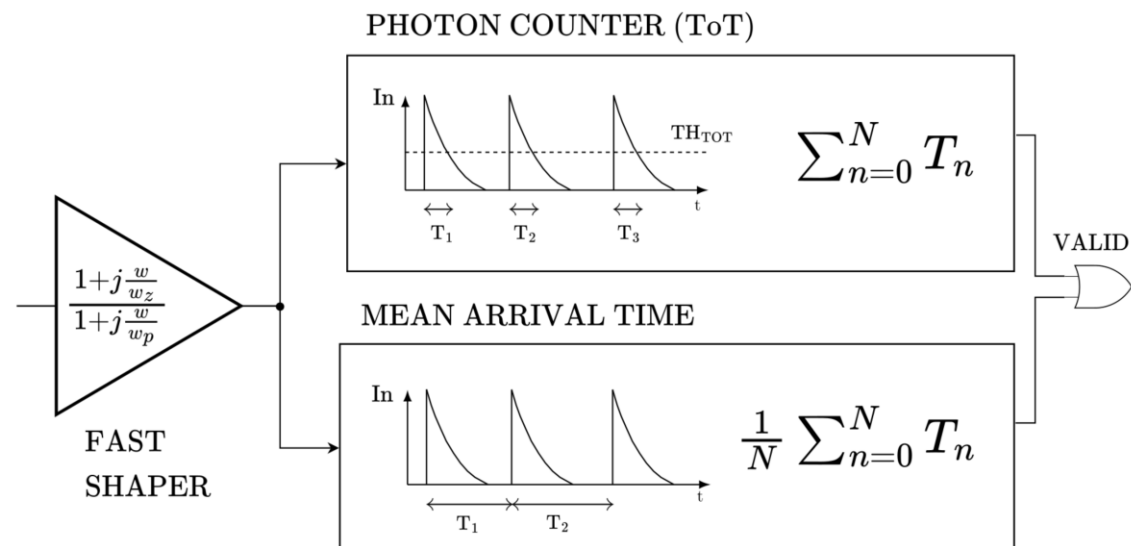


Statistical estimator

Dark Count Rejection

Fully-analog  
Implementation

Signal recovery

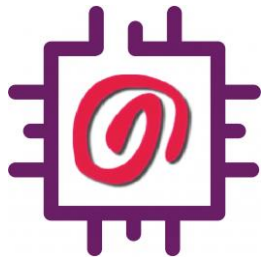


Pile-up effects overcome

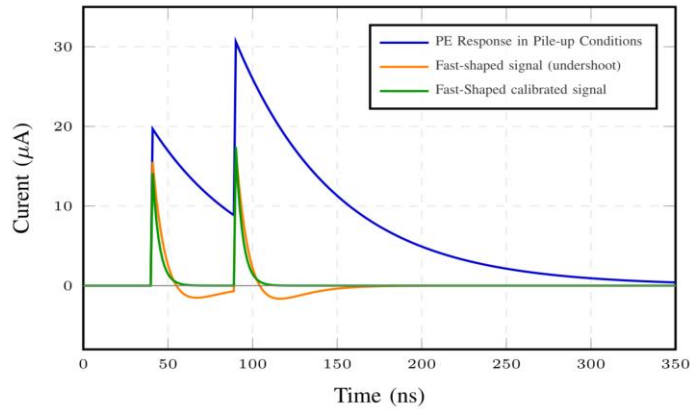
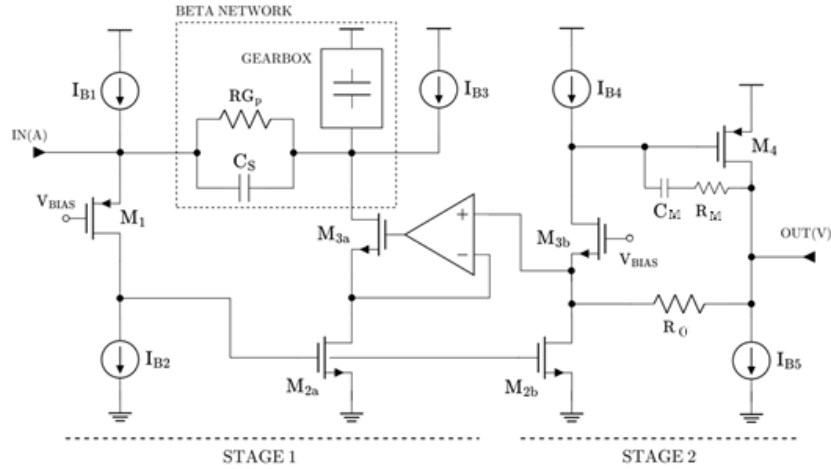
Low Power Consumption

\* Early Statistical Estimation for Data Rate Optimization in Dark-Count-Limited Detector Using Fully-Analog Processing, this morning at 9:30h

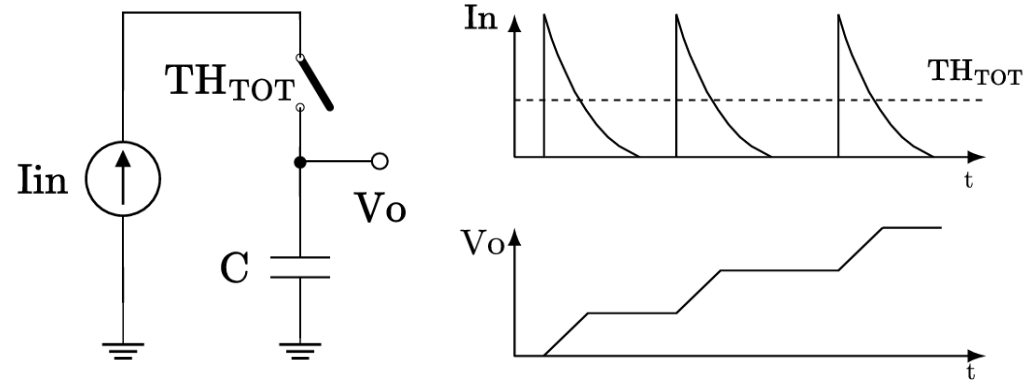
# FAST PATH - Summary



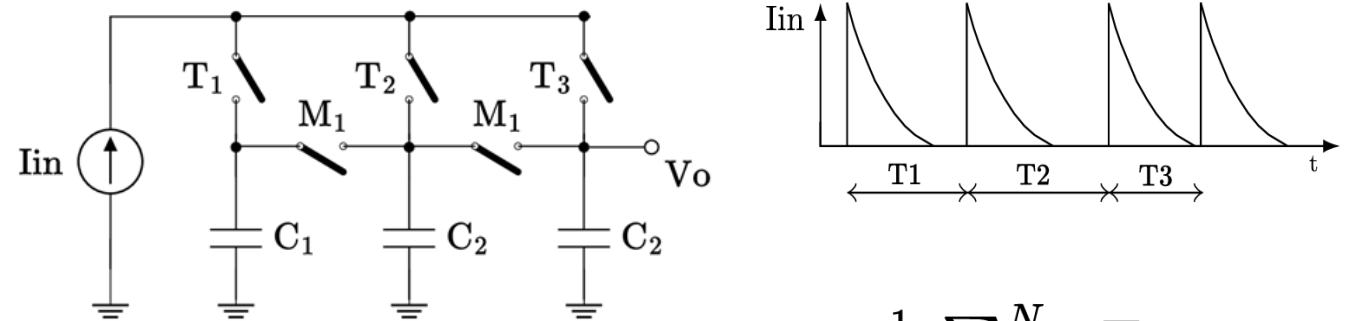
## Fast Shaper



## ToT based Photon Counter



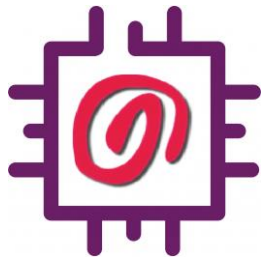
## Mean arrival time measure



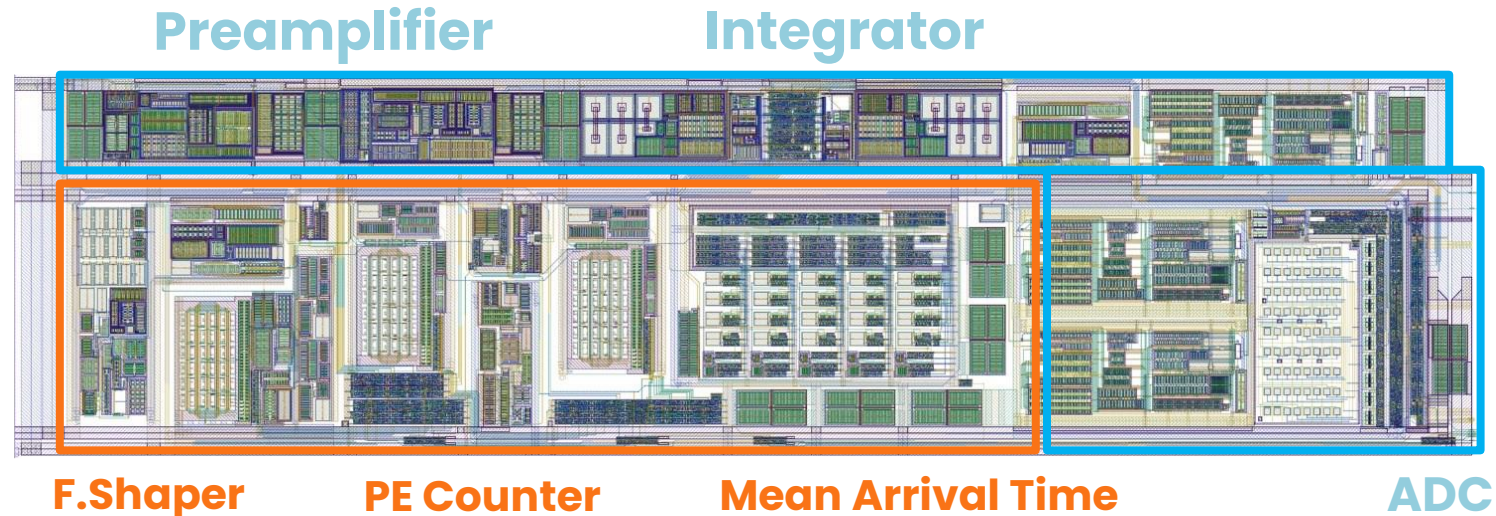
$$\frac{1}{N} \sum_{n=0}^N T_n$$

\* Early Statistical Estimation for Data Rate Optimization in Dark-Count-Limited Detector Using Fully-Analog Processing, this morning at 9:30h

# ASIC: TRISK-J



Threshold signal **R**ecovery and **I**mprovement for **S**tatistical dar**K** count rejection



**Slow Path**

(Preamplifier + Integrator + ADC)

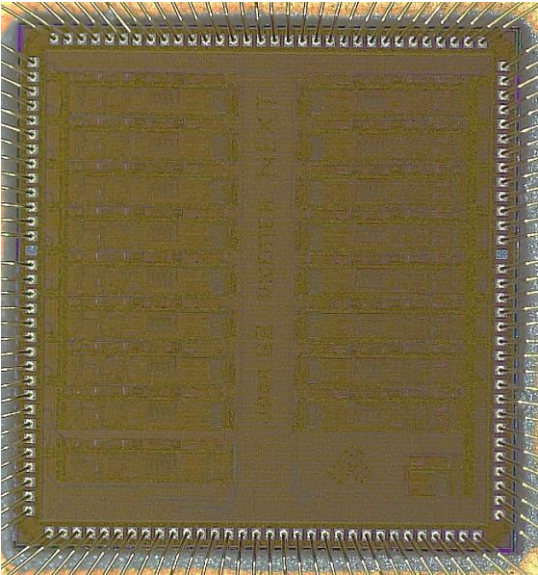
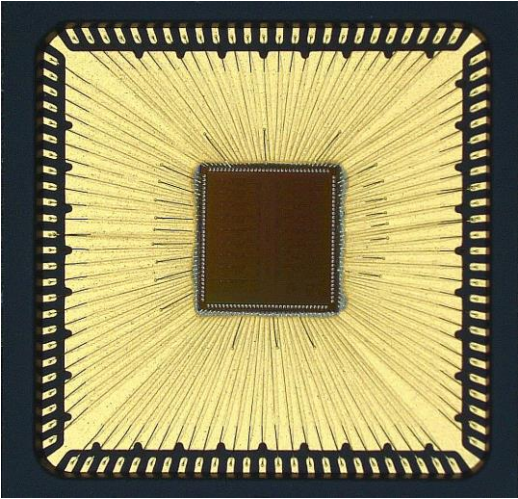
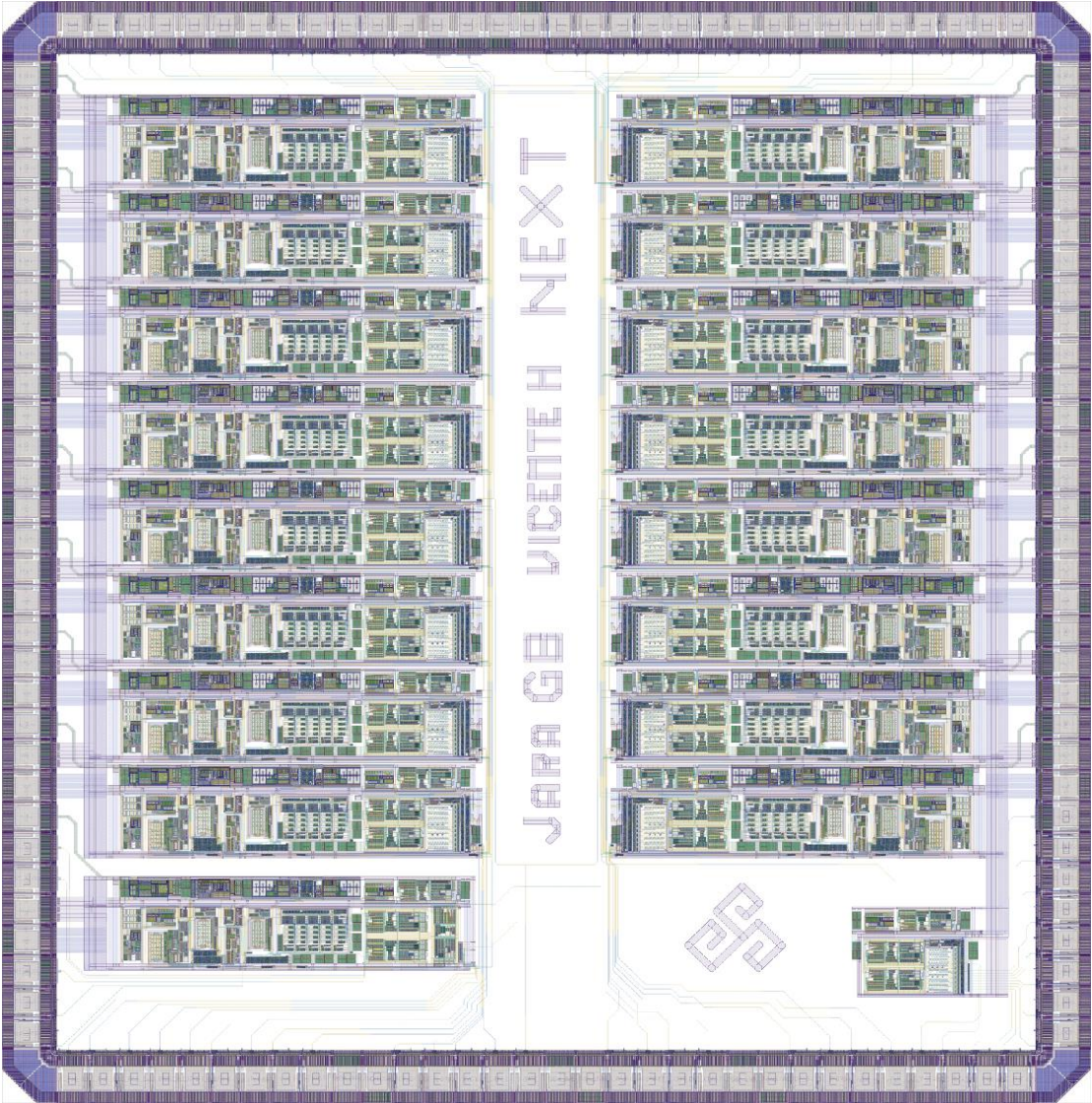
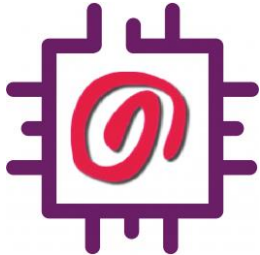


**Fast Path**

(Signal Optimization Processing)

# TRISK-J

Threshold signal Recovery and Improvement for Statistical dark count rejection



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# Questions!

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