

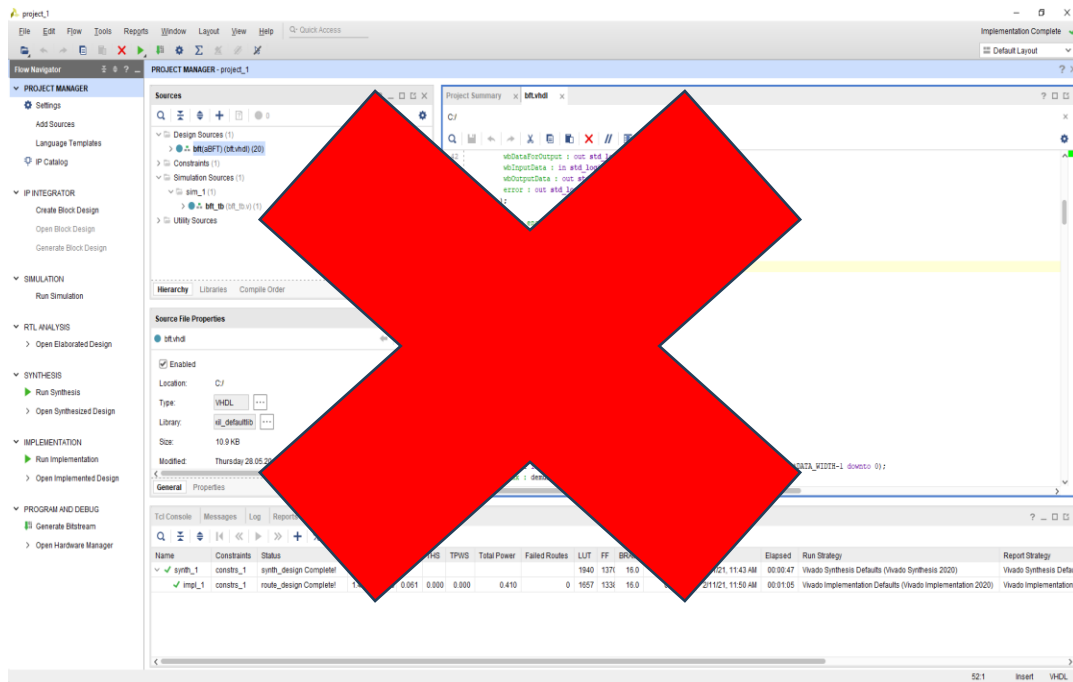


A. Abba  
F. Caponio  
S. Carsi  
D. Bianchi  
V. Arosio  
M. Petruzzo  
C. Tintori  
L. Colombini  
M. Bianchini  
V. Bottiglieri  
Y. Venturini  
A. Cusimano

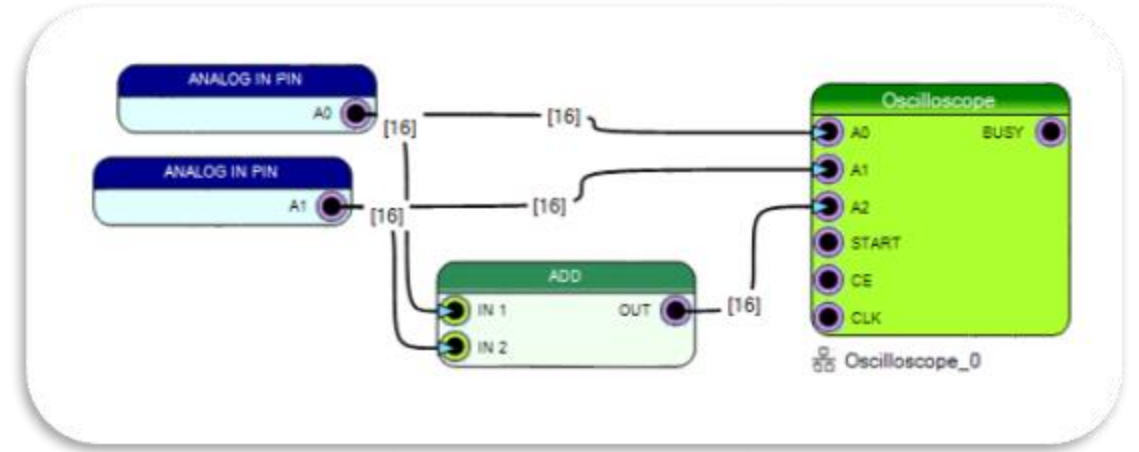
designed for CAEN digital acquisition systems

# From Concept to Creation: SciCompiler Brings Your Ideas to Life

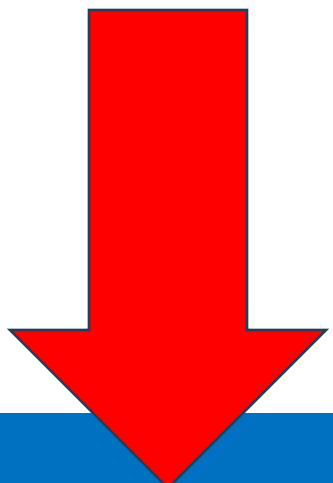
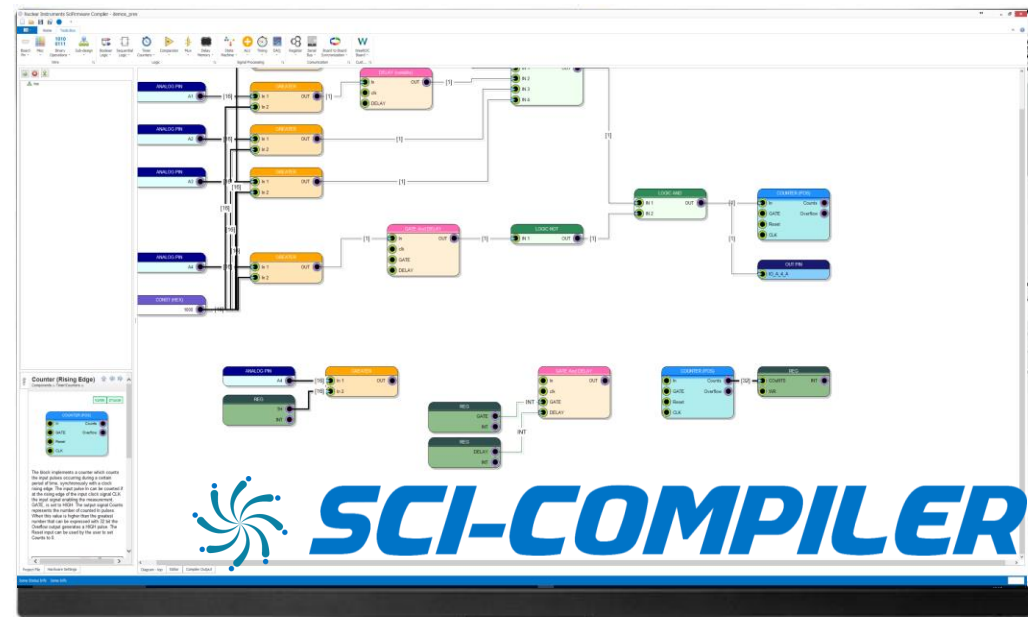
Design as easily as sketching your ideas – no need to learn complex languages like VHDL or Verilog; SciCompiler takes care of it for you.



Develop with block diagram



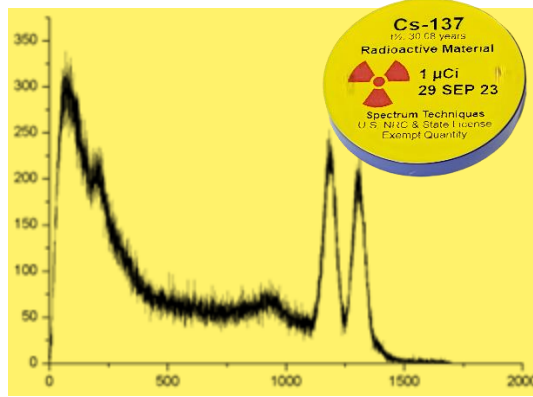
# NI/CAEN Solution: OpenFPGA digitizers + SciCompiler firmware generator



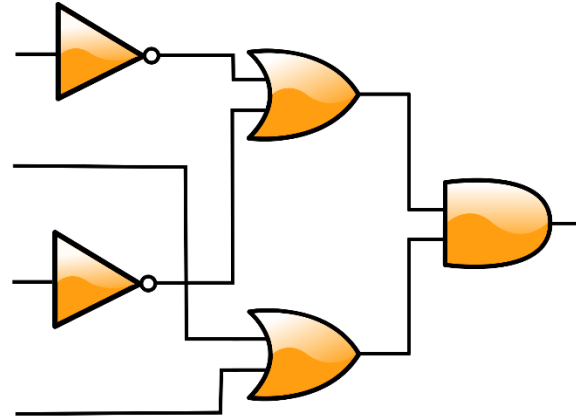
**DAQ 121 / DAQ 122**  
12/14 bit – 1 Gbps  
32 channels



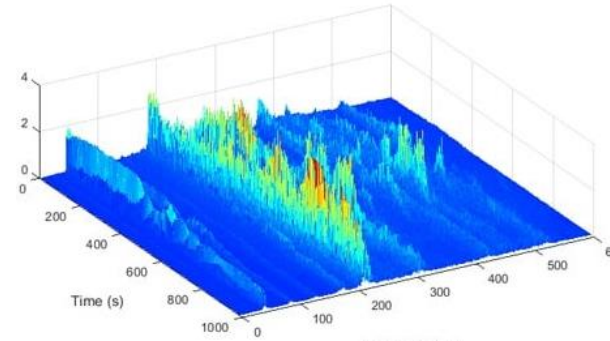
# Examples of what you can do with Sci-Compiler



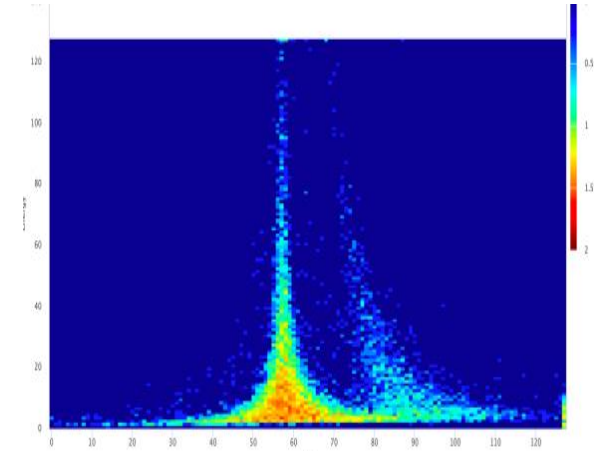
PHA



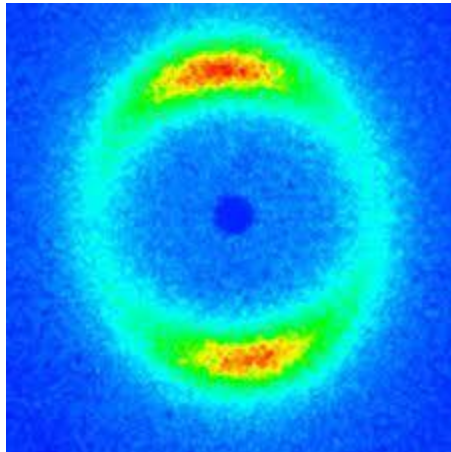
COMPLEX TRIGGER LOGIC



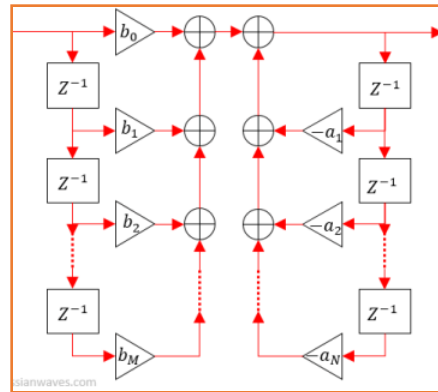
REALTIME FFT



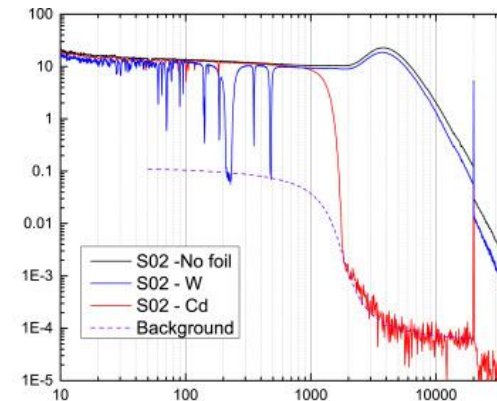
PSD



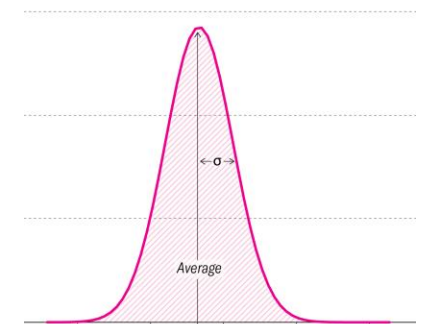
NEUTRON IMAGING



REALTIME IIR-FIR FILTER



SUB-ns TOF TDC



REALTIME STATISTICS

# Open-FPGA Board architecture

Primary function of a firmware:



Control the board acquisition process

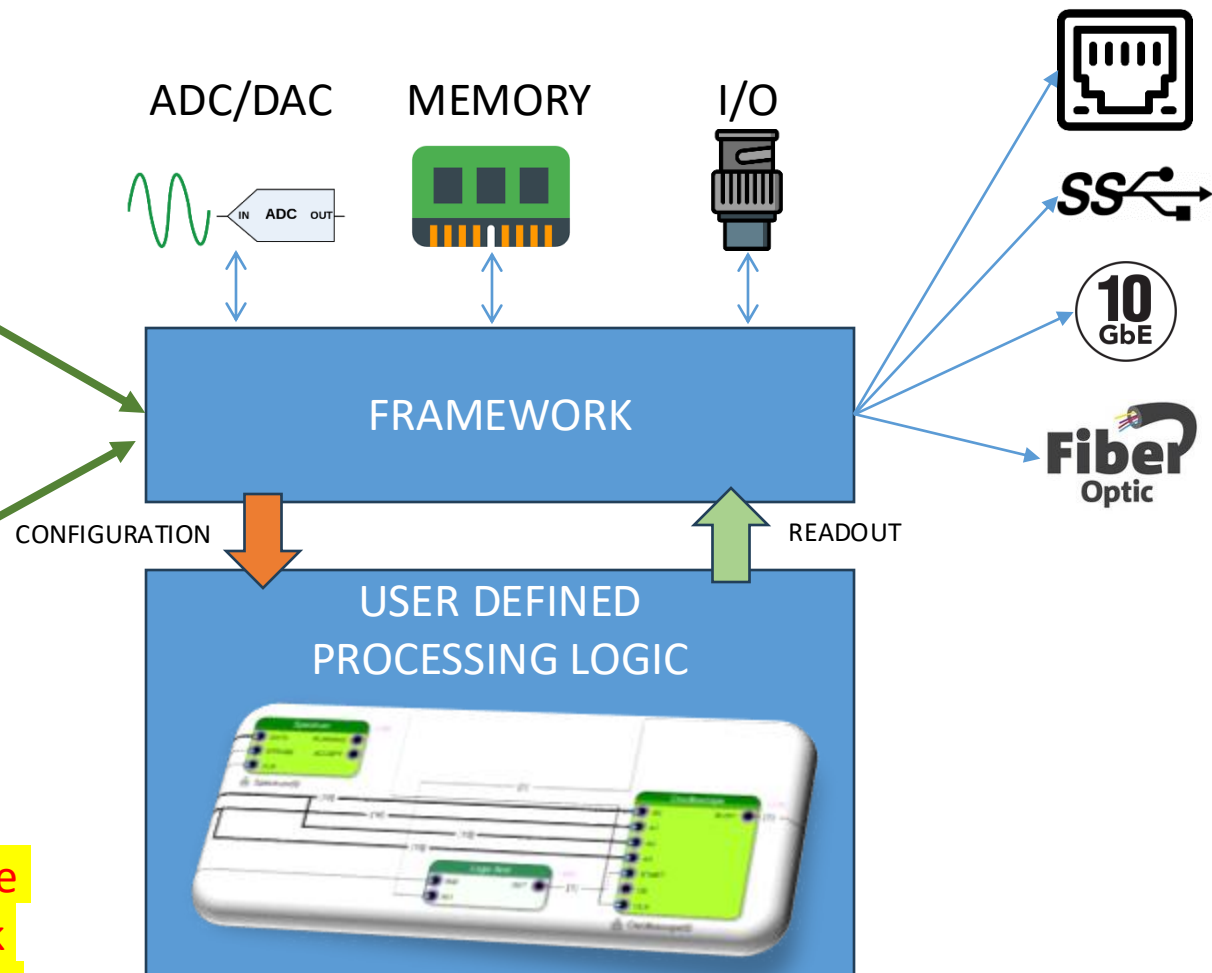


Processing data

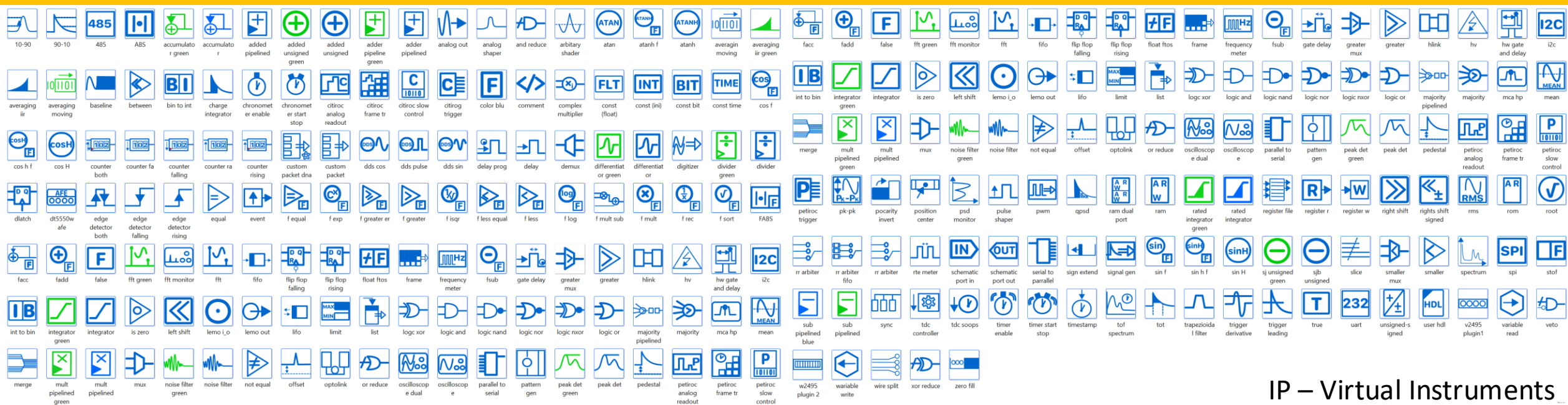


Transfer data to and from readout  
PC/Server

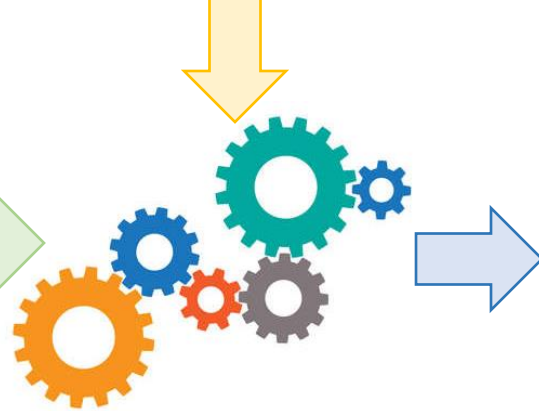
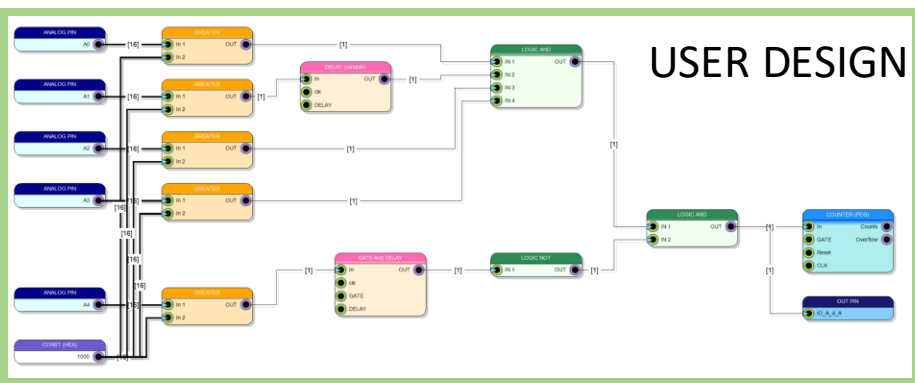
Sci-Compiler lets the developer think only about the core algorithm — everything else, from framework to readout, is handled automatically with high-level abstraction blocks.



# SciCompiler: ip integrator software



IP – Virtual Instruments



BUILDER ENGINE

```

18 architecture Counter_Arch of AAC2M2P1 is begin
19
20   count_proc : process(CP,SR,PE,CEP,CET) begin
21
22     if (SR='0') then Q <= "0000";
23
24     elsif rising_edge(CP) then
25
26       if PE = '0' then Q <= P; --Load
27
28       elsif CET = '1' and CEP = '1' then Q <= Q+1; -- count
29
30       end if;
31
32       if CET = '1' and Q = "1111" then TC <= '1'; -- Terminal count
33
34       else TC <= '0';
35
36       end if;
37
38       end if;
39
40     end process count_proc;
41
  
```

```

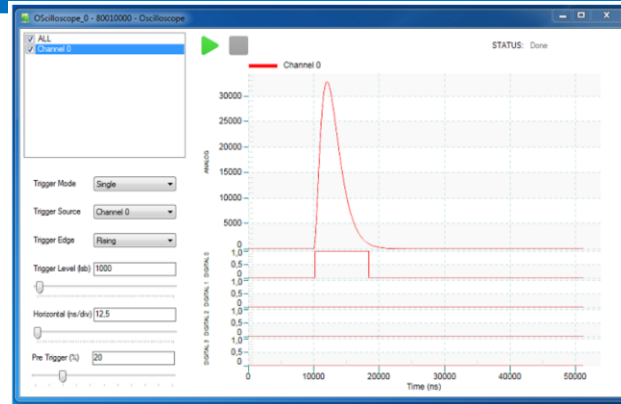
0001 0001 0000 0011 0000 0101 0101 0110 0111
1000 0000 0000 0011 0000 0101 0101 0101 0101
0110 0111 1000 0001 0001 0000 0011 0100 0100
0101 0110 0111 0000 0000 0000 0000 0100 0101
0110 0111 0110 0000 0000 0011 0000 0101 0101
0100 0101 0000 0111 0000 0000 0000 0111 0000
0000 0000 0000 0000 0001 0001 0001 0010 0111
0111 0100 0101 0110 0111 1000 0001 0001 0100
0111 0100 0101 0110 0111 0000 0000 0000 0111
0111 0011 0100 0101 0110 0111 0000 0000 0000
0111 0000 0111 0011
0110 0111 0000 0000
0101 0101 0110 0101
0000 0110 0111
  
```



# Sci-Compiler generate for you firmware and software

```
40 architecture Behavioral of SERIAL_TO_PARALLEL_FIXED is
49   SERIAL_OUT(0) <= IDATA(0);
50
51   deserializer_process: process(CLK,RESET)
52   begin
53     if RESET(0) = '1' then
54       IDATA <= (others => '0');
55       LDATA <= (others => '0');
56     else
57       if rising_edge(CLK(0)) then
58         if CE(0) = '1' then
59           IDATA(buswidth-1) <= SERIAL_IN(0);
60           for I in 1 to buswidth-1 loop
61             IDATA(I-1) <= IDATA(I);
62           end loop;
63         end if;
64
65         if STREAM_START(0) = '1' then
66           counter <= buswidth;
67           PARALLEL_DV <= "0";
68           running <= '1';
69         else
70           if running = '1' then
71             if counter = 0 then
72               PARALLEL_DV <= "1";
73               running <= '0';
74               if MSBFirst = "0" then
75                 LDATA <= IDATA;
76             else
```

FIRMWARE



READOUT UI

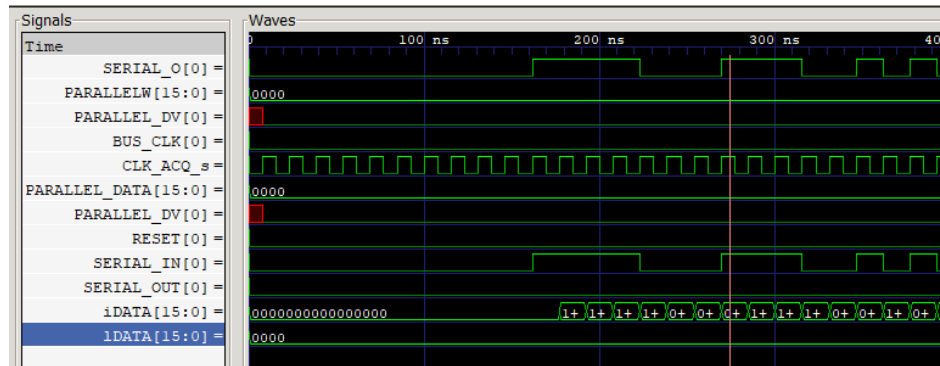


SIMULATE

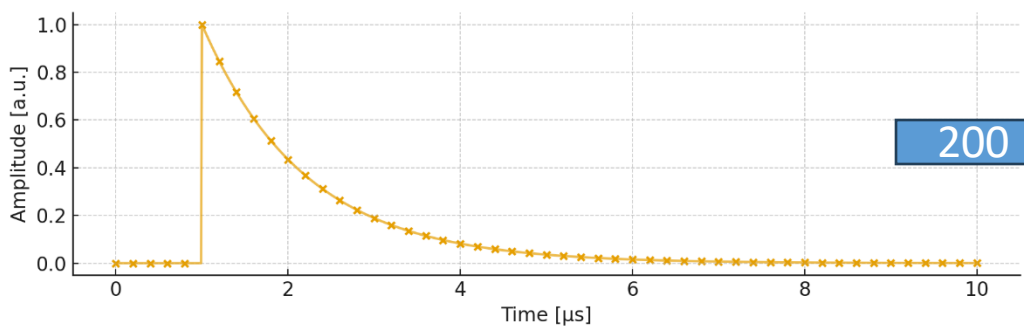
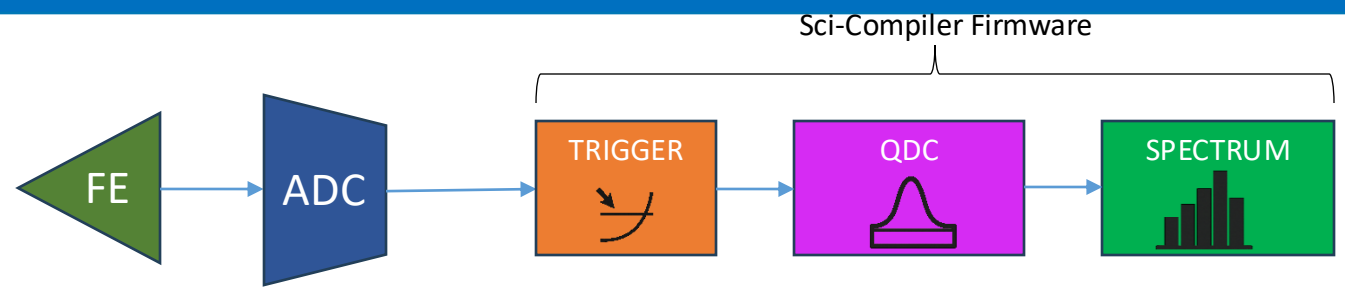
```
13 int main()
14 {
15     SCISDK_OSCILLOSCOPE *osc_data;
16
17     sdk.AddNewDevice("usb:0006", "dtl");
18     sdk.StrobeRegister("Registers/res", "p");
19
20     sdk.SetParameter("Oscilloscope_0/decim", "10");
21     sdk.SetParameter("Oscilloscope_0/trigger", "ext");
22     sdk.SetParameter("Oscilloscope_0/acq_mode", "b");
23     sdk.SetParameter("Oscilloscope_0/data_processing", "decode");
24
25     sdk.ExecuteCommand("Oscilloscope_0", "start");
26
27     sdk.AllocateBuffer("Oscilloscope_0", "decoded_buffer", (void **) &osc_data);
28
29     for (int i = 0; i < 10; i++) {
30         sdk.ReadData("Oscilloscope_0", osc_data);
31         dump_to_file(osc_data);
32     }
33
34     return 0;
}
```



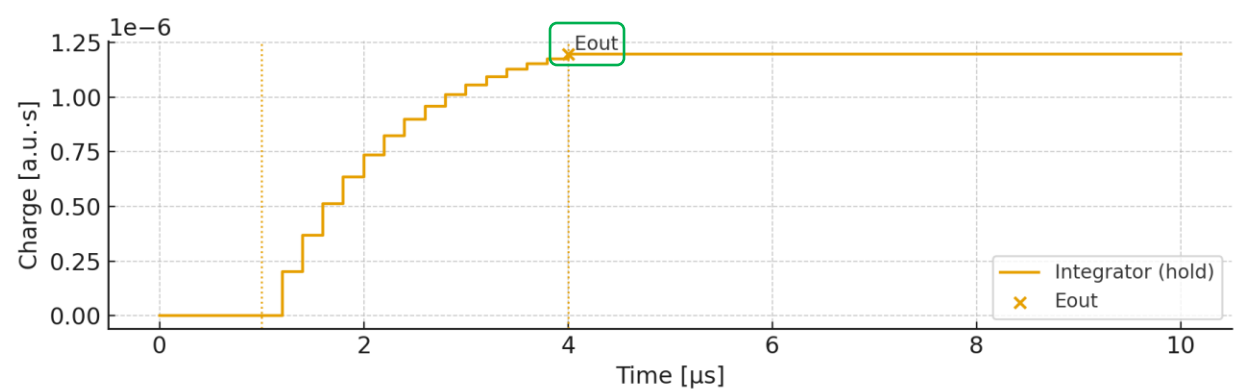
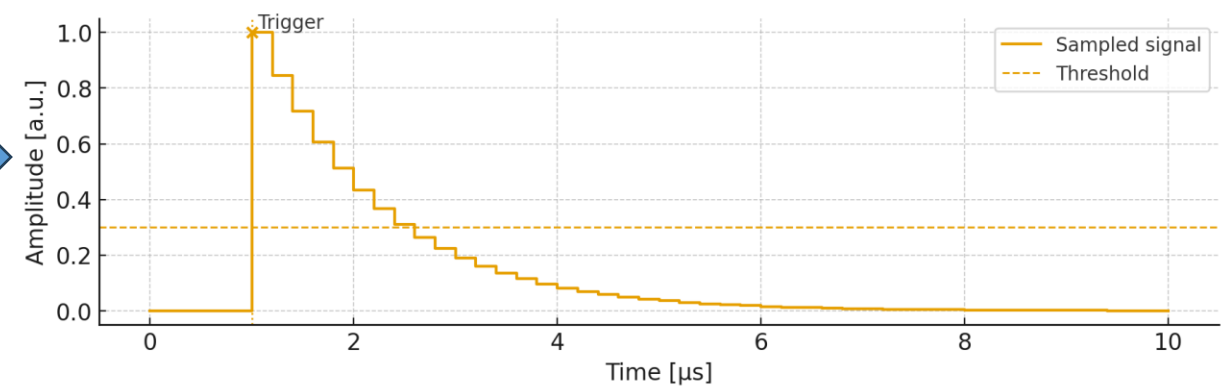
WINDOWS AND LINUX SDK



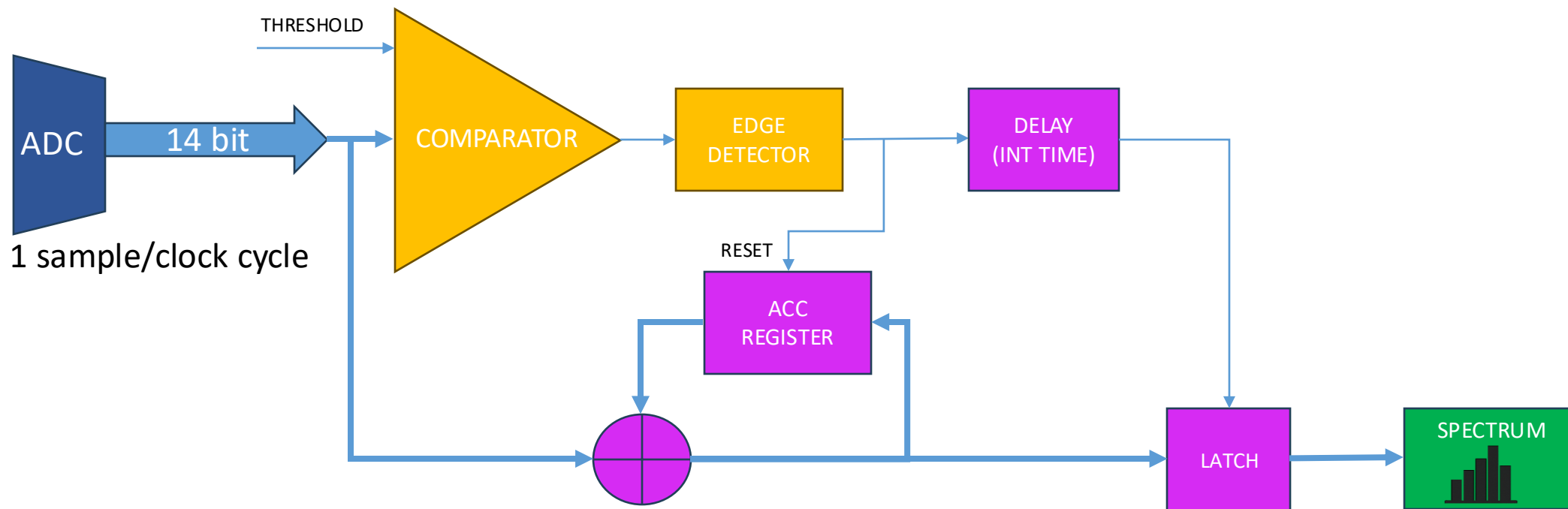
# High Speed Digitizer (up to 200 MSPS)



200 MspS



# High Speed Digitizer (up to 200 MSPS)

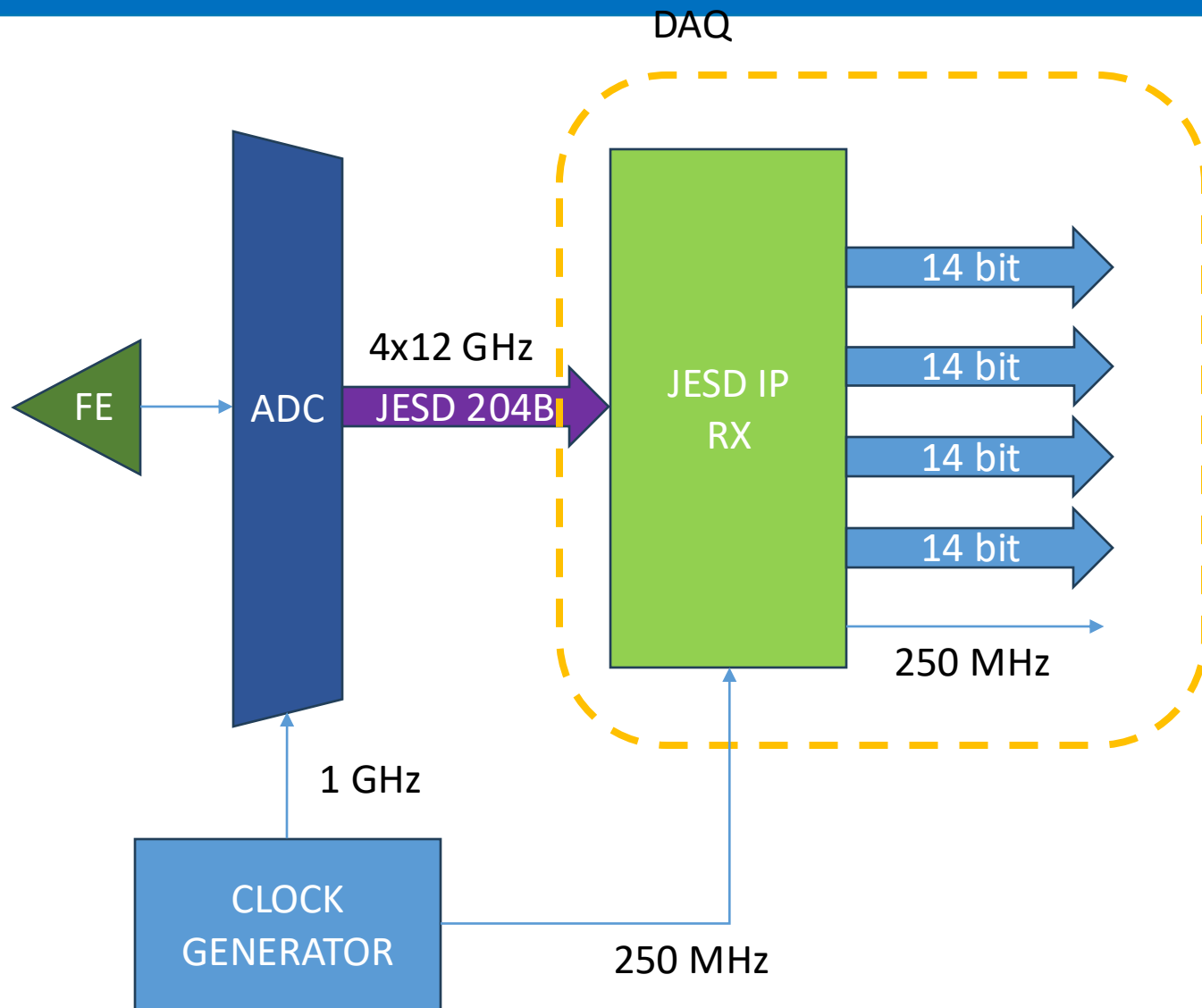
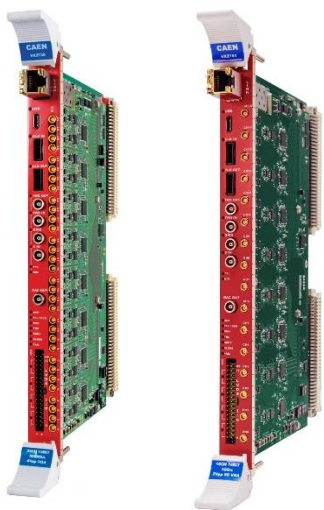


# Ultra-High Speed Digitizer

**Nuclear Instruments**  
**DAQ 121 - DAQ 141**  
**1 Gsps, 32 channel, 12/14 bit**

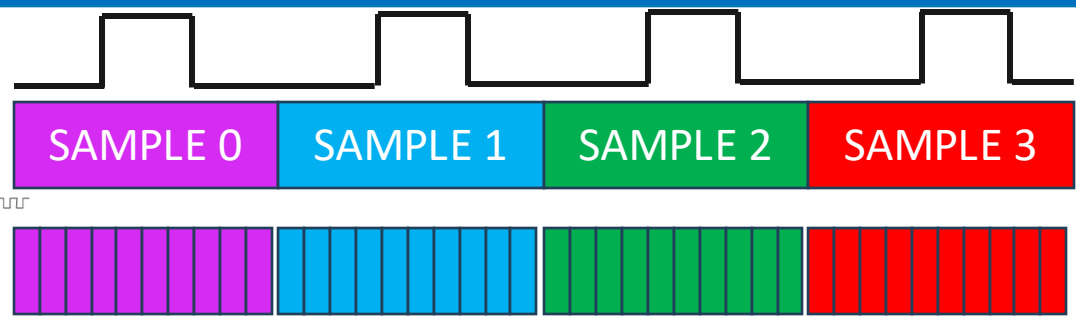


**CAEN V2730 - 500 Msps, 32 channel, 14 bit**  
**CAEN V2751 - 1 Gsps, 16 channel, 14 bit**

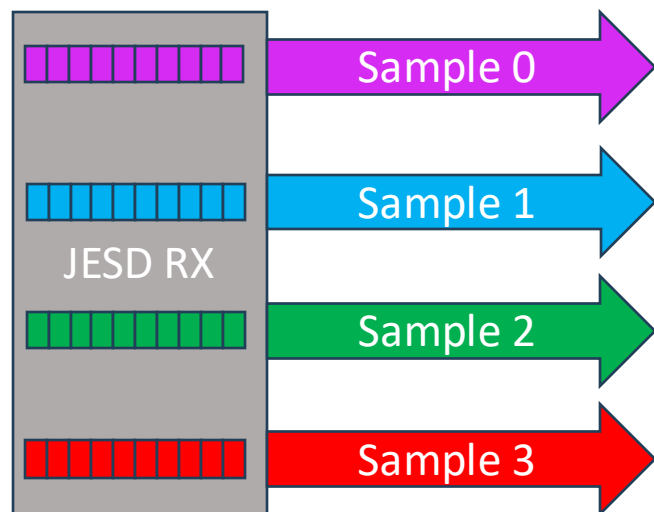


# Ultra-High Speed Digitizer: Parallel data decoding

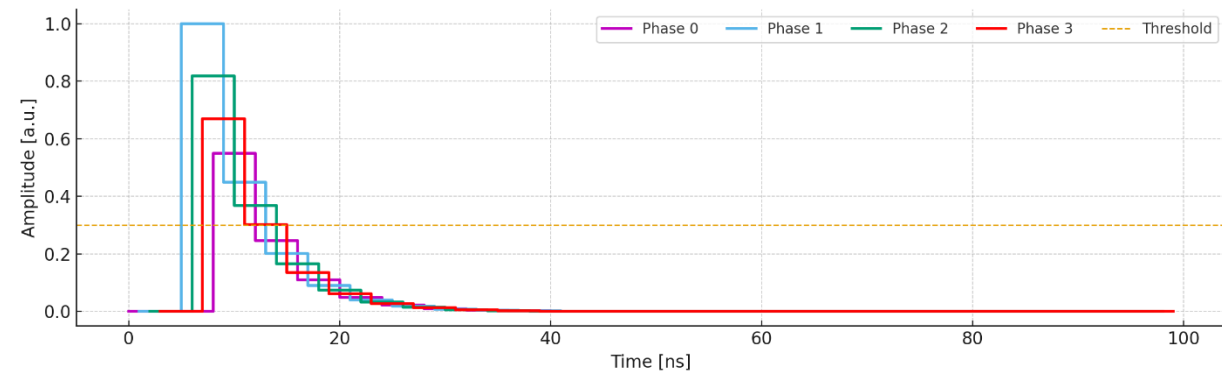
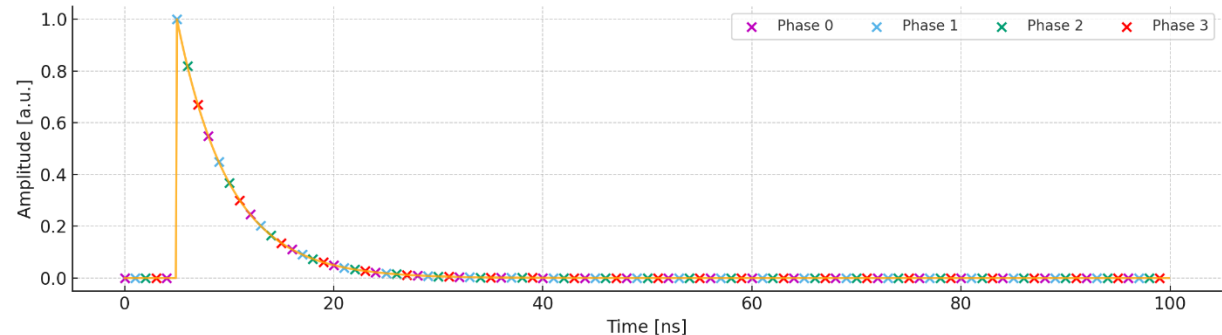
1 GHz



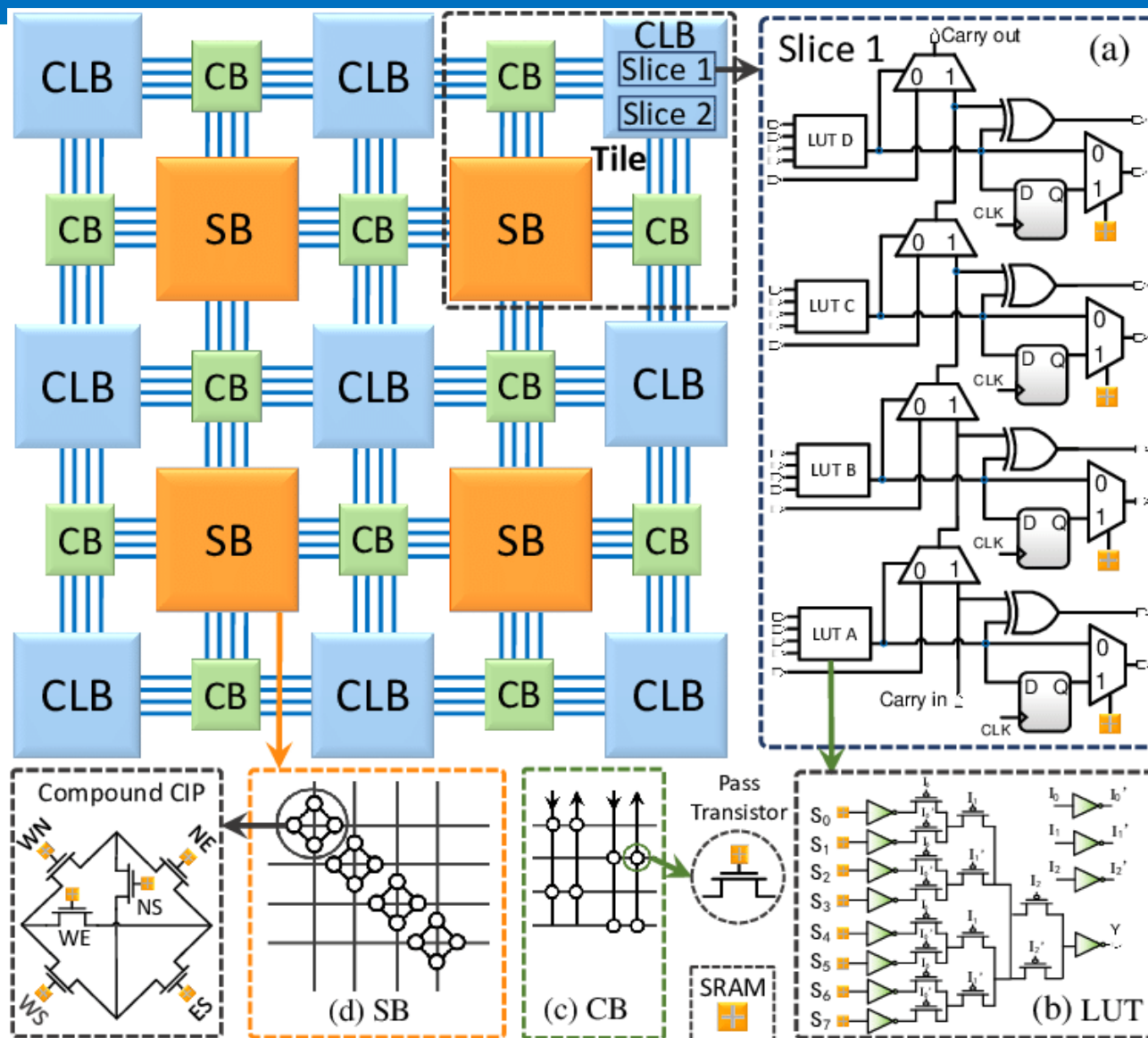
Serial Link



250 MHz

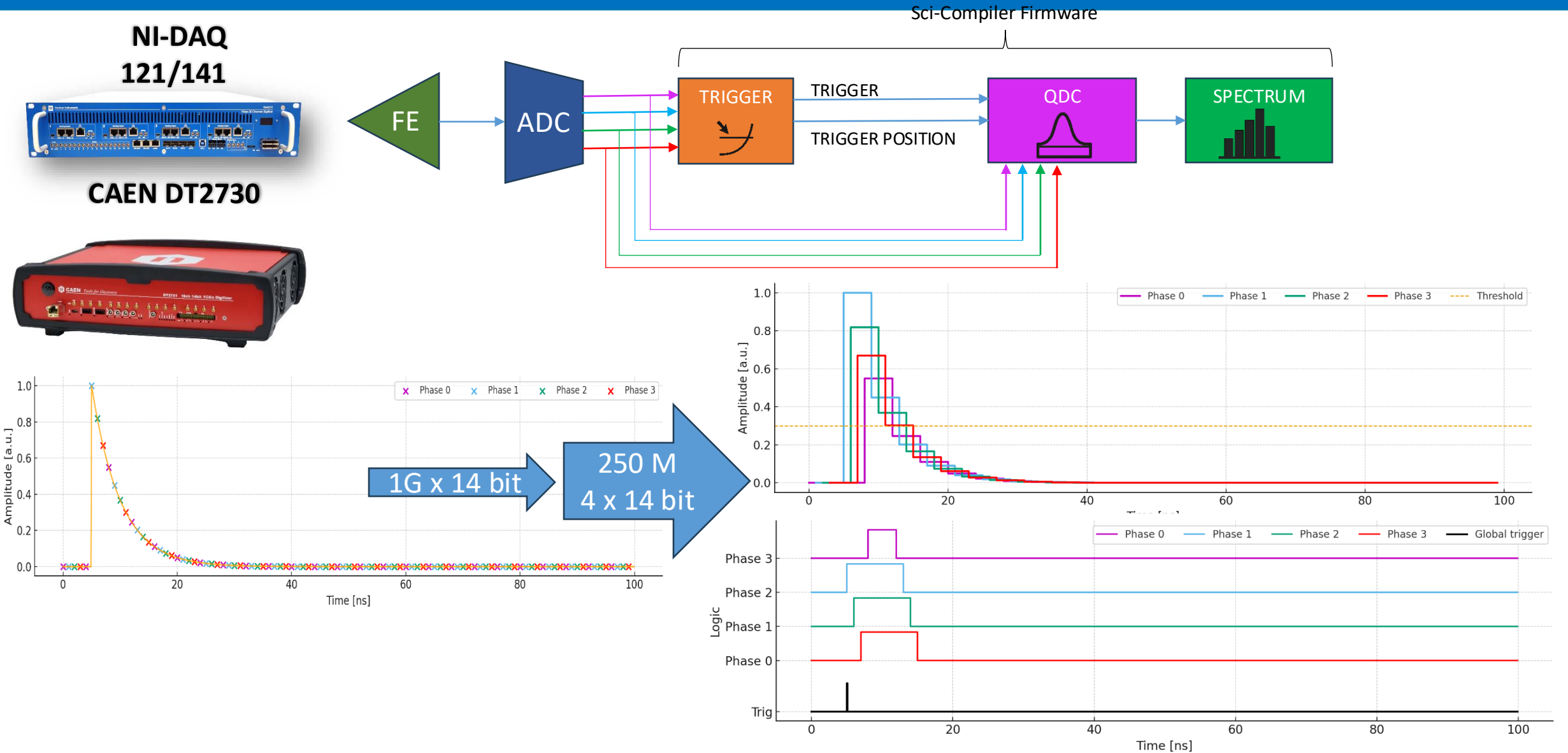


# Ultra-High Speed Digitizer: FPGA clock speed limit

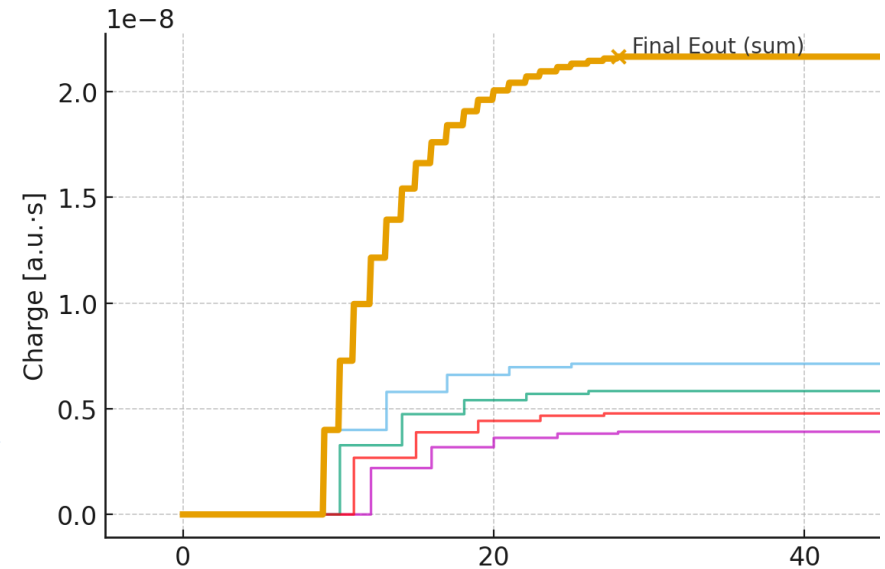
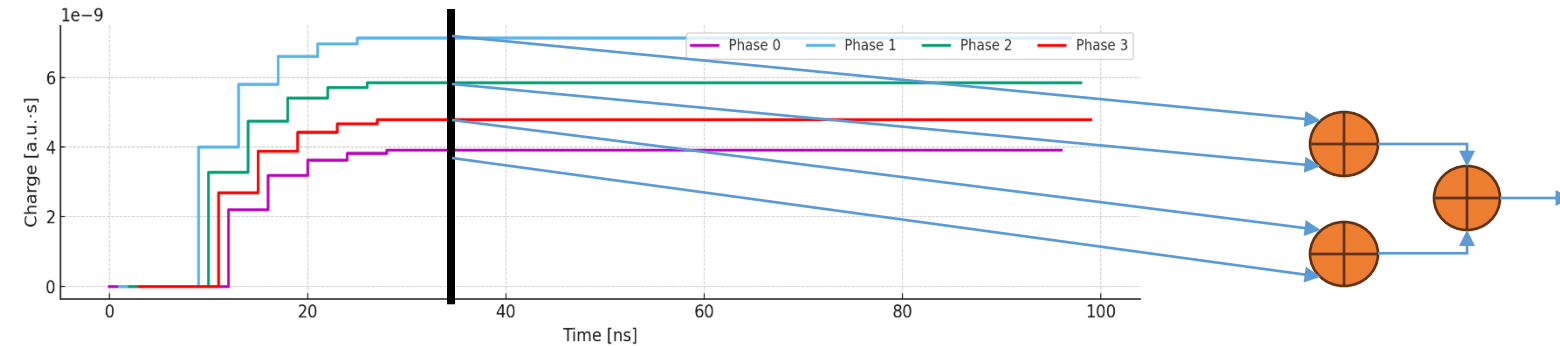
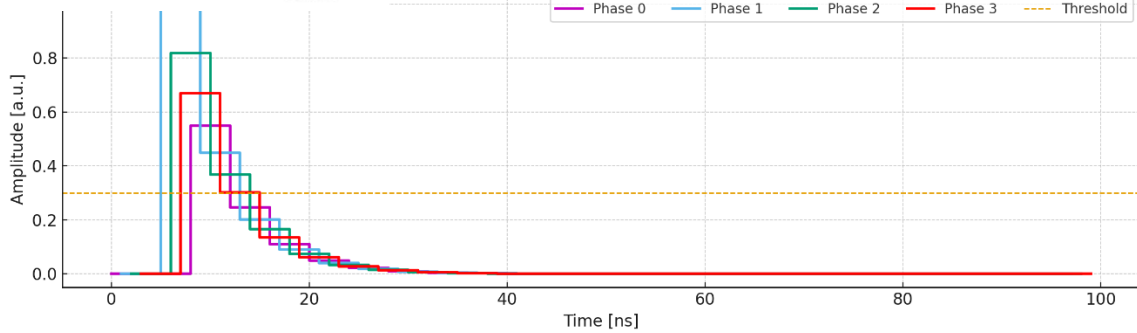
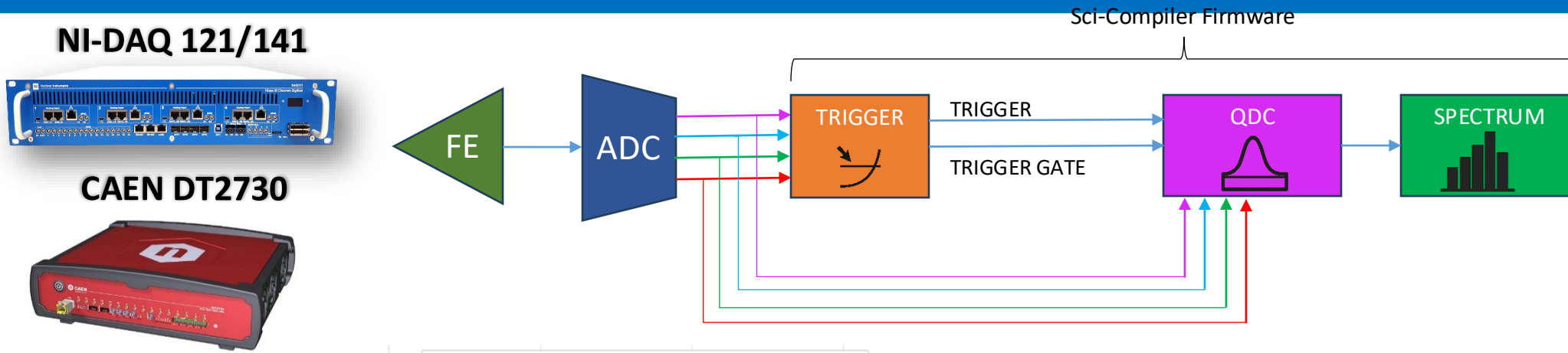


- Programmable FPGA architecture limits maximum clock speed
- Modern FPGA optimized designed may operate in the range 250 – 400 MHz
- Congestion in the device reduce maximum speed
- Safe margin must be considered for “open hardware” configurable application

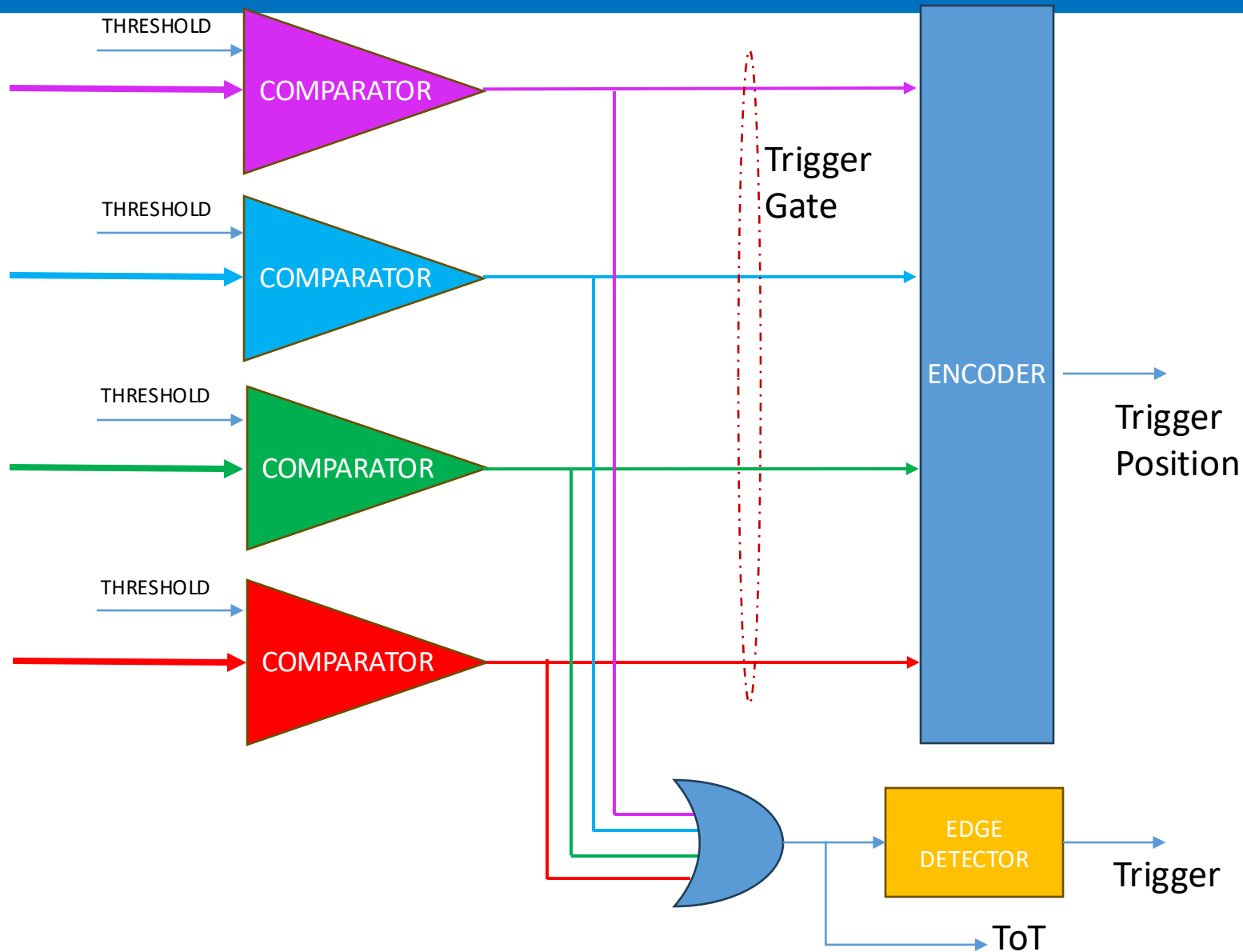
# Parallel QDC implementation



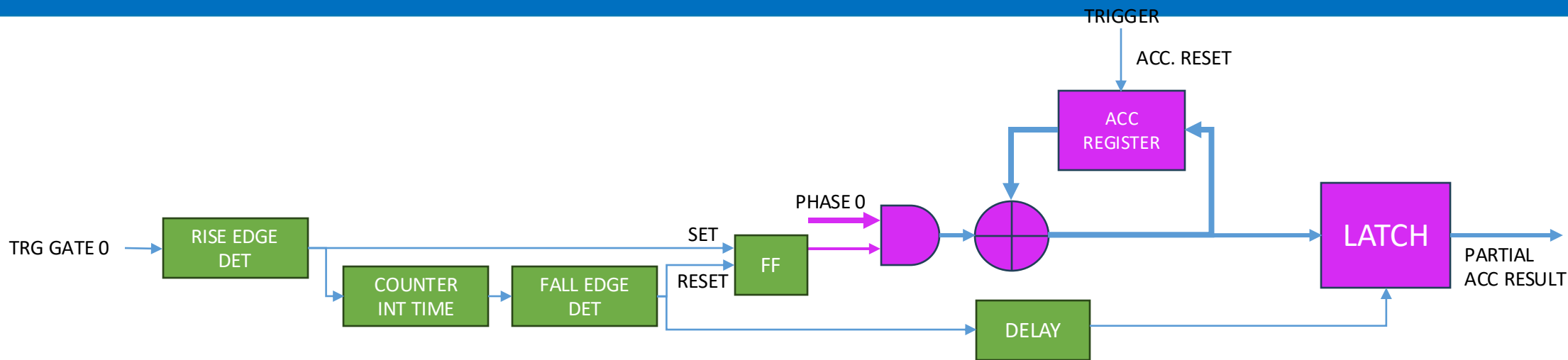
# Ultra-High Speed Digitizer: Parallel QDC implementation



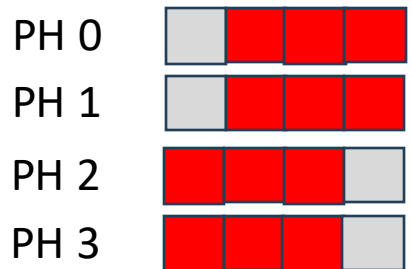
# Parallel QDC implementation



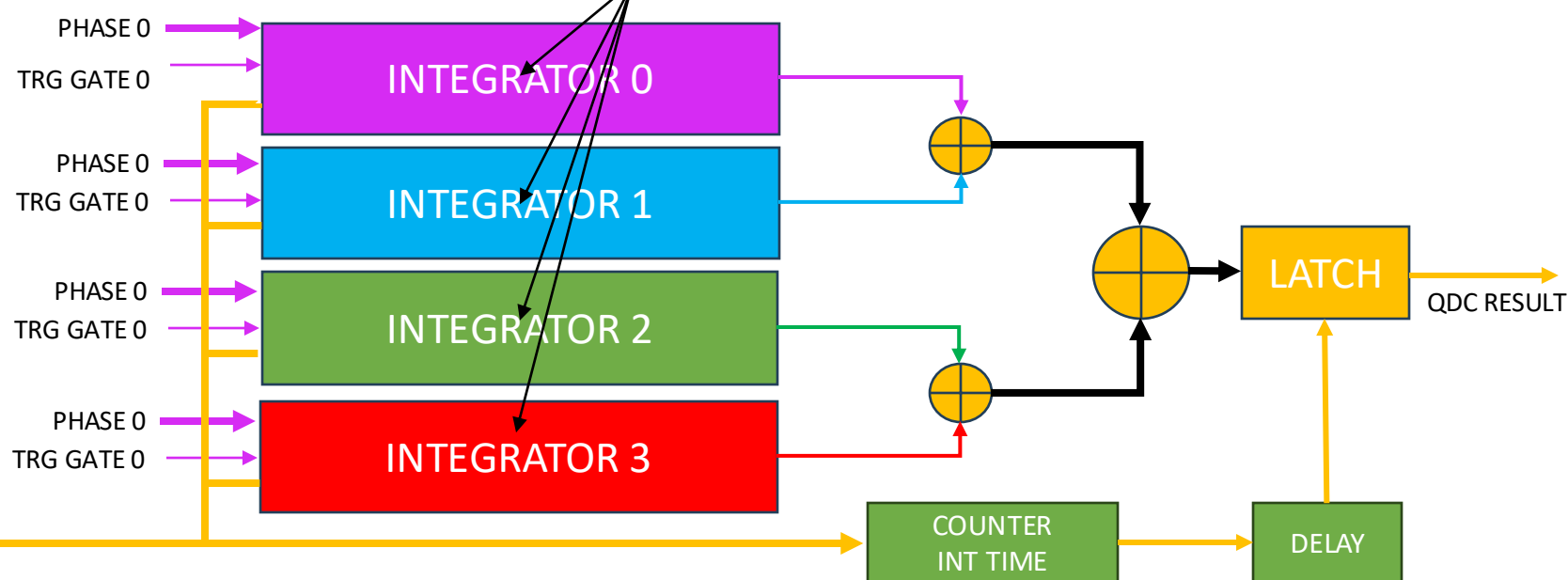
# Parallel QDC implementation



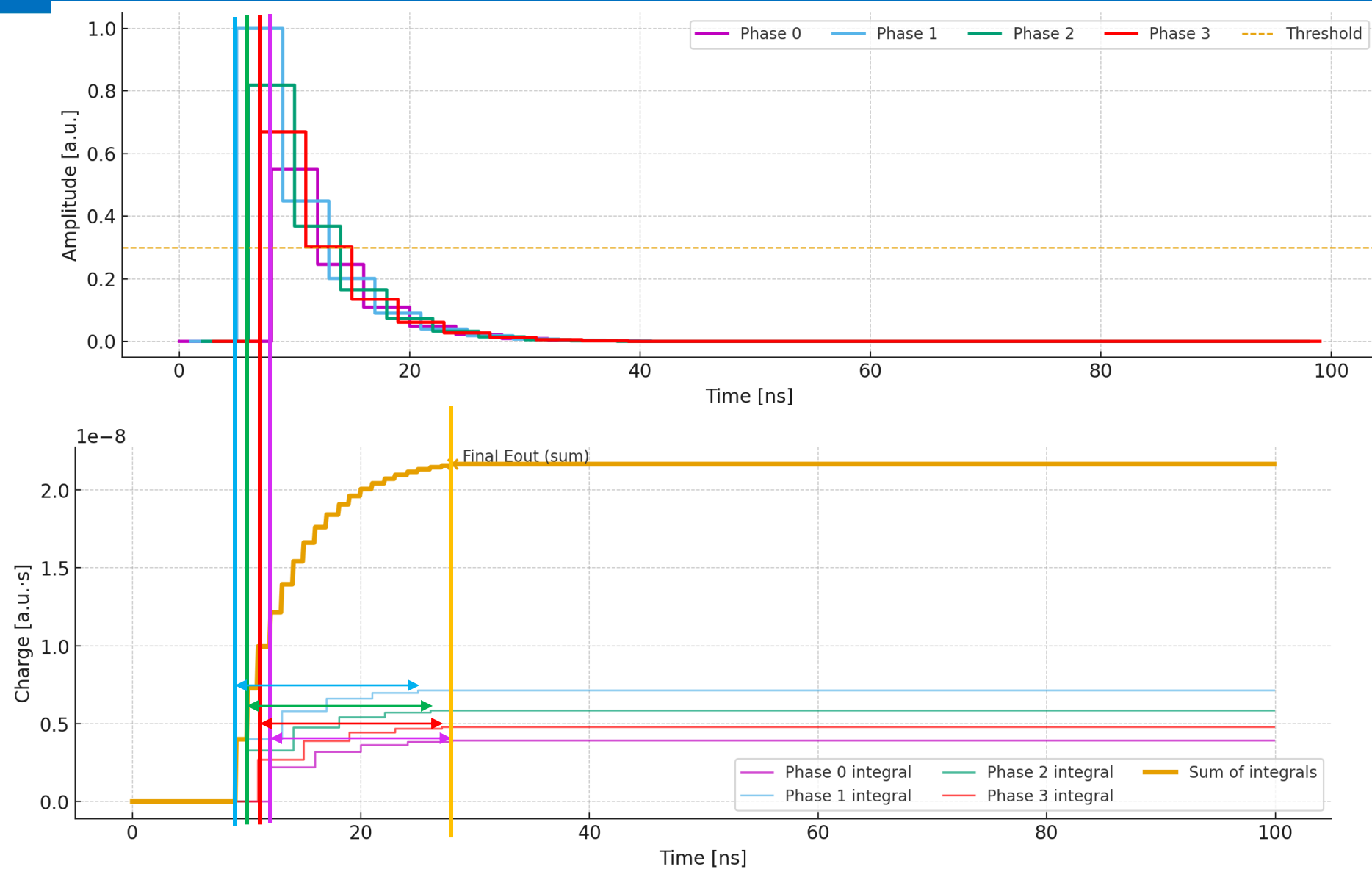
## 12 sample integration



■ Integrated  
■ NOT Integrated



# Parallel QDC implementation

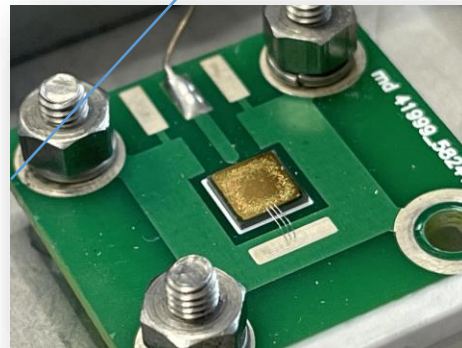


# Parallel trapezoidal implementation

DT9000 → 5 Gbps  
upcoming digitizer family



Diamond Detector



## High-Energy Physics

- Particle tracking in collider experiments
- Radiation-hard sensors for extreme environments.

## Nuclear Physics & Fusion

- Neutron detection and spectroscopy.
- Monitoring of intense radiation fields in fusion reactors.

## Medical Physics

- Dosimetry for radiotherapy and proton therapy (high precision and radiation hardness).
- Real-time monitoring of therapeutic beams.

## Space & Astrophysics

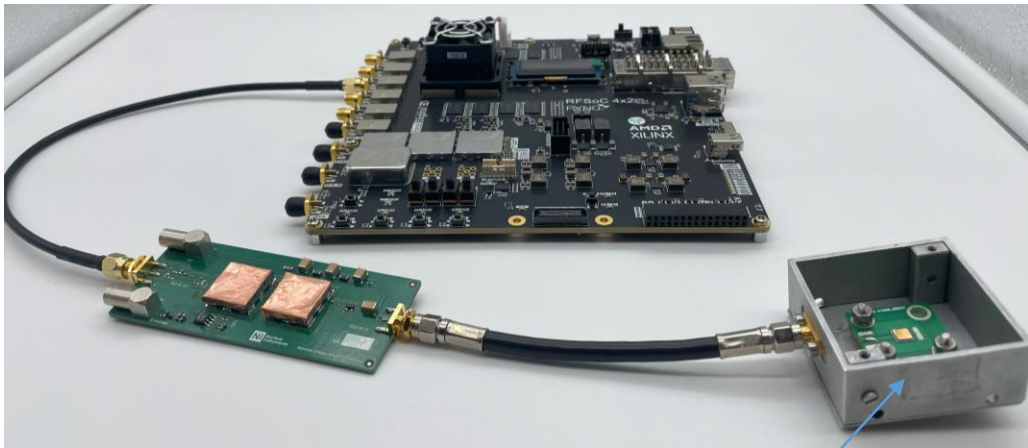
- Radiation monitoring in satellites and space missions.
- Detection of cosmic rays and solar particle events.

## Industrial & Security Applications

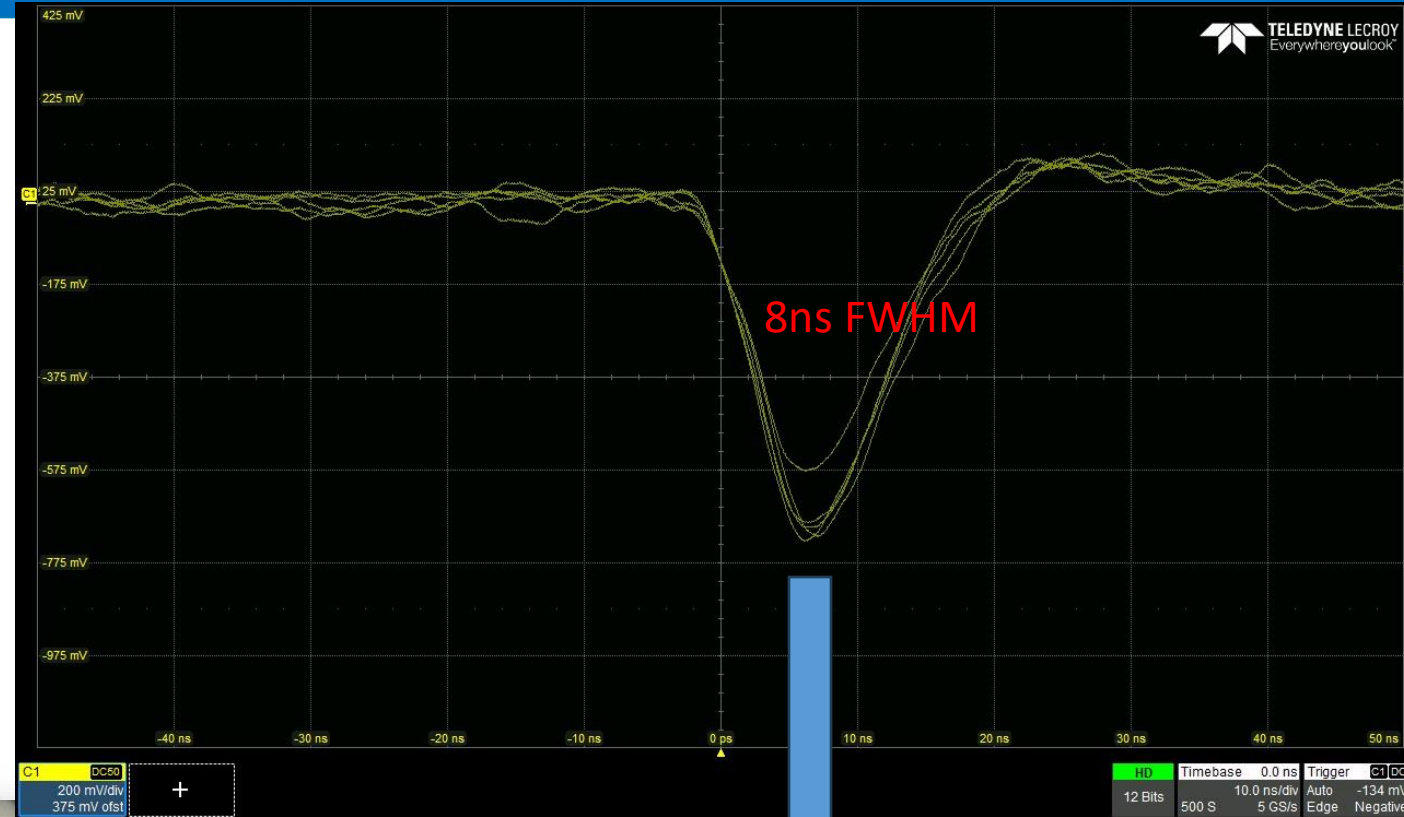
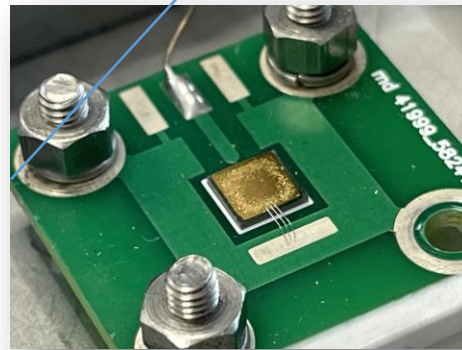
- Beam diagnostics in accelerators and synchrotrons.
- Non-destructive testing using radiation.
- Radiation monitoring in nuclear facilities.

# Parallel trapezoidal implementation

DT9000 → 5 Gbps upcoming digitizer family



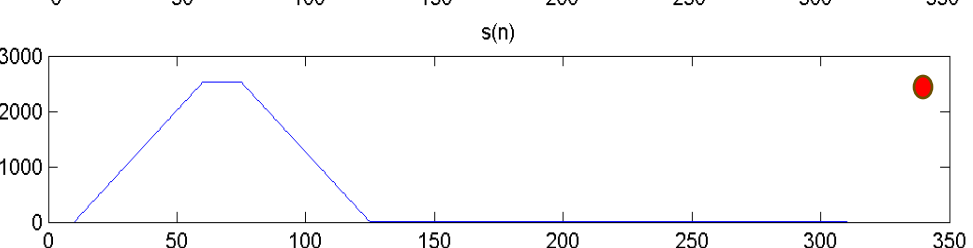
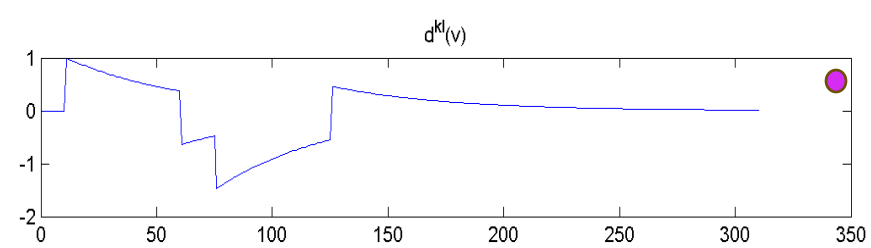
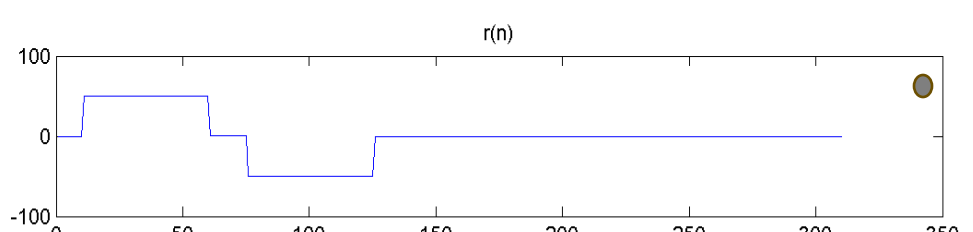
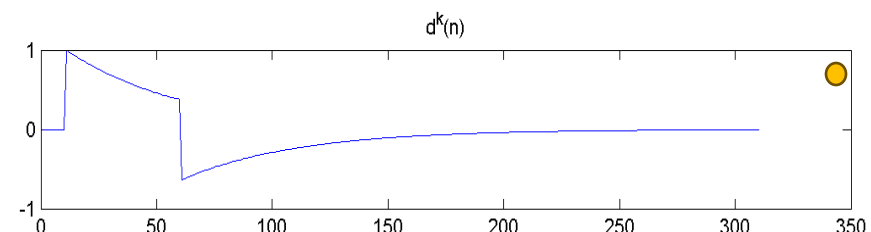
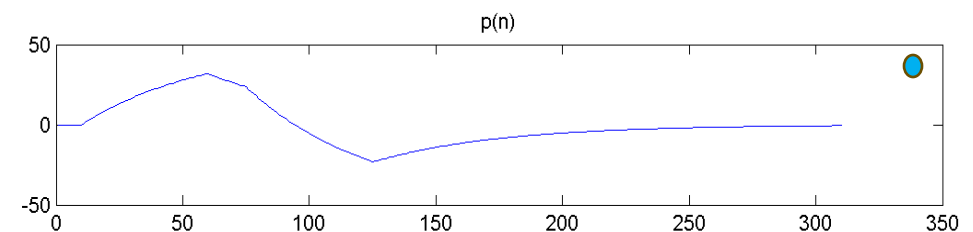
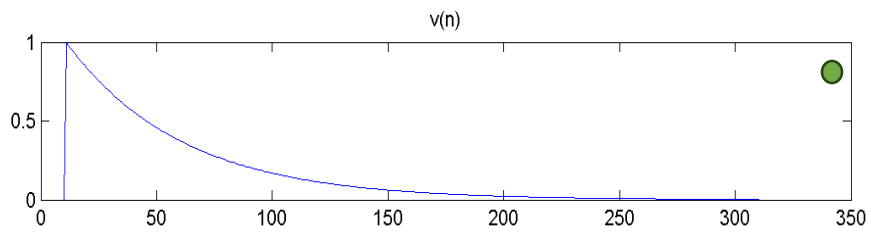
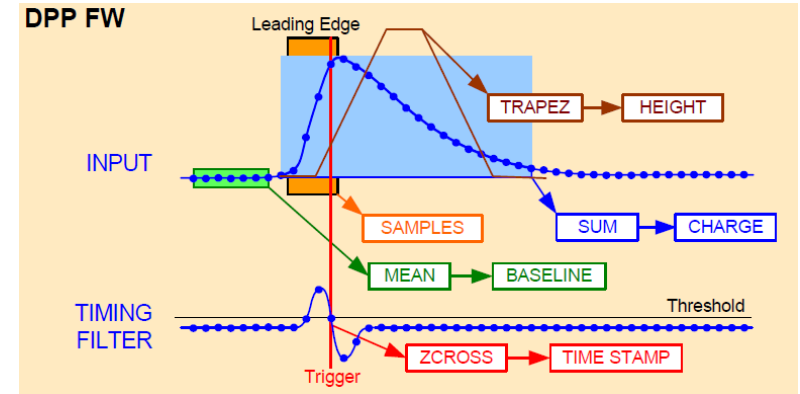
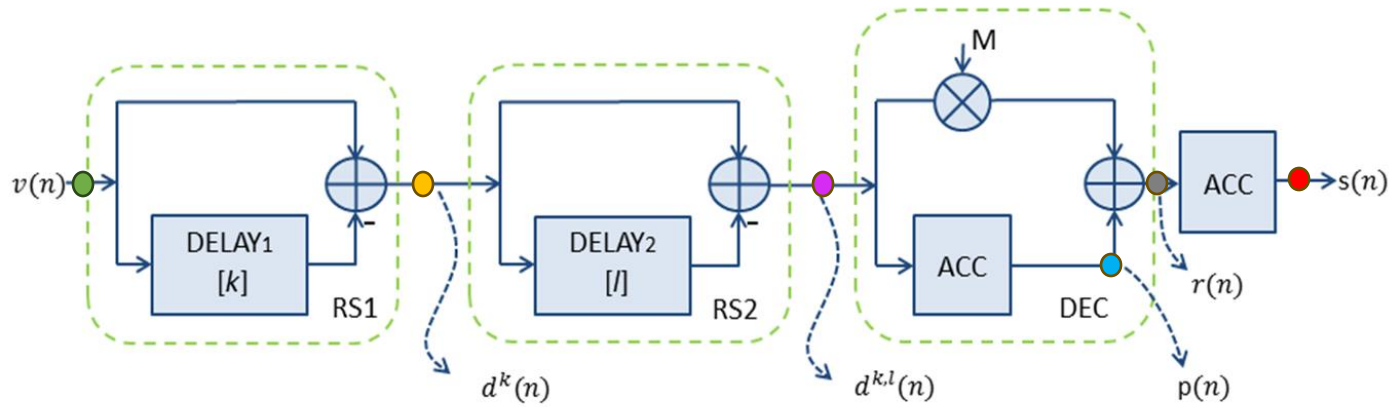
Diamond Detector



Ultra Fast signal response

Fast digitizer and new processing algorithms

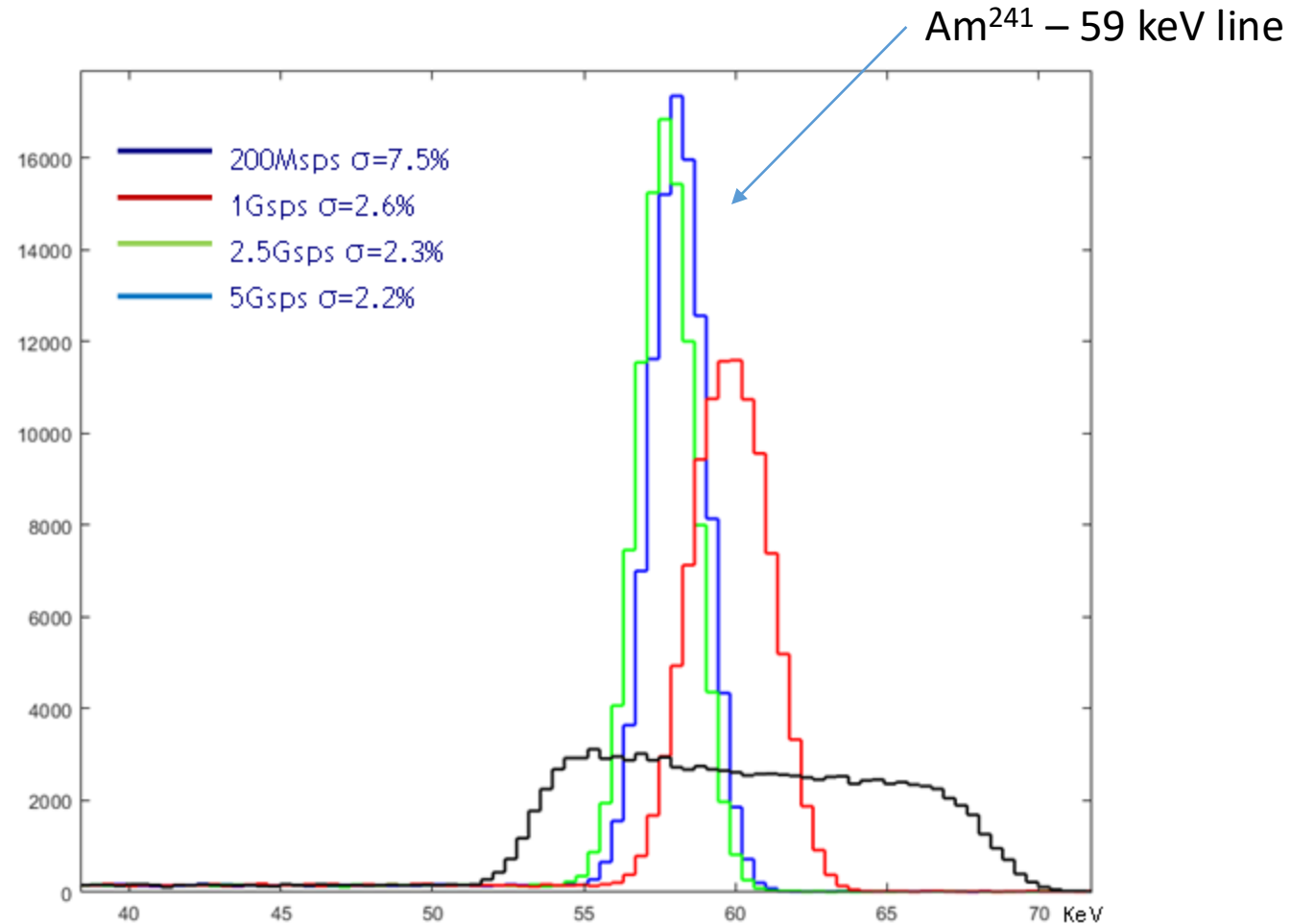
# Parallel trapezoidal implementation



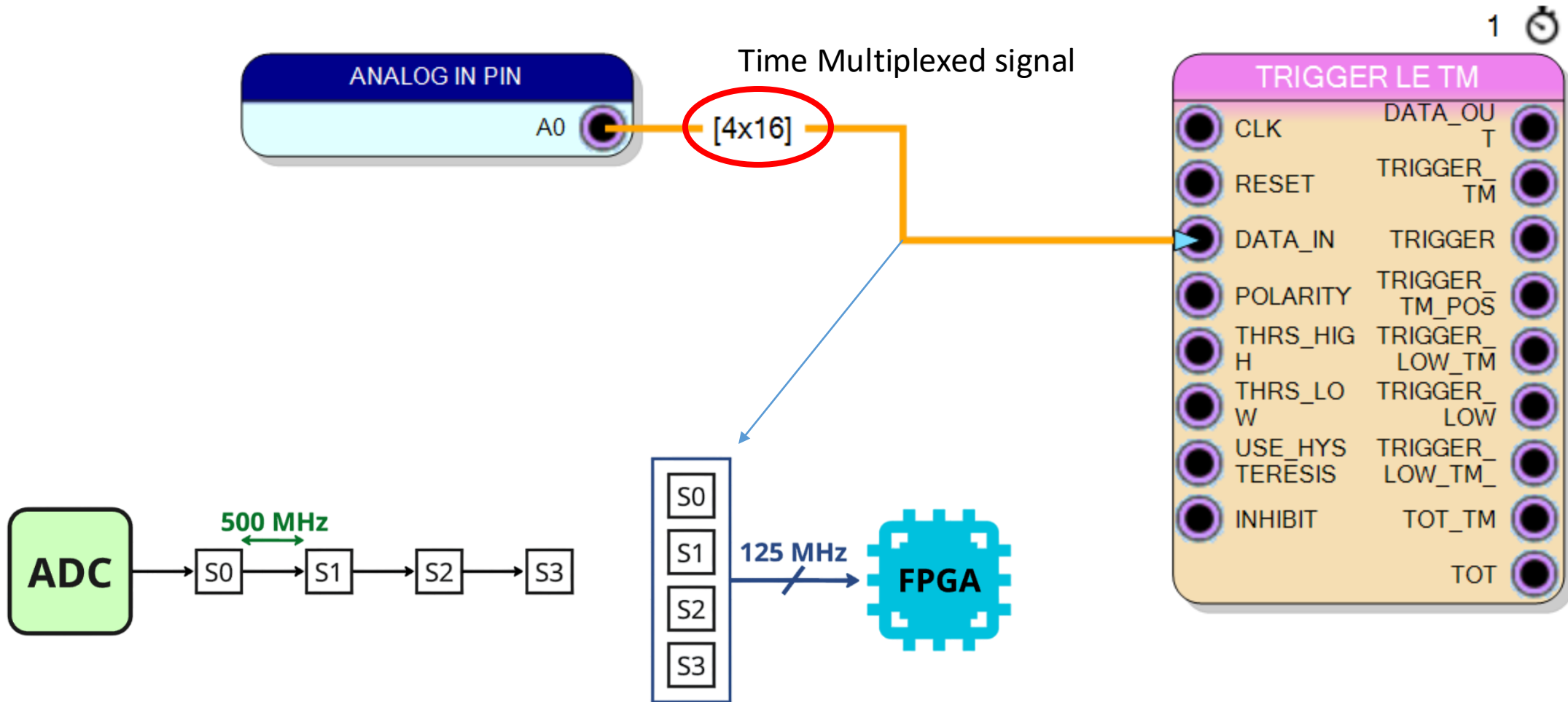


# Parallel trapezoidal implementation

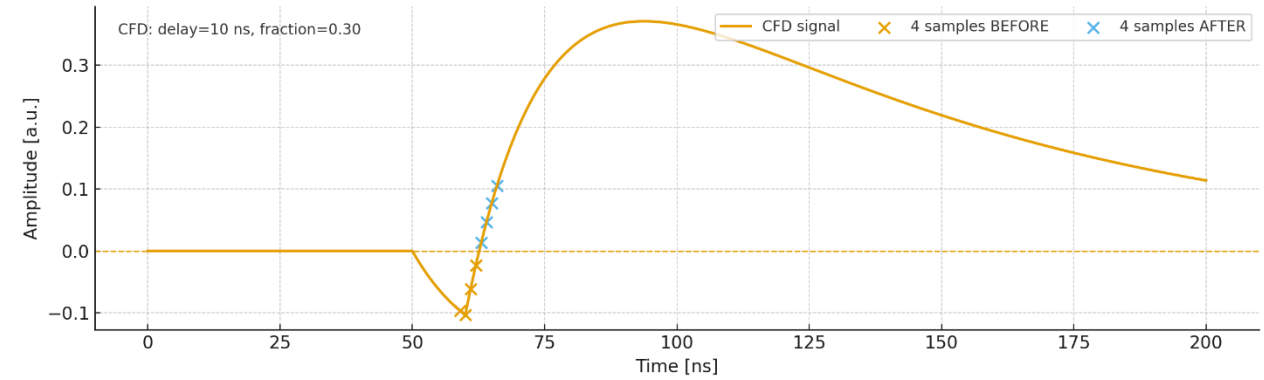
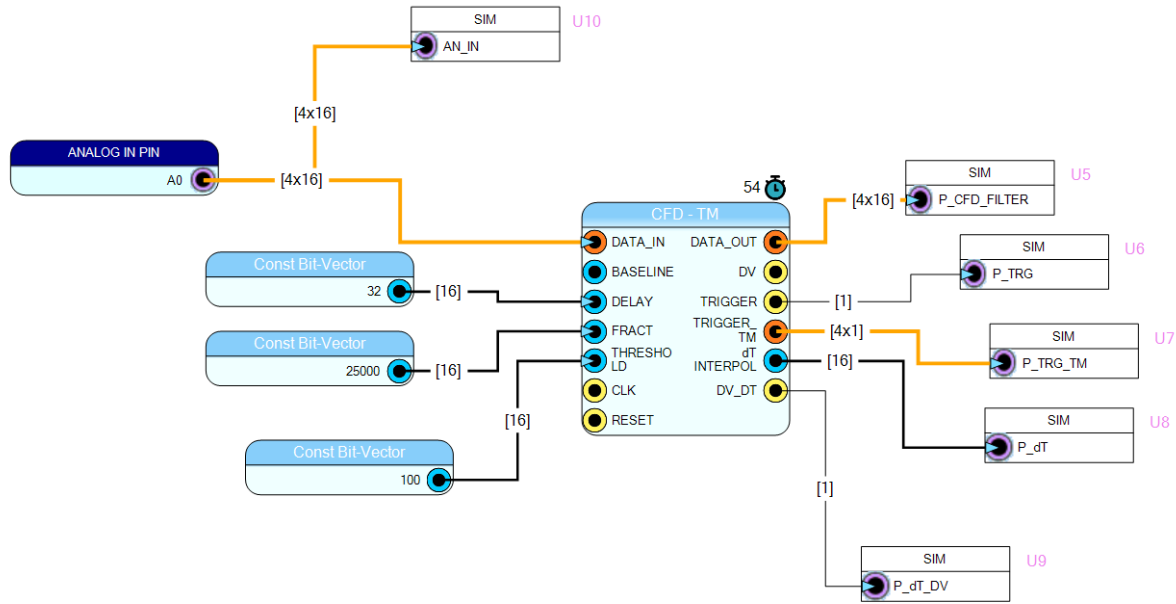
Resolution comparison at different sampling rate and constant shaping time for 20ns decay signal from diamond detector



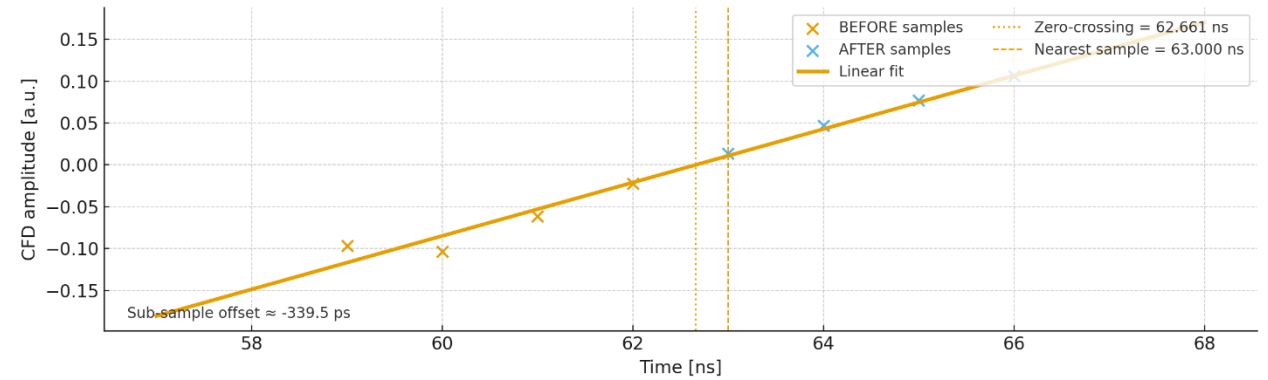
# Sci-Compiler TM signals



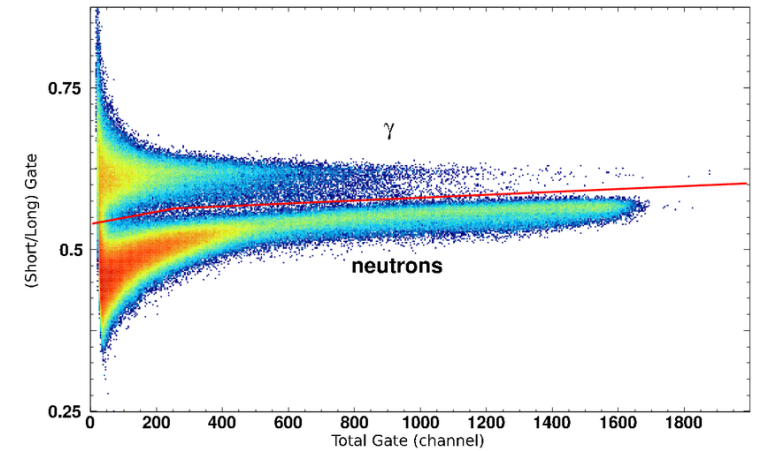
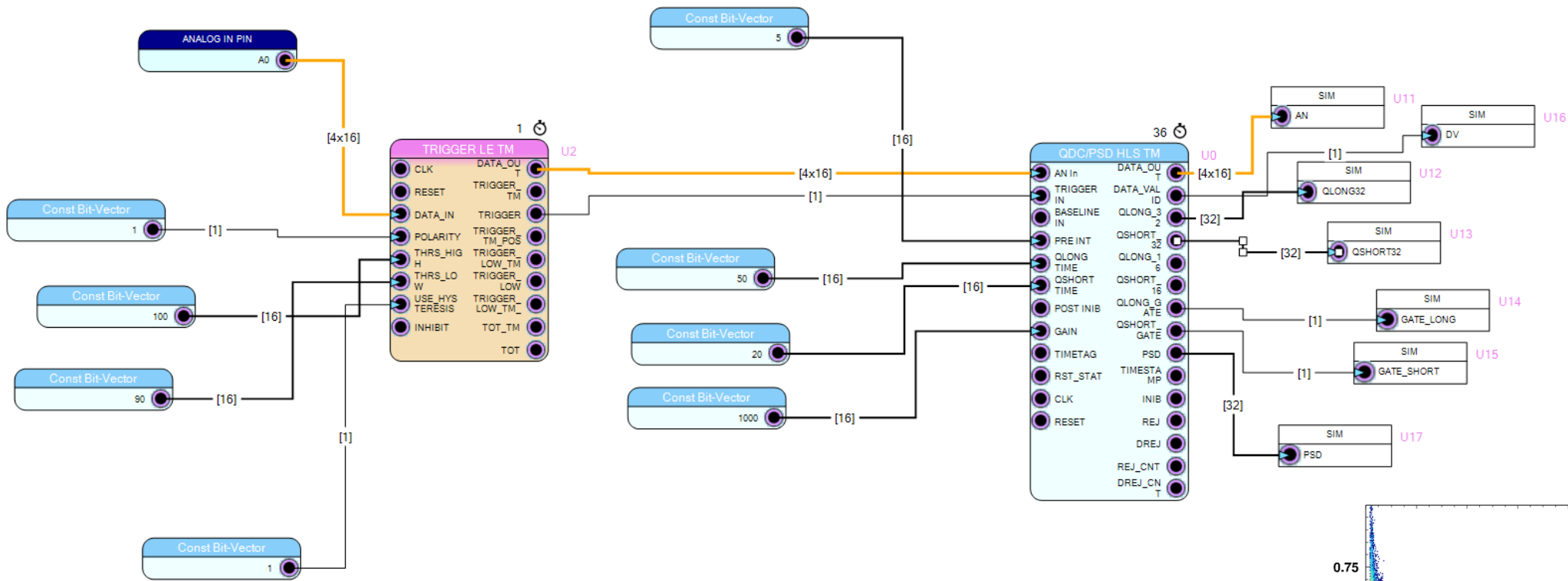
# Sci-Compiler TM signals



Sub-sample interpolator



# Sci-Compiler TM signals



# (ISIS) Realtime PSD on GS20 scintillator and Nanoparticles detectors

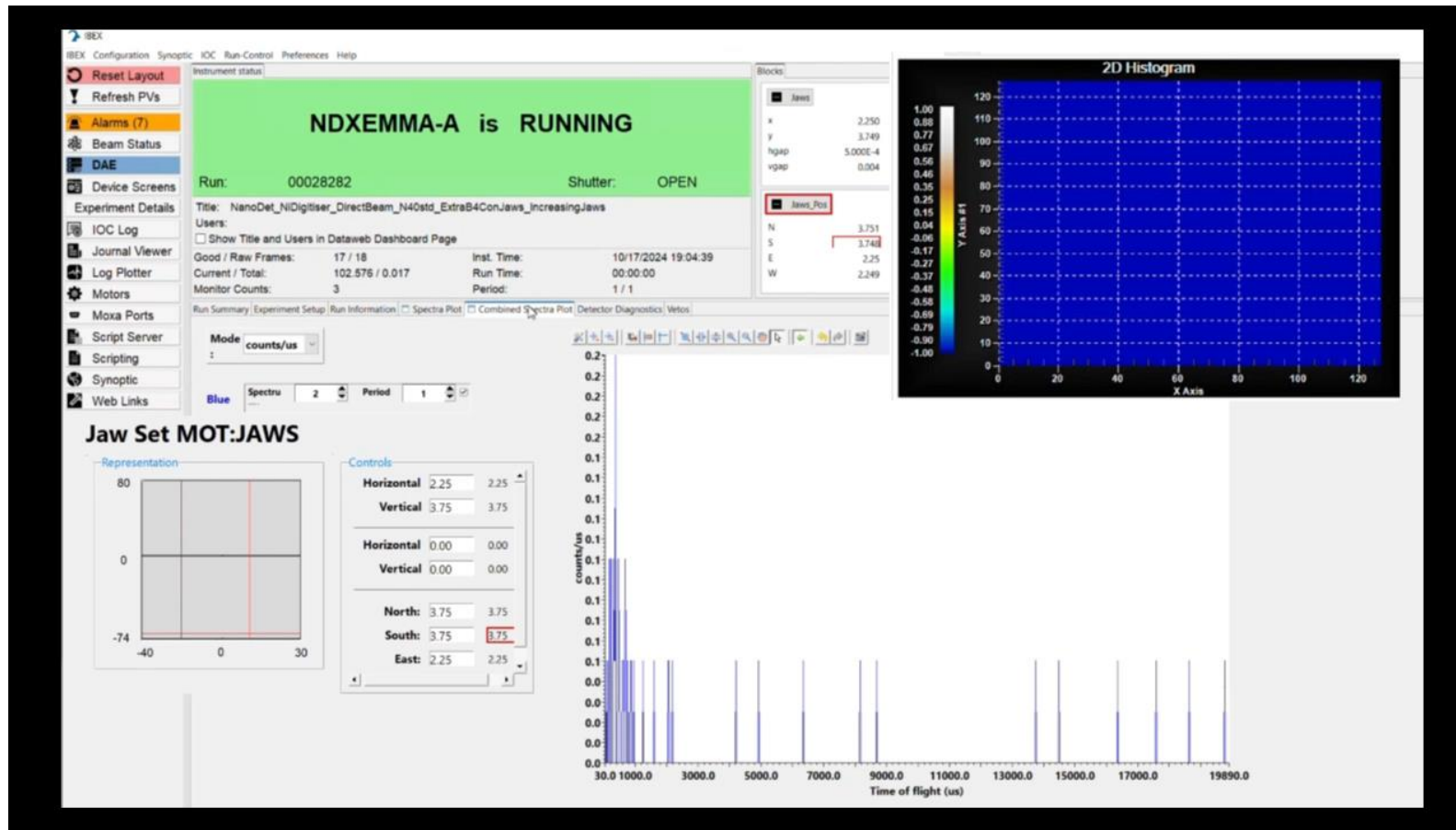


DAQ 121 Real Time Processor

220 ns Latency  
Up to 50 Mcps



ISIS DAE



# Fission Fragment Gamma Spectroscopy

Combination of different Gamma detector arrays:

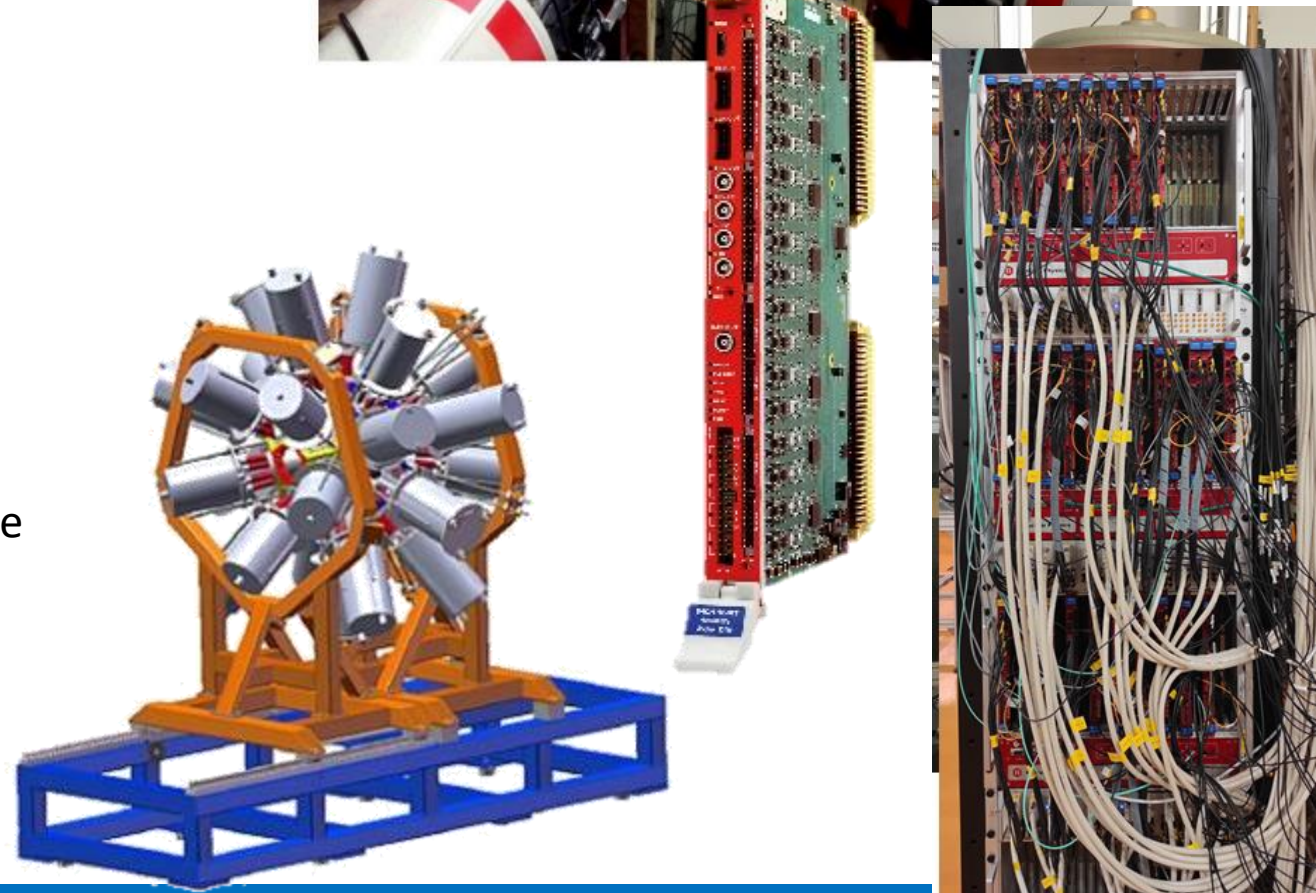
- HPGe (Clover) for high energy resolution
- BGO for Anti-Compton Shield
- LaBr<sub>3</sub> for fast timing information (prompt gamma coincidences)

Several installations with similar requirements:

- **VENUS @ VECC (Kolkata)**
- **ROSPHERE Array @ ELI-NP (Romania)**

Readout Modes:

- BGO: 250/500 MS/s, 14 bits, QDC algorithm (gated charge integration)
- LaBr<sub>3</sub>: 500 MS/s, 14 bits, QDC + CFD algorithms (charge integration + high resolution timing interpolation)
- LVDS I/Os for sync/trigger/inhibit distribution among the boards



# RFX (Padova) Neutron Monitor

## Scientific Goals

- **Neutron measurement** as a direct indicator of fusion reaction rate and fusion power.
- Requires **accurate neutron/gamma discrimination (PSD)**.

## Detector Setup

- **Three scintillator-based detectors** installed below the vacuum vessel.

## Scintillators:

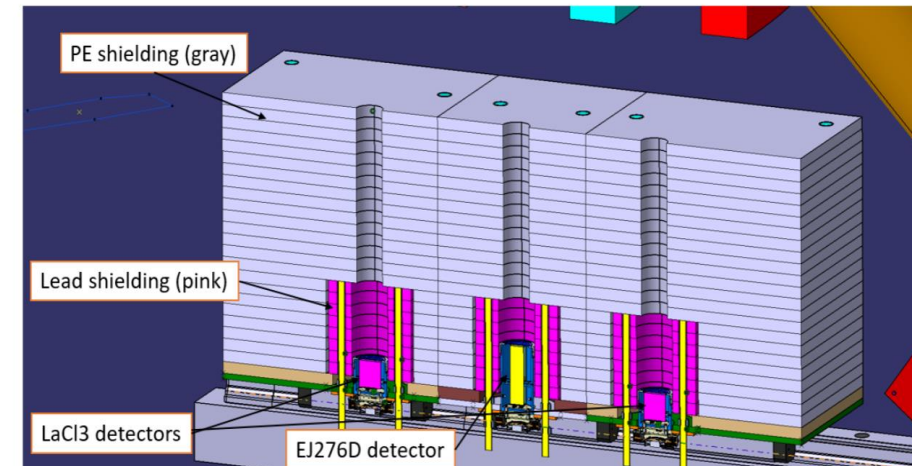
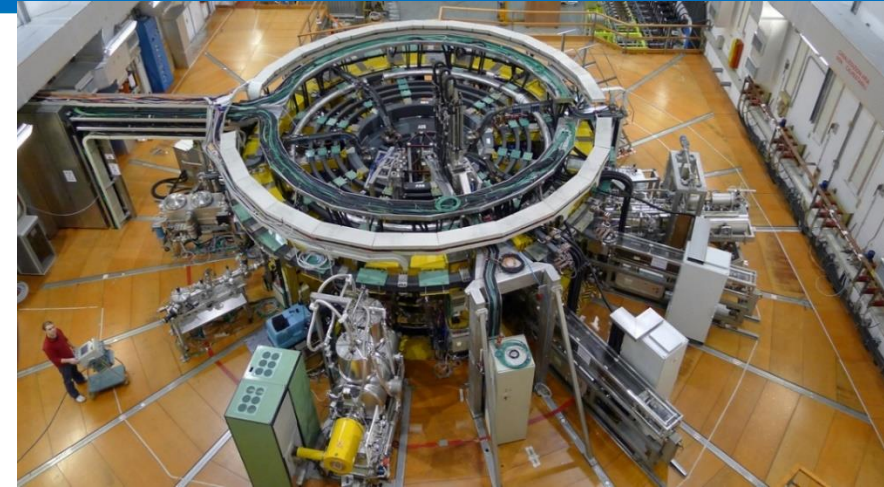
- **EJ276D (25×25×100 mm, plastic)**: fast response, excellent n/γ discrimination, efficient for fast neutrons (no spectral info).
- **LaCl<sub>3</sub> (∅1" × 1")**: provides spectral information (discrete peaks), fast (~50 ns) but poor n/γ discrimination → needs advanced algorithms.

## Readout & Acquisition

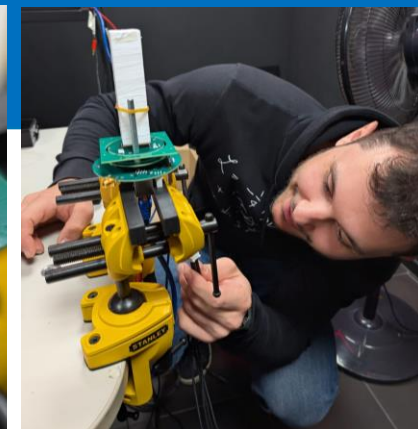
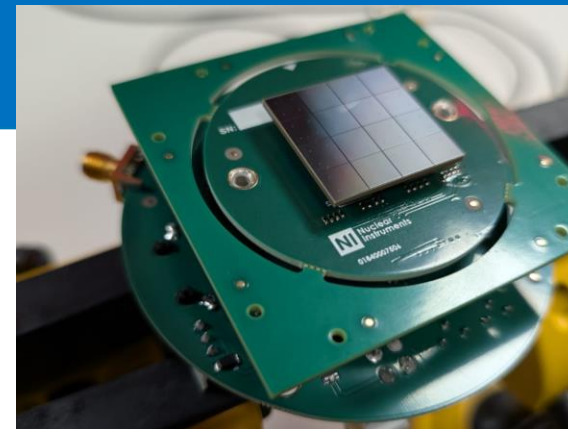
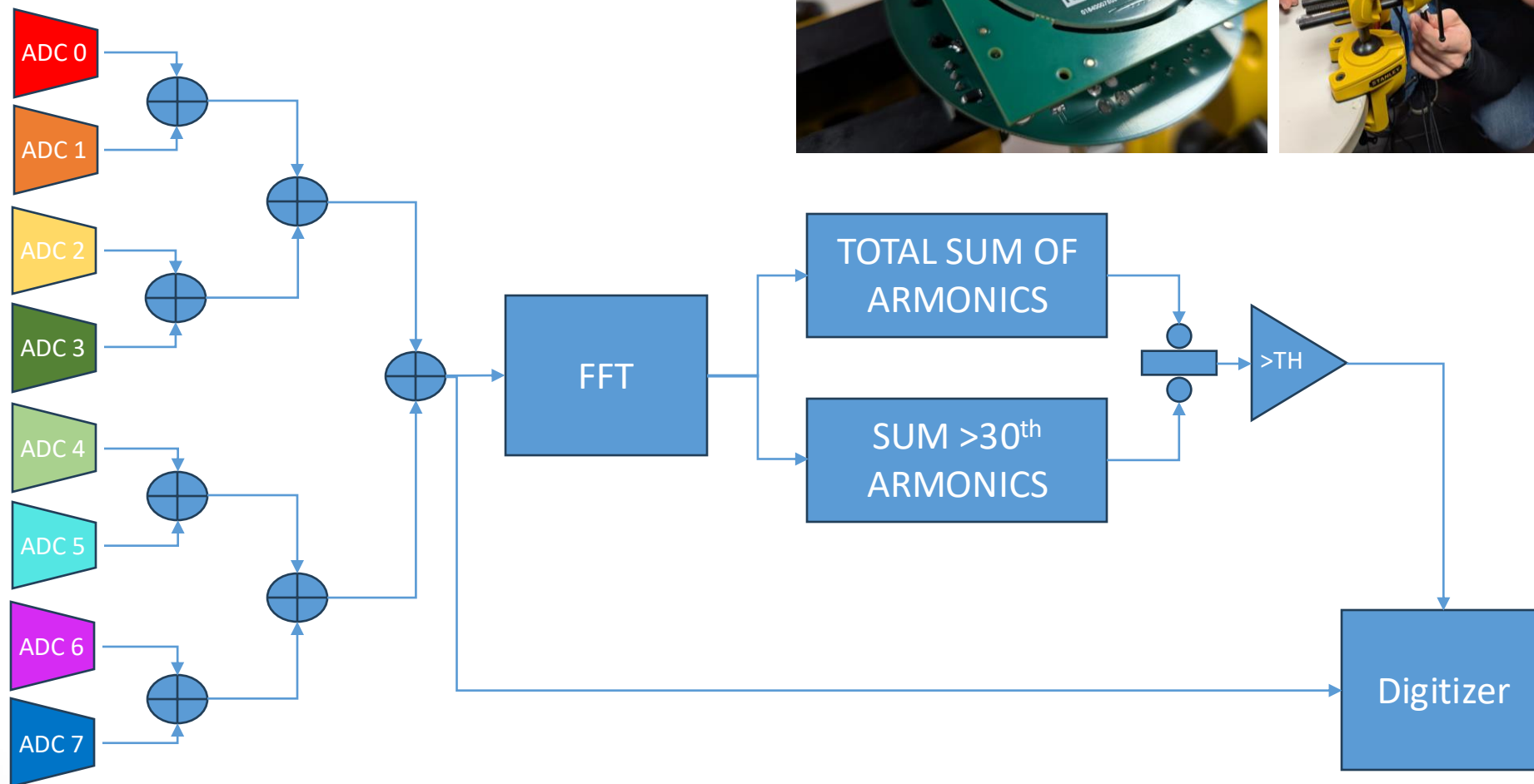
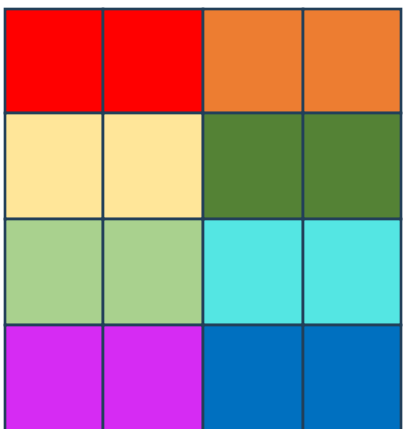
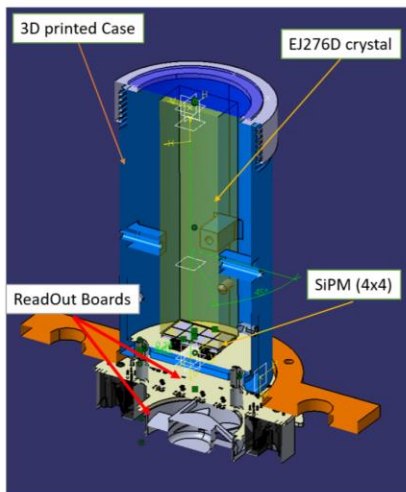
- All crystals coupled to **SiPM arrays (4×4)**, grouped and summed analogically.
- Signals sampled by **NI DAQ121** with **full waveform**
- **Typical discharge**: ~1 s, average ~1 kHz, bursts (100 μs–1 ms) from magnetic reconnection events.

## PSD Methods

- Standard PSD effective for EJ276D but **ineffective for LaCl<sub>3</sub>**.
- **FFT-based approach**: compute FFT for each event and evaluate amplitude ratio → **improves neutron/gamma separation**.

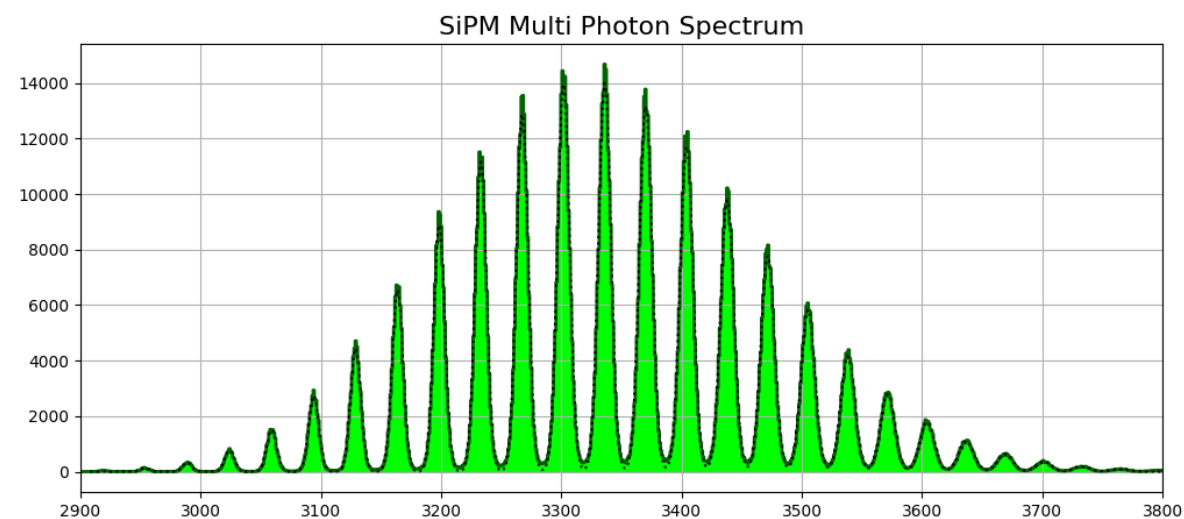


# RFX (Padova) Neutron Monitor: Firmware

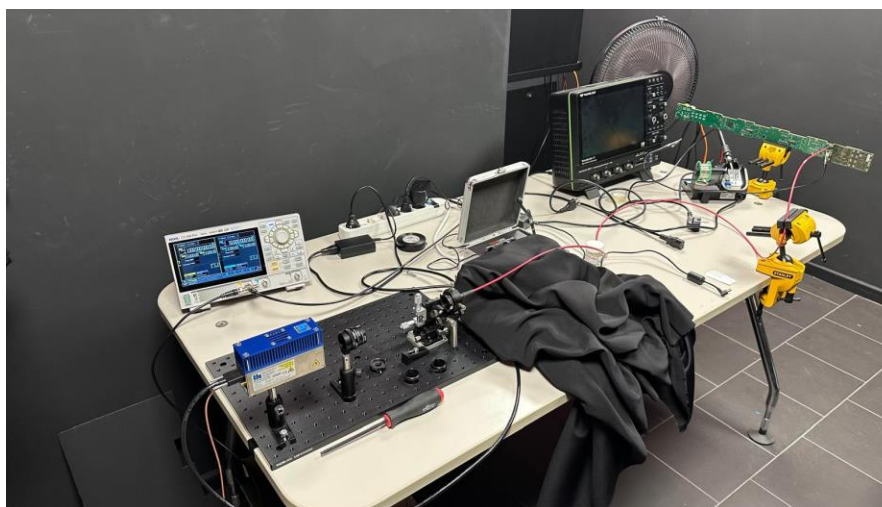


# Quantum optics and quantum computing

- Measurement of quantum correlation in optical states
- Very Low noise  $<$  Shot Noise
- Quantum Entangled states
- Single photon counting
- Hamamatsu S13360 MPPC
- 1 Gsps 14 bit Nuclear Instruments Digitizer with real-time pulse processing.



Hamamatsu S13360-1325



# FAST DIGITIZER WITH TM SUPPORT



DAQ121 – 1 Gbps 32 channels – 12 bit  
DAQ122 – 1 Gbps 32 channels – 14 bit  
*(differential input)*  
(COMPATIBLE WITH ESS & ISIS READOUT)



CAEN V2730 – 500 Mps 32 channels – 14 bit  
CAEN V2751 – 1 Gps 16 channels – 14 bit  
*(single ended input)*

DT5571

DT5560

DT1260

V2495

V2751  
V2730  
V2740/5

20 bit !!

DT5550W

R5560

NI Nuclear Instruments  
SCICOMPILER  
OPENFPGA  
HARDWARE PLATFORMS

CAEN  
Tools for Discovery