Firmware Architecture for the ePixUHR Detector Enabling 35-kHz X-ray Imaging with Real-Time FPGA/GPU Processing

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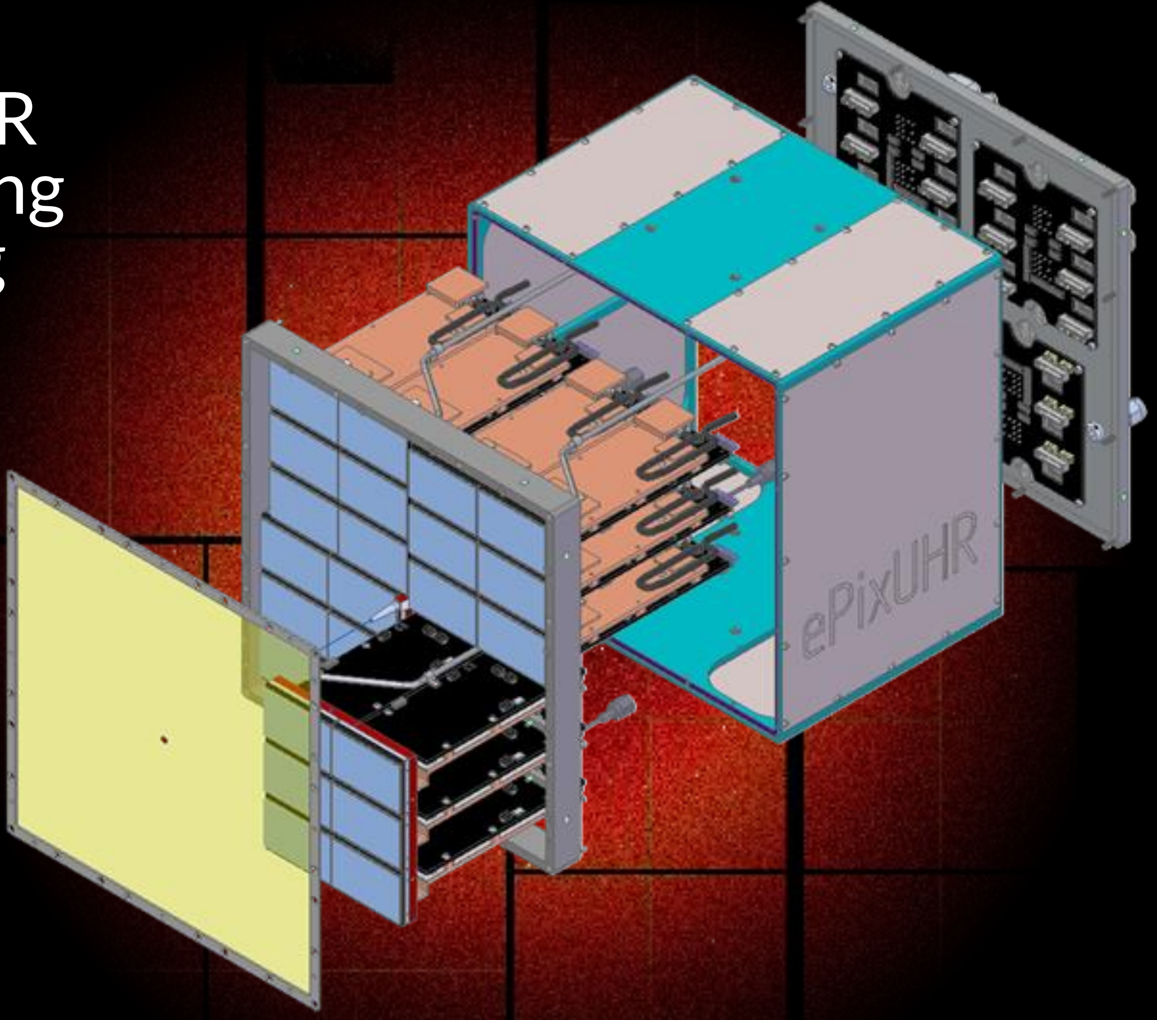
*on behalf of SLAC X-ray Detector R&D Program



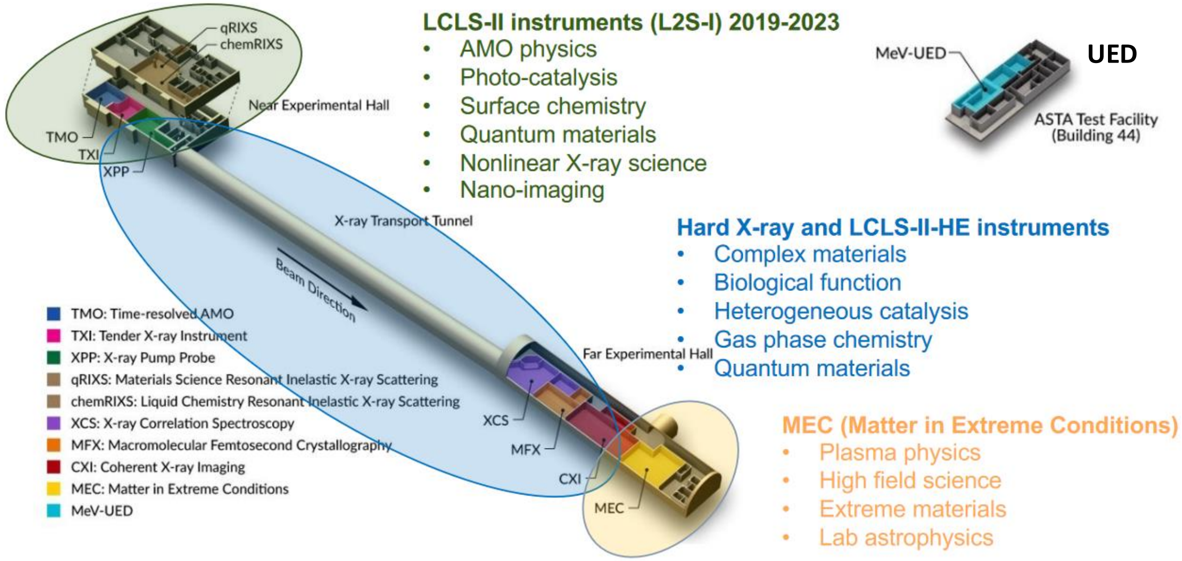
May 2026

SLAC NATIONAL ACCELERATOR LABORATORY
Stanford University
U.S. DEPARTMENT OF ENERGY

LCLS, LCLS-II, and LCLS-HE

- **L**inac **C**oherent **L**ight **S**ource (2009)
  - Continuous repetition rate of 120 Hz.
- LCLS-II (2023)
  - Superconducting Linac capable of **1 MHz** beam rates for soft X-ray beamlines. Currently running user operation at 33 kHz – 93 kHz for soft X-ray hutches.
- LCLS-II-**H**igh **E**nergy (2028)
  - Extend the superconducting Linac to the **hard X-ray beamlines** (13 keV), and later to 20 keV (low-emittance injector)

The science opportunities of LCLS-II and LCLS-II-HE impose stringent requirements on detectors.



LCLS-II instruments (L2S-I) 2019-2023
- AMO physics
- Photo-catalysis
- Surface chemistry
- Quantum materials
- Nonlinear X-ray science
- Nano-imaging

Hard X-ray and LCLS-II-HE instruments
- Complex materials
- Biological function
- Heterogeneous catalysis
- Gas phase chemistry
- Quantum materials

MEC (Matter in Extreme Conditions)
- Plasma physics
- High field science
- Extreme materials
- Lab astrophysics

Our long-term X-ray detector development plan

"Bigger, faster, higher resolution, and higher energies"

With goals built into projects progressively meeting science priorities and requirements

Ultra-High Rate (UHR)

ePixUHR$_{\text{35kHz}}$ (2019–2027)

- **Full frame 35 kHz for HE first light**
- Sensors for hard X-rays

ePixUHR (2019–2029)

- **Full frame 100 kHz – 1 MHz**
- “General purpose” cameras
- Efficient information extraction (Advanced Calibration / Edge-ML)

ePixHR$_{\text{5kHz}}$ (2016–2023)

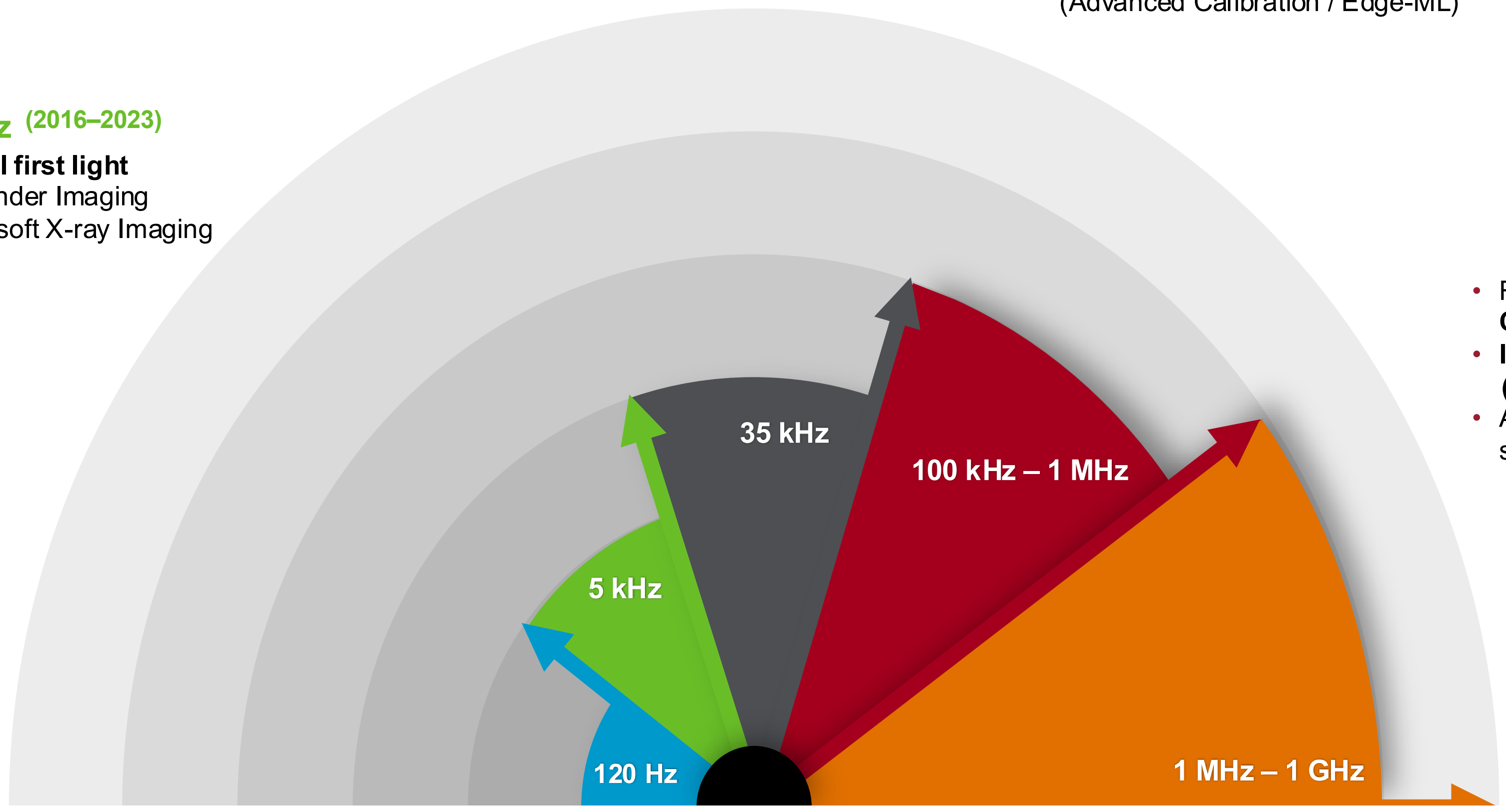
- **5 kHz for LCLS-II first light**
- ePixHR10k for tender Imaging
- ePixHR250M for soft X-ray Imaging

SparkPix (2020–2027)

- Revolutionary **E**xperiment **S**pecific **X**-ray Cameras
- **Information extraction at full rate (1 MHz CW, 3 GHz burst)**
- Advanced features (triggering, sparsification, zero suppression, etc.)

ePix (2013–2018)

- **In use at LCLS**

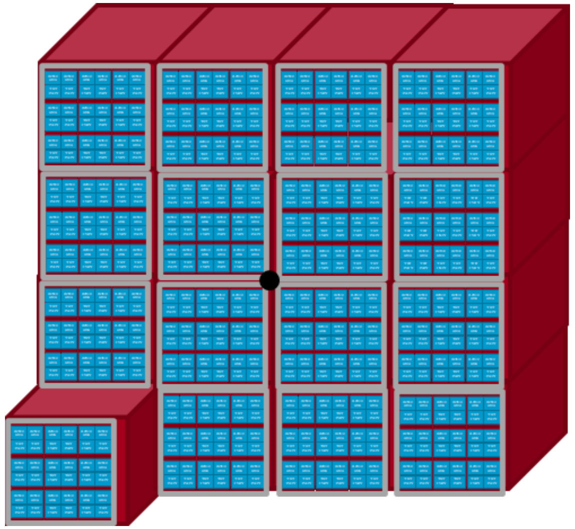


ePixUHR for LCLS-II/HE

A one-of-a-kind Modular Detector

Modular approach with independent "SuperTile" 1-Megapixel detectors

- Serviceable for metrology, calibration, repair
- Independent power, data and cooling lines per module
- All electronics behind the sensor modules
    - Minimizes dead space
- Beam pipe at the center of the detector
- Assembled in-air and in-vacuum



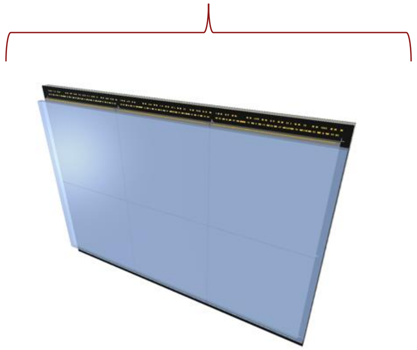
ePixUHR – 16M

ePixUHR – 1M

56 cm x 56 cm

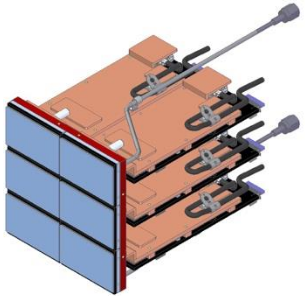
14 cm x 14 cm

ePixUHR 3x2

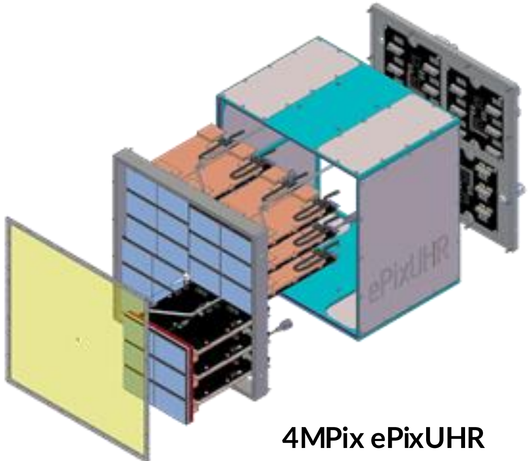


4 cm x 12 cm

ePixUHR – 1M



ePixUHR – 4M



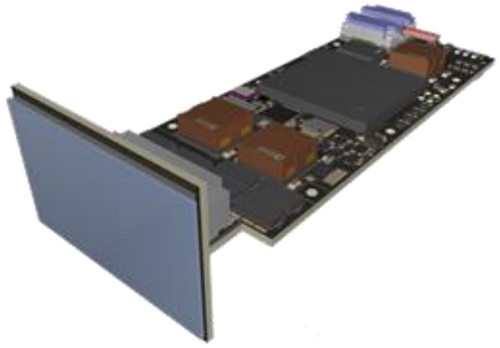
4MPix ePixUHR
35kfps

Beyond HE design

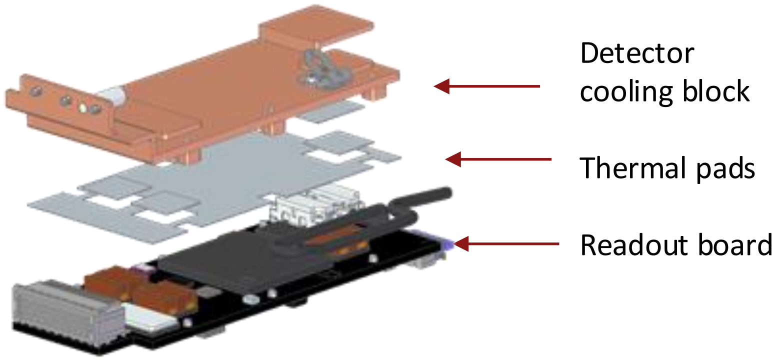
1 Megapixel design

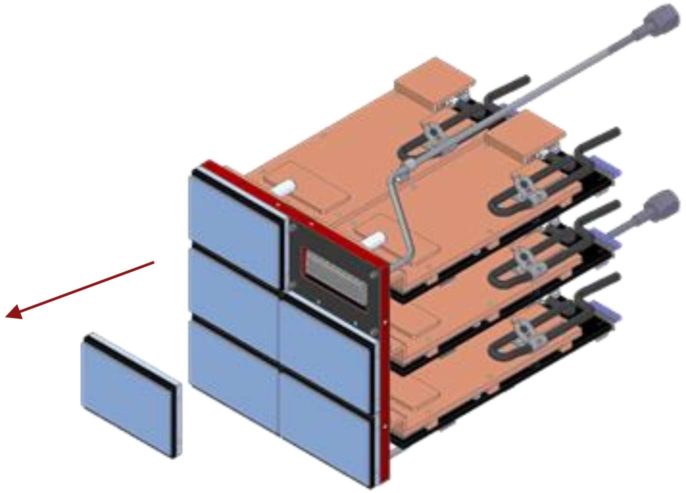
Detector modularity: 6 independent sensor modules per 1 Megapixel

Target temperature at the sensor is 15°C while in vacuum using CO_2 cooling



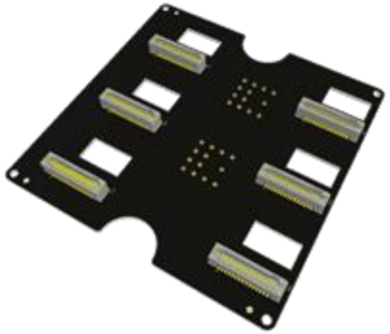
Electronics system modules
Carrier and readout board





Detector module:

- Sensor
- 6 x ASIC
- Carrier board
- Strongback

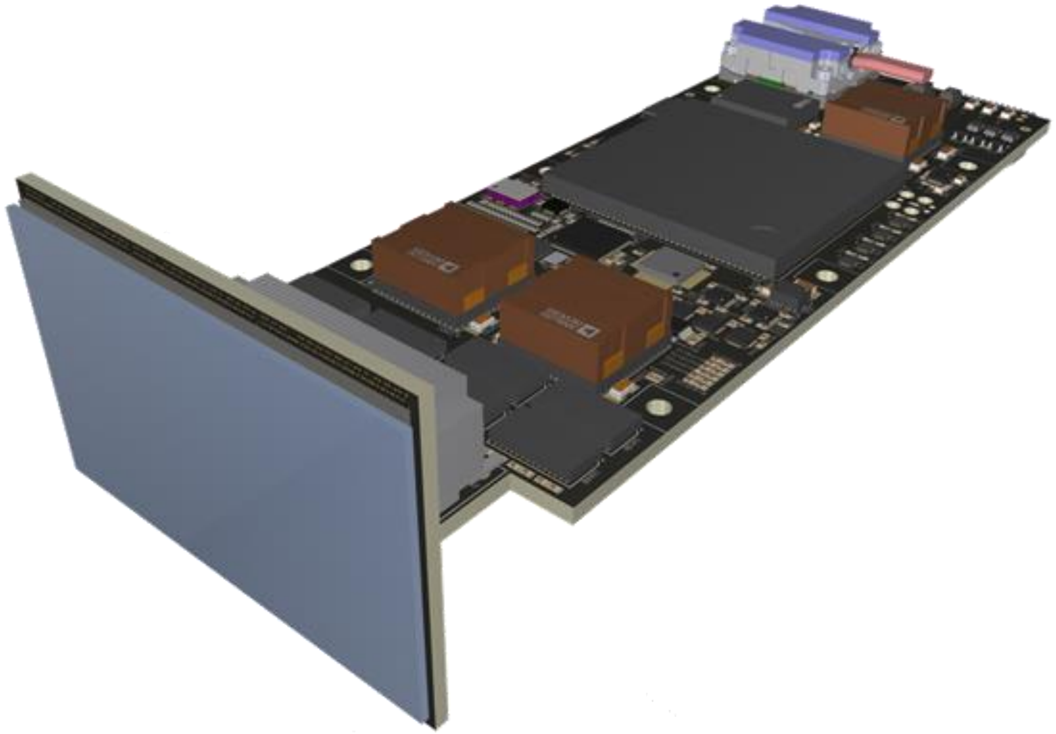


Power distribution board in the rear of the assembly

3x2 Tile Module Boards

Overview

- Two boards instrument a 3x2 sensor/ASIC array
- Carrier board:
  - ASIC/Sensors
  - Serial number, humidity sensor, temperature sensors
  - **84 Gb/s** (6 ASICs x 14 Gb/s/ASIC)
- Readout board
  - Power supply & controls for ASIC
  - FPGA for ASIC control and backend communication
  - Serial number, humidity sensor, voltage and current monitoring

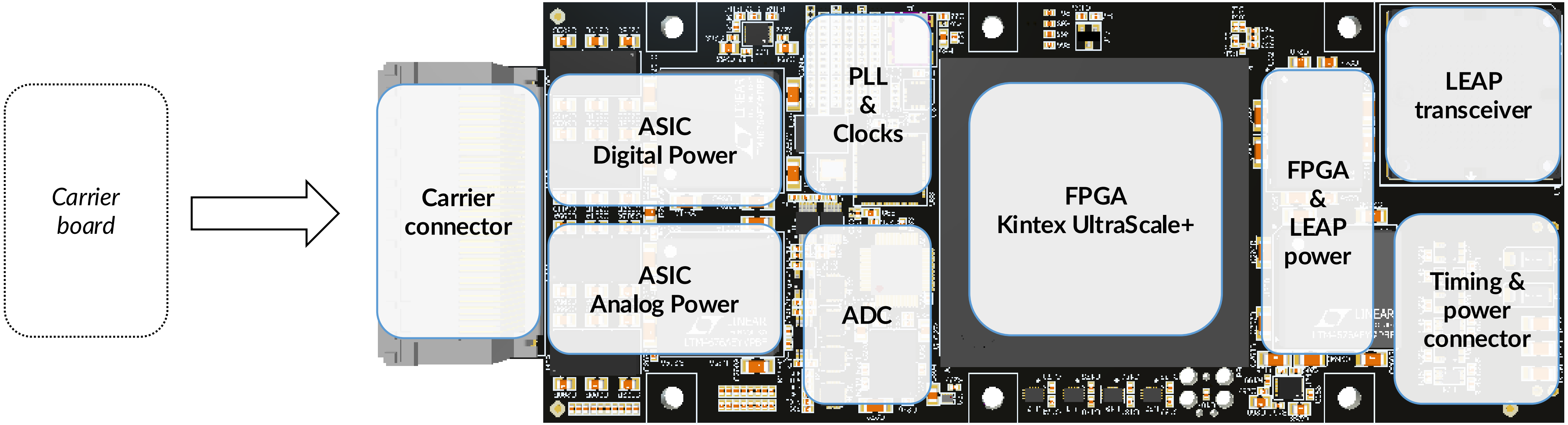


3D model of a 3×2 module rendered in Altium

3x2 Tile Module Boards

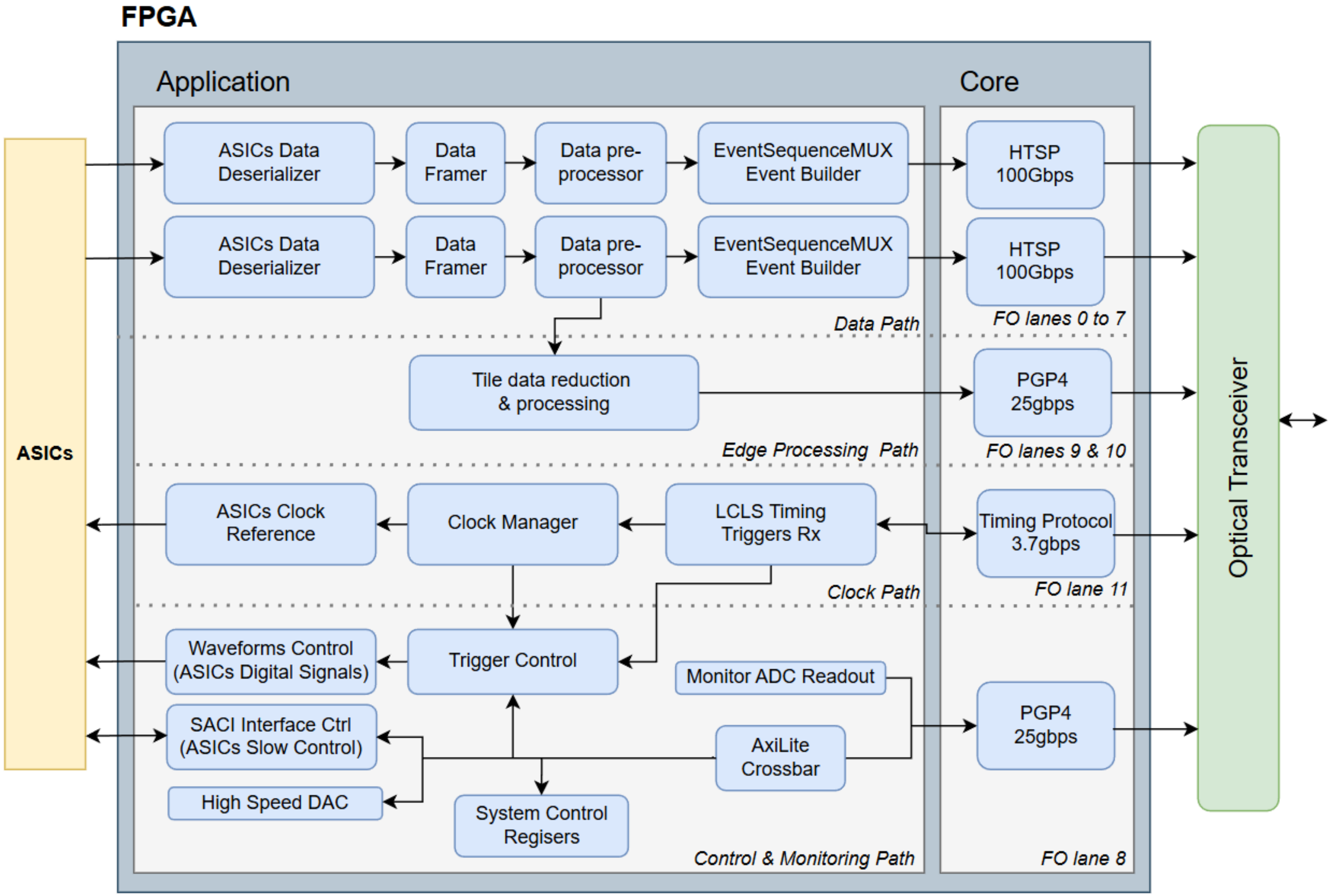
Readout Board

- Readout Board contains all the active components for interfacing with the ASICs on the Carrier Board through a Samtec SEAF8 connector (left side).
- Provides separate analog and digital power to the ASICs with low-speed monitoring of voltages and currents using an ADC.
- Amphenol LEAP transceiver with up to 12 lanes at 25 Gb/s each, interfacing with the external DAQ through optical fibers



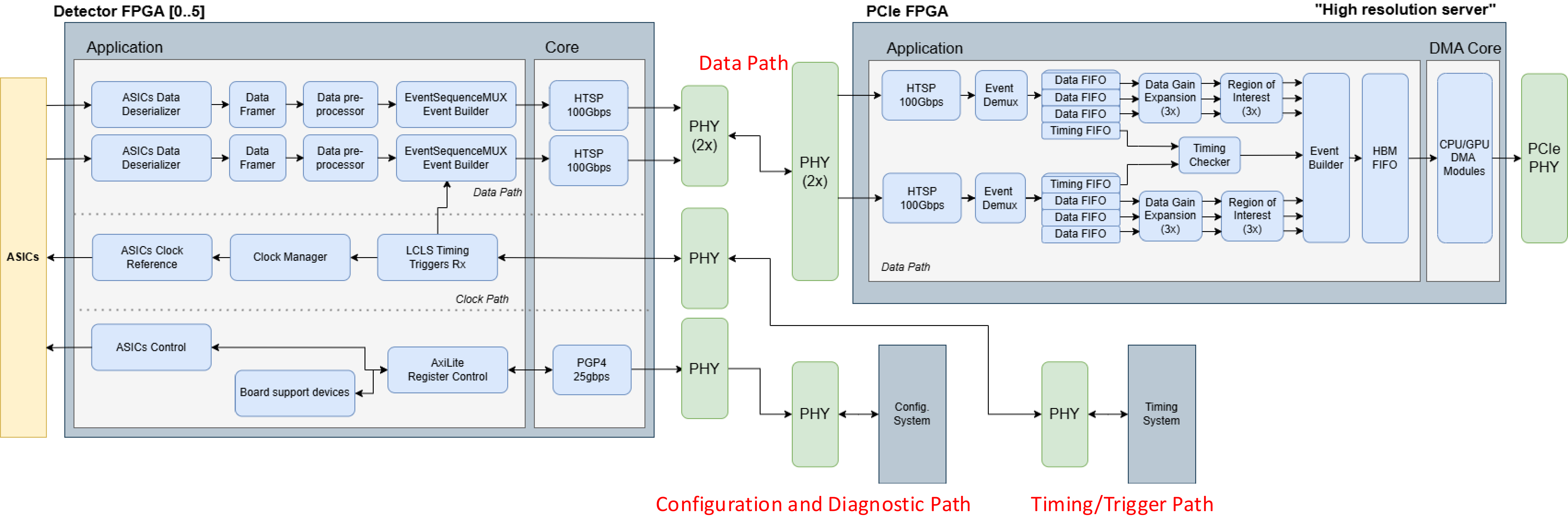
3x2 Tile Module: Firmware Block Diagram

- Pretty Good Protocol Version 4 (PGP4) [1]
  - Used for the ASIC serial protocol
  - Also used for register control/monitoring
- High Throughput Serial Protocol (HTSP) [2]
  - Used to stream data across two 100 Gb/s links (25 Gb/s/lane)
- LCLS Timing and DAQ Interface [3]
  - Synchronize the ASIC to the accelerator
  - Receive triggers on the link
  - Assert backpressure on the link when backend buffers exceed a programmable threshold



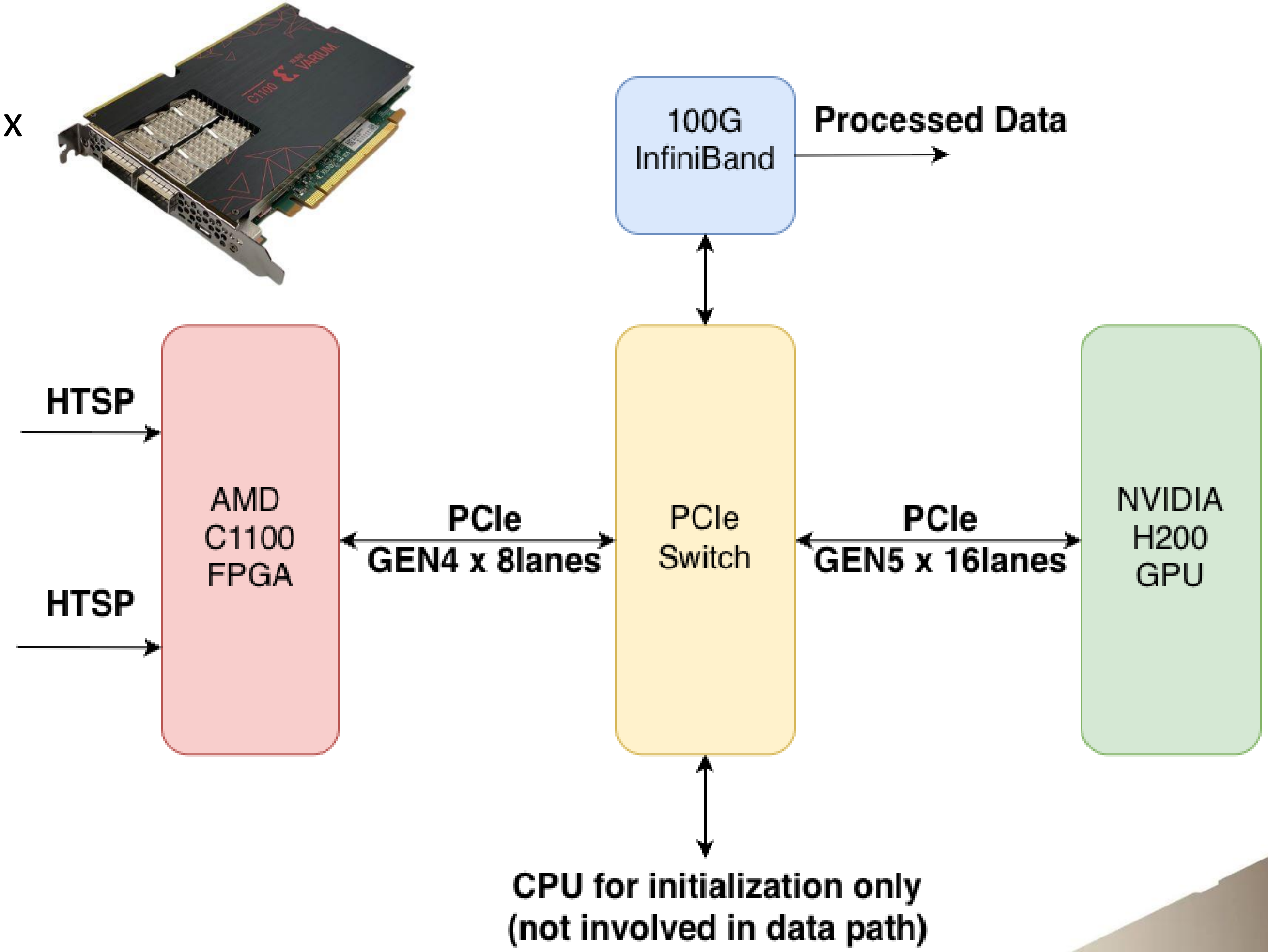
[1] PGP4: https://doi.org/10.1109/NSS/MIC44845.2022.10399159
[2] HTSP: https://doi.org/10.1088/1748-0221/17/07/P07026
[3] LCLS Timing: https://doi.org/10.18429/JACoW-IBIC2023-TH1I01

Connecting 3x2 Tile Module to Back End PCIe FPGA



Backend Data Flow Block Diagram

AMD/Xilinx
C1100



100G InfiniBand

Processed Data

HTSP

HTSP

AMD C1100 FPGA

PCIe GEN4 x 8lanes

PCIe Switch

PCIe GEN5 x 16lanes

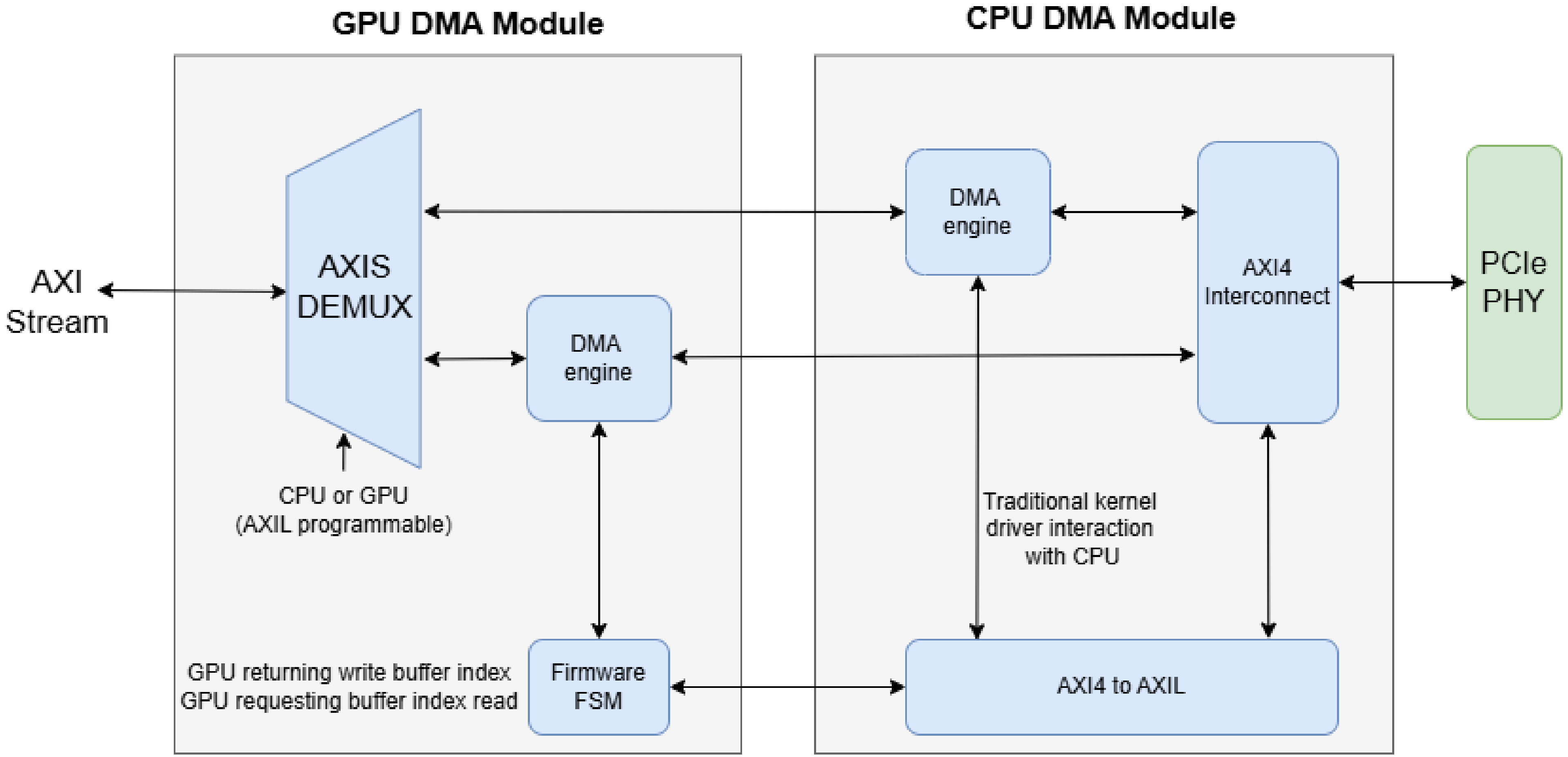
NVIDIA H200 GPU

CPU for initialization only
(not involved in data path)

NVIDIA H200

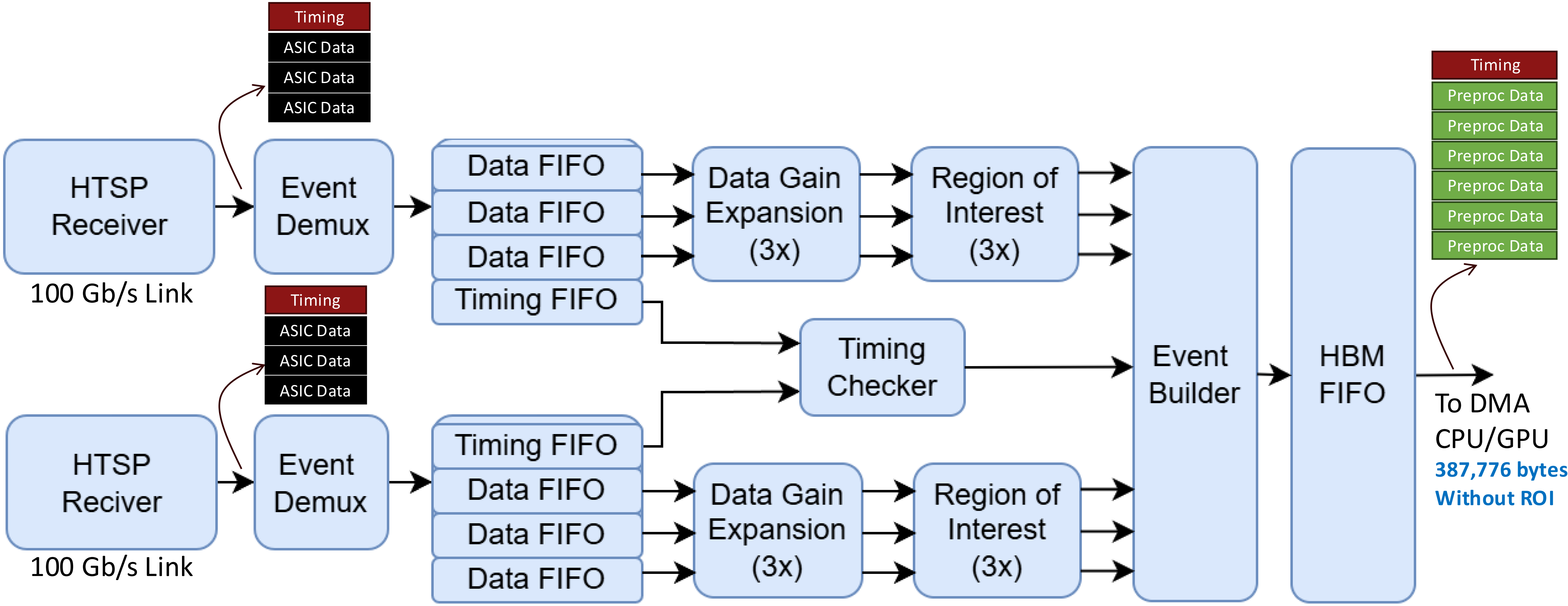
https://developer.nvidia.com/gpudirect

CPU/GPU DMA Block Diagram



- Same DMA engine firmware used in GPU core, PCIe core, and HBM FIFO (not shown in diagram)
  - Focus on reusability of common firmware blocks in our SLAC open-source firmware library
- A simple firmware FSM helps the GPU coordinate with the DMA engine (GPU-driven, not driven by a CPU kernel driver)
- Supports up to 1024 write and 1024 read GPU buffers (FPGA streaming, no buffering)

Event Building the 3x2 Tile Module on Back End FPGA

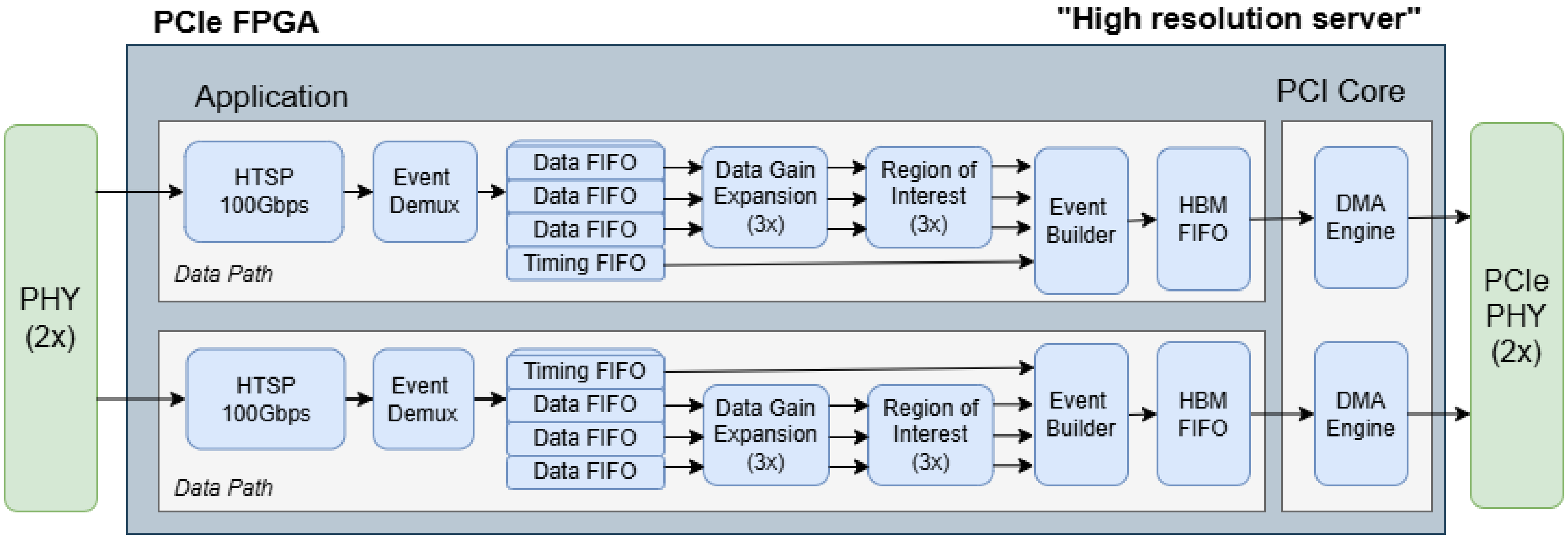


387,776 bytes
Without ROI

42 Gb/s per HTSP link (84 Gb/s total)

Data Gain Expansion:
- Convert a “dual-range” 12-bit ADC value to a float16 for GPU processing

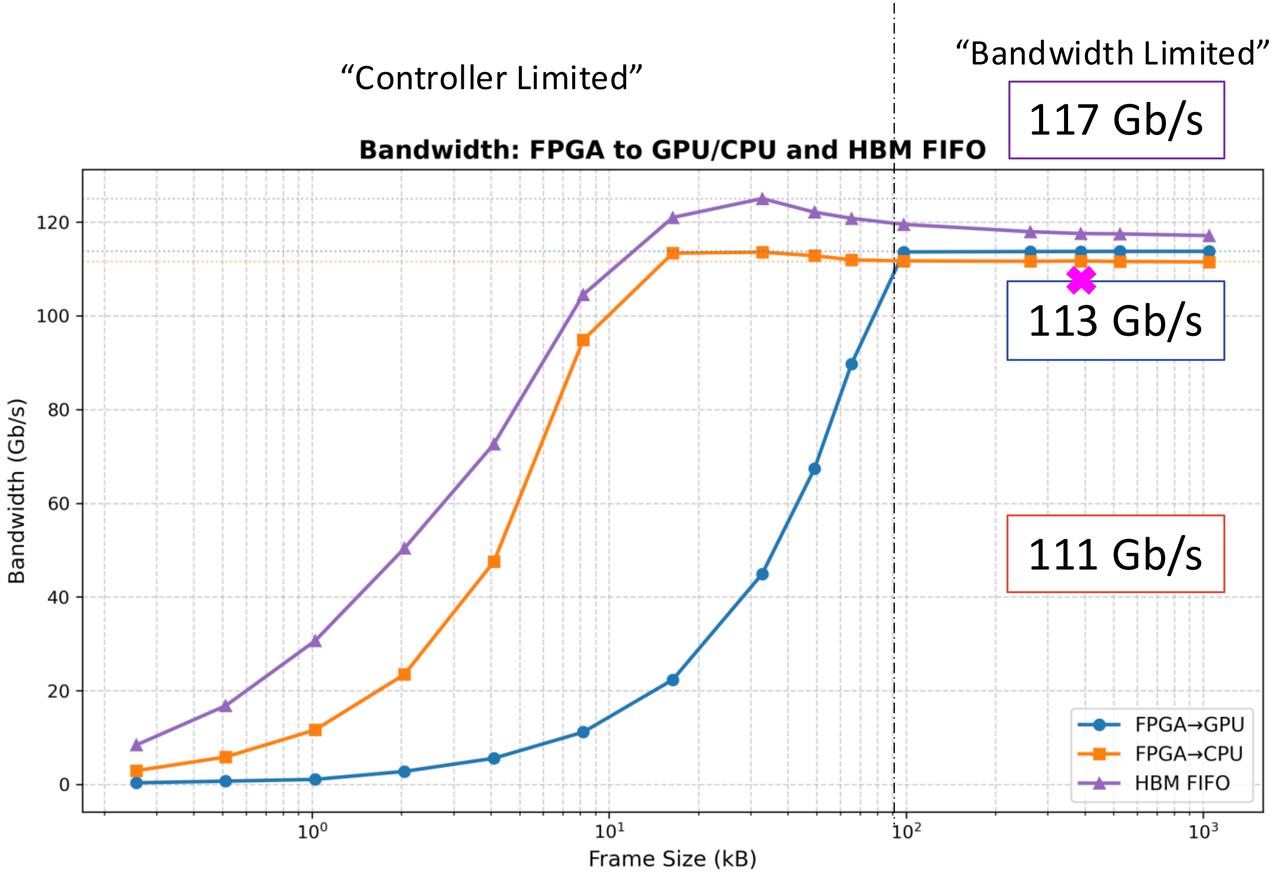
Why not a single 100 Gb/s (instead of dual 100 Gb/s)?



Original Data PCIe firmware block diagram

- Dual 100 Gb/s was chosen even though PCIe bifurcation is **unsupported** on the currently procured servers
- Cabling is forward-compatible with the 100 kHz upgrade
- The 100 kHz upgrade also requires compression on the front board to reduce the data rate from ~250 Gb/s to <200 Gb/s

FPGA→GPU/CPU & HBM FIFO Performance Benchmarks

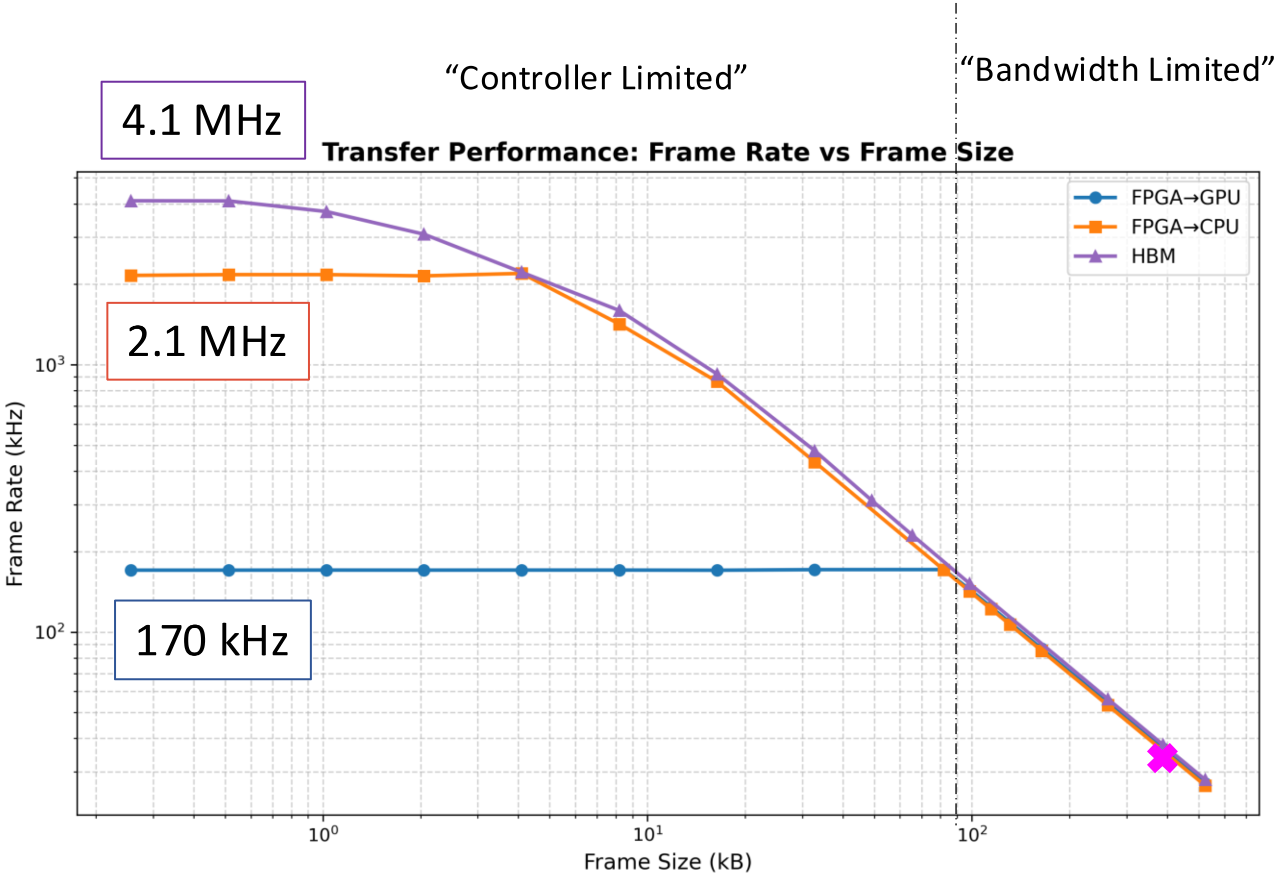

“Controller Limited”

“Bandwidth Limited”

117 Gb/s

113 Gb/s

111 Gb/s


“Controller Limited”

“Bandwidth Limited”

4.1 MHz

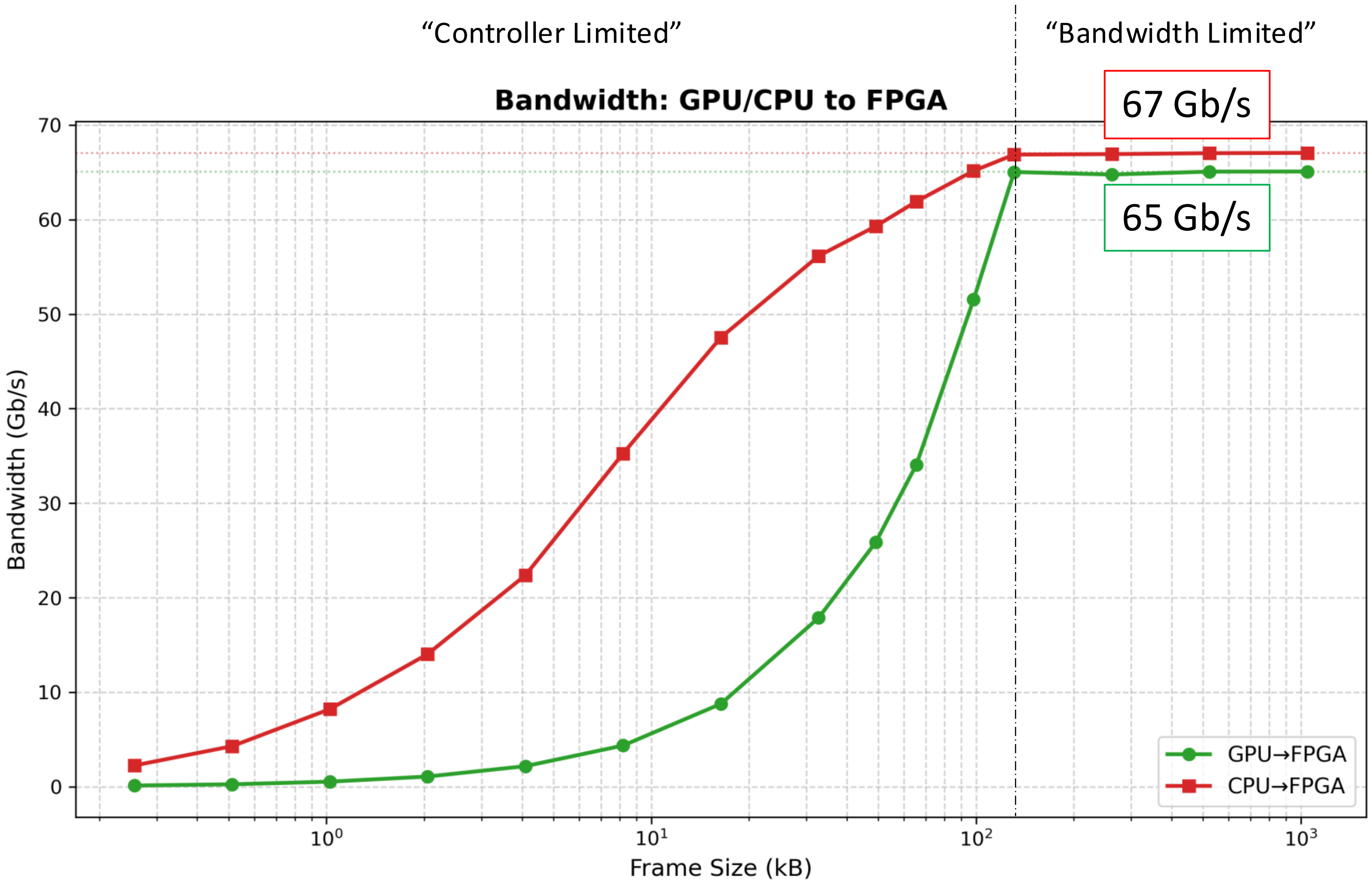
2.1 MHz

170 kHz

- Maximum data frame without ROI (Region of Interest) is **387,776 bytes**
- Maximum frame rate for this system is driven by a **35.714 kHz** laser
- Maximum operating point: **110.79 Gb/s** (= 35.714 kHz x 387,776 bytes)

FPGA = AMD/Xilinx C1100
GPU = NVIDIA RTX PRO 6000 Blackwell
CPU = AMD Ryzen 9 9900X

GPU/CPU⟶FPGA Performance Benchmarks



FPGA = AMD/Xilinx C1100
GPU = NVIDIA RTX PRO 6000 Blackwell
CPU = AMD Ryzen 9 9900X

- We will **NOT** use this path for data collection, but show it here for "**completeness**"
- **Slower** than on the previous slide because these PCIe memory transactions are **non-posted READs**
    - FPGA⟶GPU/CPU: only PCIe **posted WRITE** memory transactions during operation
- GPU uses **GPUDirect** to an InfiniBand card for moving processed data off the server to the data-storage farm

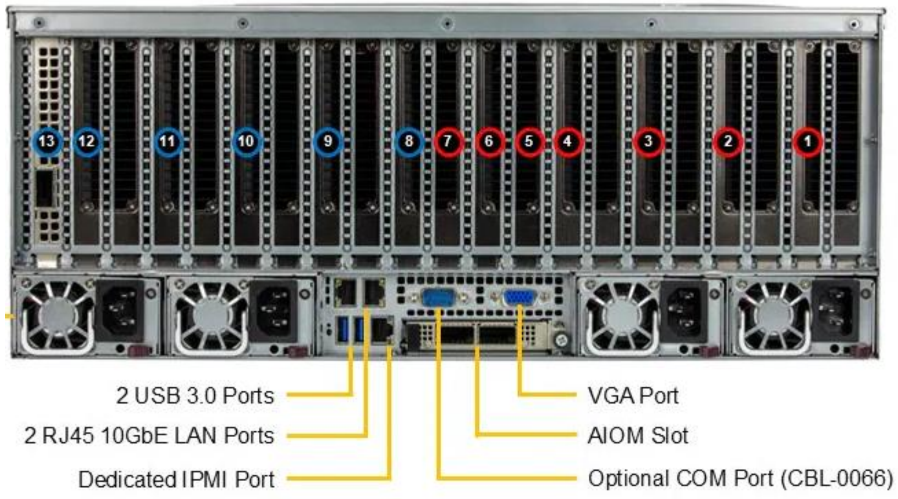
Back End Server’s FPGA/GPU Configuration

- “1 PCIe FPGA per GPU”

- 1 Server = “ePixUHR – 1 Mpixel” (4U rack space)
- 4 Servers = “ePixUHR – 4 Mpixel” (16U rack space)
- 16 Servers = “ePixUHR – 16 Mpixel” (64U rack space)

- CPU[0]: PLX Switch
  - SLOT#1–#3: GPU (H200)
  - SLOT#4–#6: HTSP Data FPGA (C1100)
- Chipset
  - SLOT#7: PGP4 Config FPGA (C1100)
  - AIOM: 100G InfiniBand link
- CPU[1]: PLX Switch
  - SLOT#8–#9: HTSP Data FPGA (C1100)
  - SLOT#10–#12: GPU (H200)
  - SLOT#13: HTSP Data FPGA (C1100)

Supermicro SYS-421GE-TNRT



	Slot Description
1 – 6	PCIe 5.0 x16 FHFL from PLX Switch
7	PCIe 5.0 x16 FHFL
8 – 13	PCIe 5.0 x16 FHFL from PLX Switch

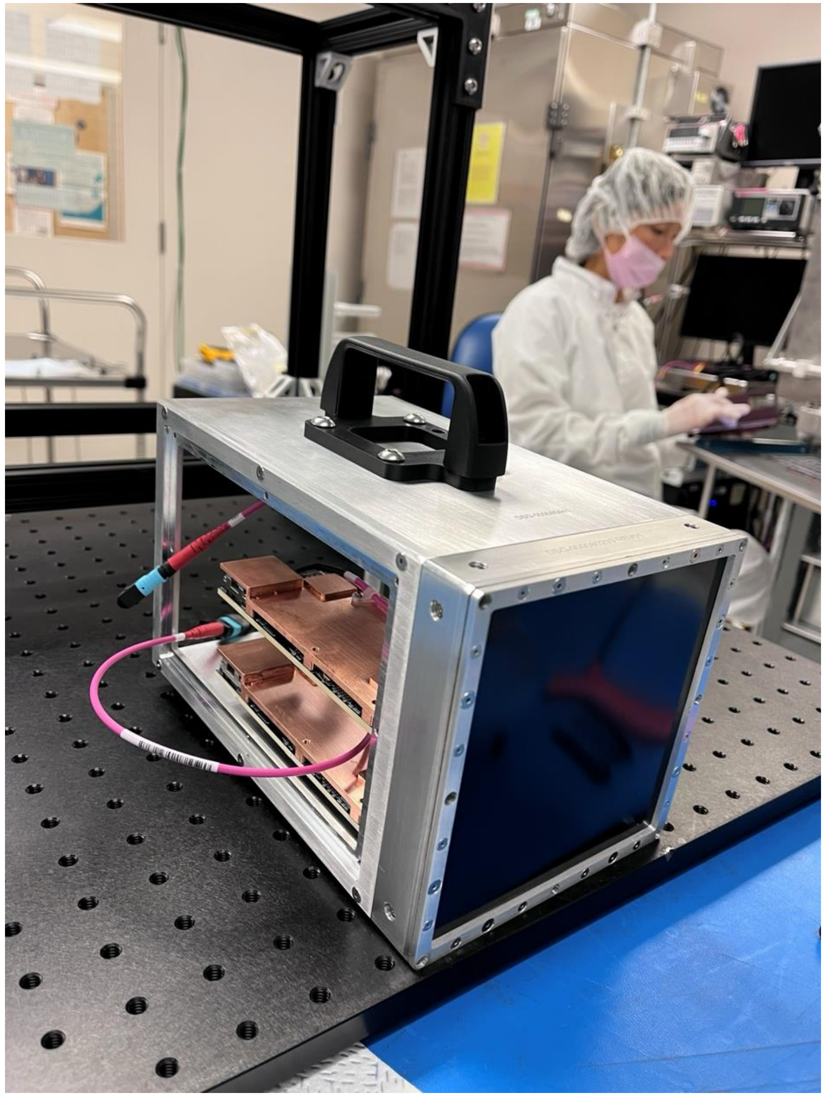
CPU1 🟥 CPU2 🟦

AMD/Xilinx C1100

NVIDIA H200

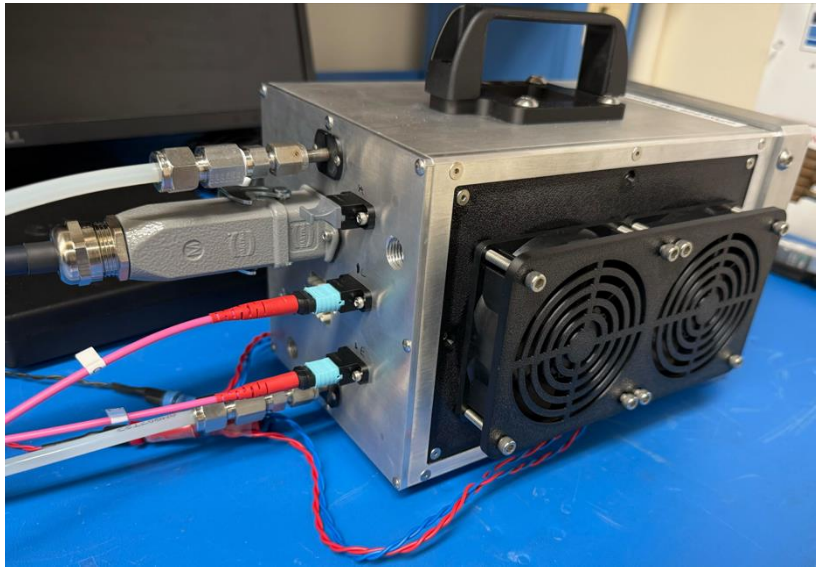
Upcoming Initiatives

- Repeat the FPGA⟶GPU benchmarks on the production Supermicro + NVIDIA H200 configuration.
  - We didn't have the fully populated hardware until last week
- We finally received our sensors last month
- Our first 1 Mpixel camera (air-cooled, for benchtop testing) is complete and is being used to stress-test the firmware/software and surface bugs
- Our deadline is to deliver a 4 Mpix camera by the end of this year

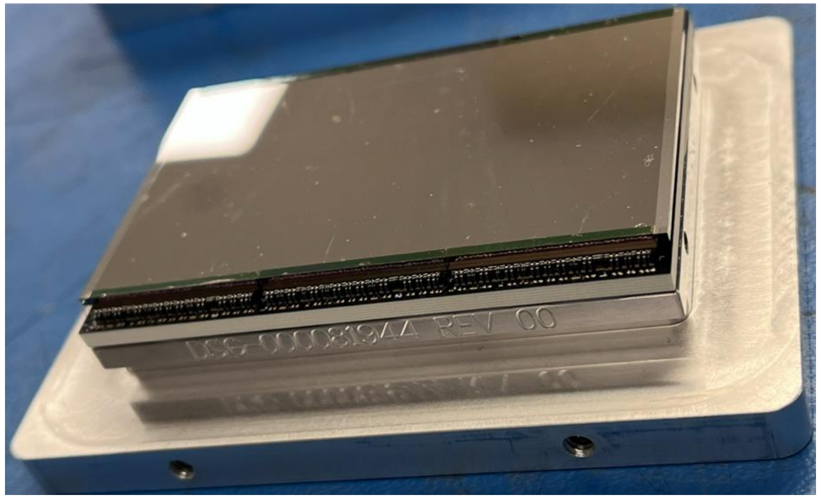


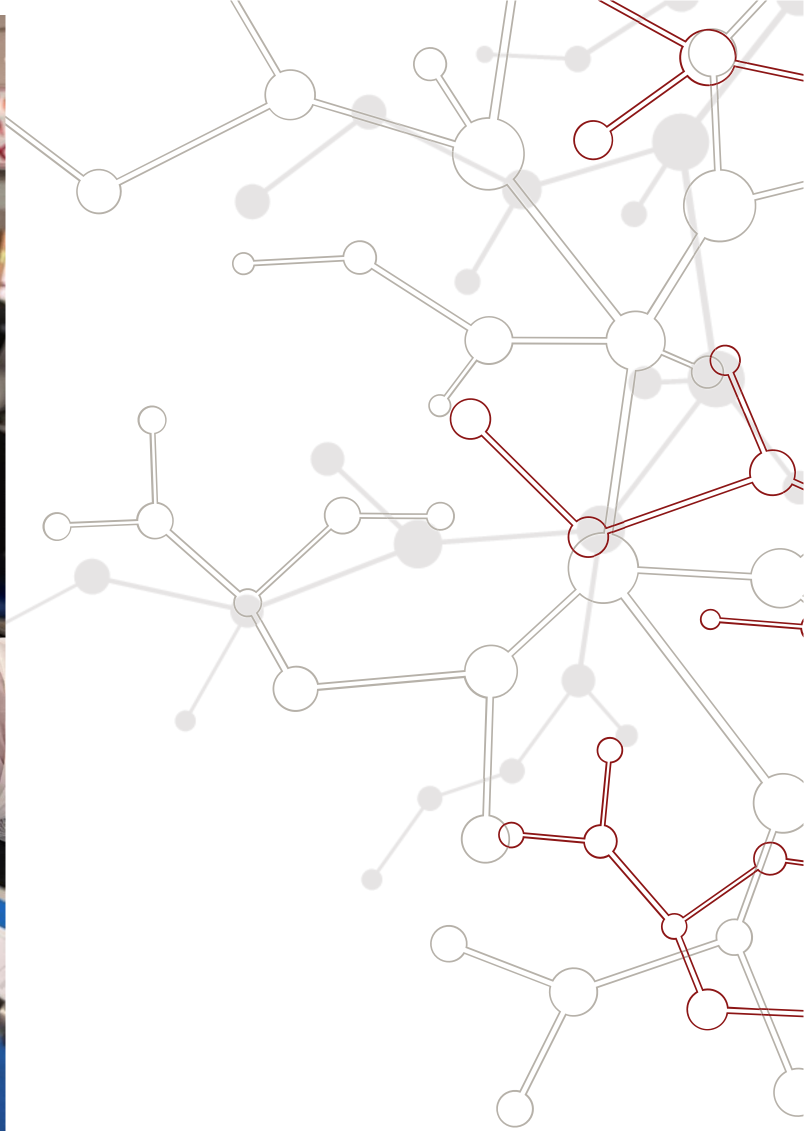
Acknowledgement

- Work supported by the U.S. Department of Energy, under contract number DE-AC02-76SF00515



BACKUP





Open-Source Firmware/Software Links

- DMA Engine for CPU/GPU Transfers:
  - https://slaclab.github.io/aes-stream-drivers/
  - https://github.com/slaclab/axi-pcie-core/tree/main/protocol/gpuAsync
  - https://github.com/slaclab/axi-pcie-core/blob/main/shared/rtl/AxiPcieDma.vhd

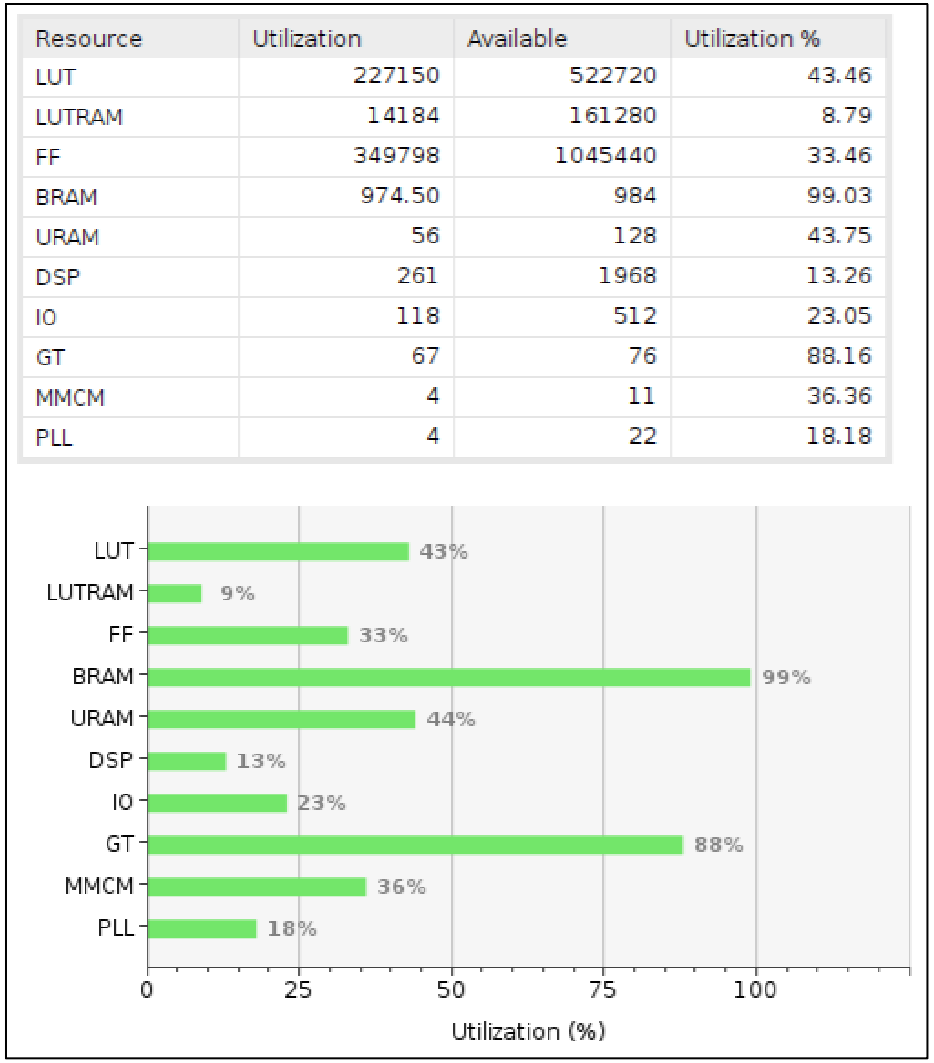
- HBM FIFO Implementation:
  - https://github.com/slaclab/axi-pcie-core/blob/main/hardware/XilinxVariumC1100/hbm/HbmDmaBufferV2.vhd

- Example Project – 100 Gb/s HTSP Communication:
  - https://github.com/slaclab/pgp-pcie-apps/tree/main/firmware/targets/XilinxVariumC1100/XilinxVariumC1100Htsp100GbpsBifurcatedPcie

- Example Project – PGPv4 at 25 Gb/s with FEC:
  - https://github.com/slaclab/pgp-pcie-apps/tree/main/firmware/targets/XilinxVariumC1100/XilinxVariumC1100Pgp4_25Gbps_Fec

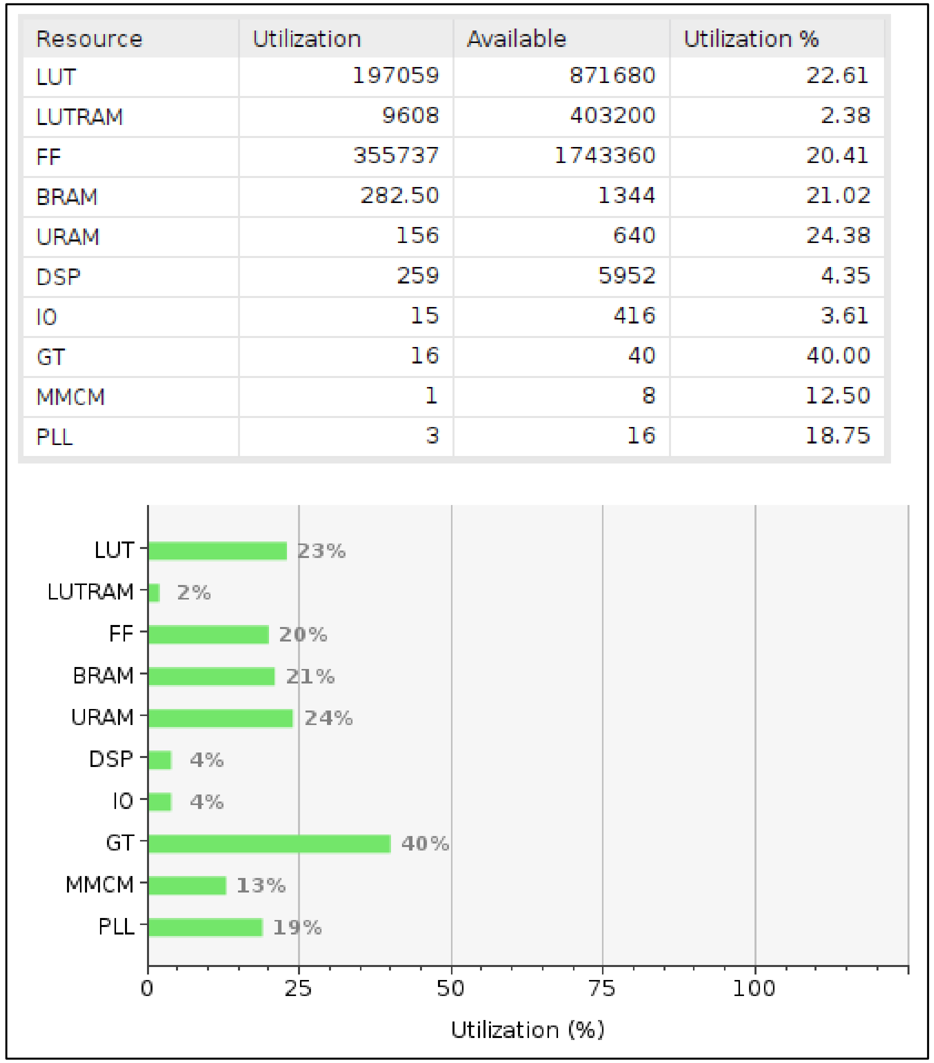
FPGA Resource Tables

3x2 Tile Module FPGA Board



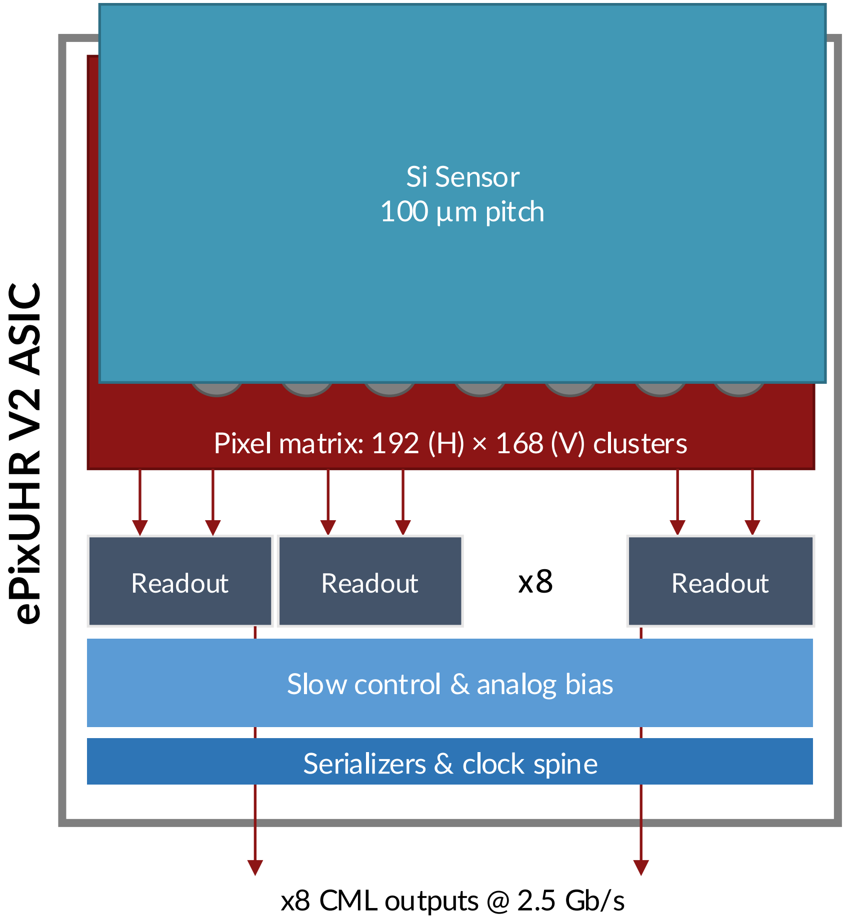
Resource	Utilization	Available	Utilization %
LUT	227150	522720	43.46
LUTRAM	14184	161280	8.79
FF	349798	1045440	33.46
BRAM	974.50	984	99.03
URAM	56	128	43.75
DSP	261	1968	13.26
IO	118	512	23.05
GT	67	76	88.16
MMCM	4	11	36.36
PLL	4	22	18.18

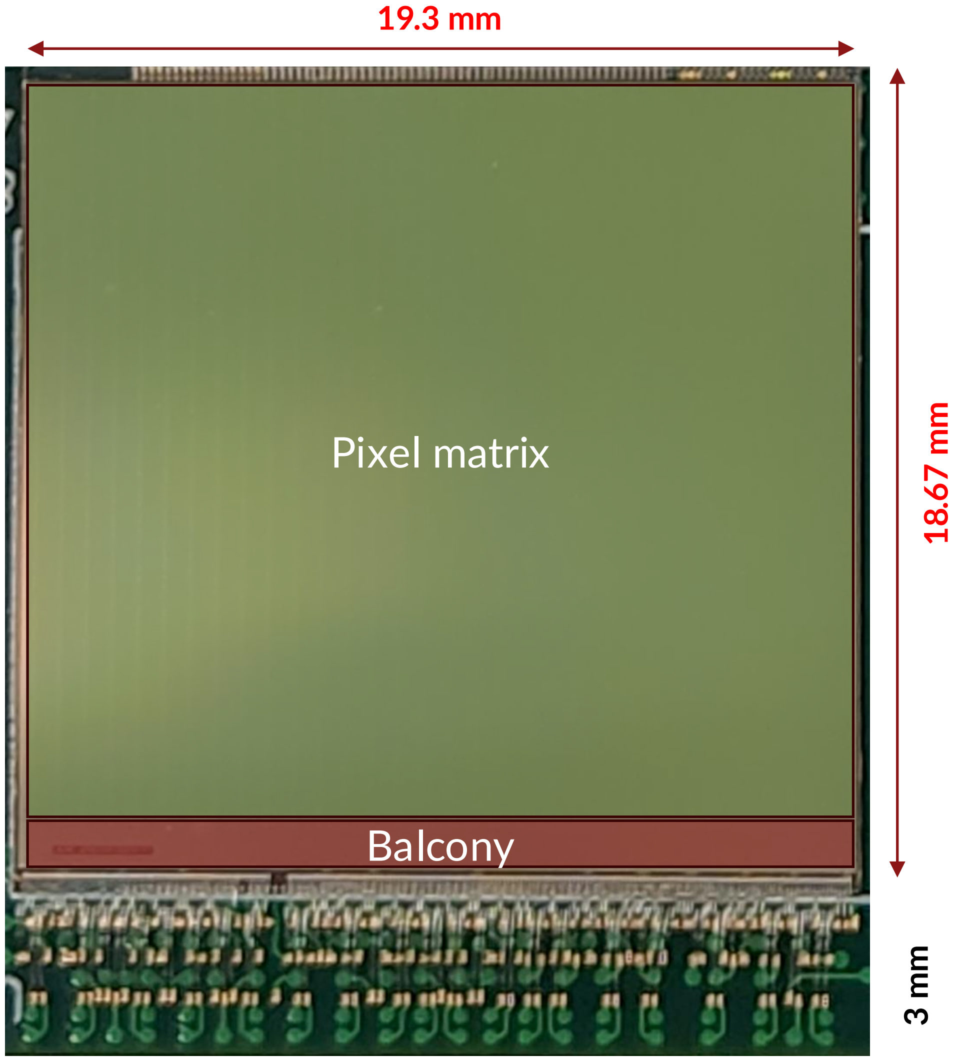
DATA PCIe FPGA Card



Resource	Utilization	Available	Utilization %
LUT	197059	871680	22.61
LUTRAM	9608	403200	2.38
FF	355737	1743360	20.41
BRAM	282.50	1344	21.02
URAM	156	640	24.38
DSP	259	5952	4.35
IO	15	416	3.61
GT	16	40	40.00
MMCM	1	8	12.50
PLL	3	16	18.75

ASIC Architecture (V2 & production)





- Increased distance from guard-ring pads to edge of wire bonding pads to 1.5 mm: 1 mm sensor edge + 0.3 mm clearance requested by Amtech + 0.2 mm safety margin
- Re-aligned the seal ring at the top corners so the X and Y distances from the last bump are equal
- Double dicing needed to keep ASIC-to-ASIC gap <200 µm